ADC141S628Q 14-Bit, 200-kSPS, Pseudo-Differential, Micro-Power ADC

1 Features

- AEC-Q100 Grade 2 Qualified
- 14-Bit Resolution With no Missing Codes
- Specified Performance Up to 200 kSPS
- Pseudo Differential Inputs
- Zero-Power Track Mode
- ±150-mV Swing Around GND on Negative Input
- Separate Digital I/O and Analog Supplies
- Operating Temperature Range of –40°C to +105°C
- SPI™, QSPI™, Microwire, DSP-Compatible Serial Interface
- Conversion Rate: 50 kSPS to 200 kSPS
- INL (–15°C to +65°C): ±0.95 LSB (max)
- DNL: ±0.95 LSB (max)
- Post Calibration TUE (–15°C to +65°C): ±0.5 mV (max)
- SNR: 80 dBc (min)
- THD: –97 dBc (typ)
- ENOB: 13.0 Bits (min)
- Power Consumption:
  - 200 kSPS, 5 V: 4.8 mW (typ)
  - Power-Down, 5 V: 13 µW (typ)

2 Applications

- Automotive Battery Management
- Automotive Navigation
- Portable Systems
- Medical Instruments
- Instrumentation and Control Systems
- Motor Control
- Direct Sensor Interface

3 Description

The ADC141S628Q device is a 14-bit, 200-kSPS, pseudo-differential, analog-to-digital converter (ADC) that is AEC-Q100 grade 2 qualified. The converter is based on a successive-approximation register (SAR) architecture and has pseudo-differential analog inputs. The signal path is maintained from the internal sample-and-hold circuits throughout the ADC to provide excellent common-mode noise rejection. The ADC141S628Q features a zero-power track mode where the ADC is consuming the minimum amount of supply current while the internal sampling capacitor tracks the applied analog input voltage.

The serial data output of the ADC141S628Q is straight binary and is compatible with several standards, such as SPI, QSPI, Microwire, and many common DSP serial interfaces. The ADC141S628Q has no latency which means the conversion result is clocked out by the serial clock input and is the result of the conversion currently in progress.

The ADC141S628Q can be operated with independent analog (VA) and digital input/output (VIO) supplies. VA and VIO can range from 4.5 V to 5.5 V and can be set independent of each other. This functionality allows a user to maximize performance and minimize power consumption. Similarly, the ADC141S628Q uses an external reference that can be varied from 1.0 V to VA allowing users to optimize the full dynamic range of the input. The pseudo-differential input, low power consumption, and small size make the ADC141S628Q ideal for remote data acquisition applications.

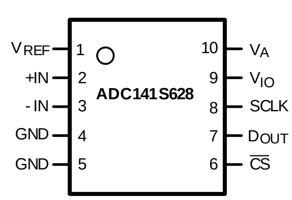
Operation is specified over the temperature range of –40°C to +105°C and clock rates of 0.36 MHz to 3.6 MHz. The ADC141S628Q is available in a 10-lead package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC141S628Q	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Pin Out Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

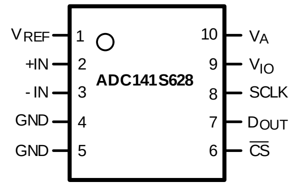
Changes from Revision A (September 2011) to Revision B — **Page**

- Added *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Thermal Information* table, *Functional Block Diagram* section, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Changed MSOP to VSSOP throughout document 1
- Changed *Pin Out Diagram* title from *Connection Diagram* 1
- Deleted *Ordering Information* table 4
- Added I/O column to *Pin Functions* table 4
- Added maximum specification to *Power consumption* row of *Absolute Maximum Ratings* table 5
- Changed footnote 1 of *Absolute Maximum Ratings* table 5
- Changed *Operating Ratings* table title to *Recommended Operating Conditions* 5
- Changed *Operating temperature range* parameter specifications to min and max specifications from $–40 \le T_A \le 105$ max specification 5
- Added f_{SCLK} parameter to *Recommended Operating Conditions* from *Operating Conditions* section; deleted *Operating Conditions* section 5
- Deleted *Package Thermal Resistance* table 5
- Added unit to *Analog input pin, +IN*, *Analog input voltage*, and *Digital input pins voltage range* parameters 5
- Deleted footnote 1 from *Recommended Operating Conditions* table and changed last footnote to include updated link 5
- Changed condition statement of *ADC141S628Q Converter Electrical Characteristics* table to remove boldface condition . 6
- Changed *INL* and *PCTUE* parameter specification test conditions 6
- Added T_A = *–40°C to +105°C* to I_{DCL} parameter test conditions 6
- Changed V_A to max specification from typ specification in V_{REF} parameter 7
- Changed $f_{SCLK} = 0$ to f_{SCLK} = *low* in I_{VA} (PD), I_{VIO} (PD), and I_{VREF} (PD) parameter test conditions 7
- Deleted last footnote from *ADC141S628Q Converter Electrical Characteristics* table 7
- Changed condition statement of *ADC141S628Q Timing Requirements* table to remove boldface condition 8
- Added temperature conditions to certain parameters in the *ADC141S628Q Timing Requirements* table 8

Revision History (continued)

5 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{REF}	Reference input	Voltage reference input. A voltage reference between 1 V and V_A must be applied to this input. V_{REF} must be decoupled to GND with a minimum ceramic capacitor value of 0.1 µF. A bulk capacitor value of 1.0 µF to 10 µF in parallel with the 0.1-µF capacitor is recommended for enhanced performance.
2	+IN	Analog signal input, positive	Noninverting input. +IN is the positive analog input for the signal applied to the ADC141S628Q.
3	–IN	Analog signal input, negative	Inverting input. Must be GND ± 150 mV.
4	GND	Supply	Ground. GND is the ground reference point for all signals applied to the ADC141S628Q.
5	GND	Supply	Ground. GND is the ground reference point for all signals applied to the ADC141S628Q.
6	$\overline{CS}$	Digital input	Chip-select bar. $\overline{CS}$ must be active LOW during an SPI conversion, which begins on the falling edge of $\overline{CS}$. The ADC141S628Q is in acquisition mode when $\overline{CS}$ is HIGH.
7	D_{OUT}	Digital output	Serial data output. The conversion result is provided on D_{OUT}. The serial data output word is comprised of two null bits followed by 14 data bits (MSB first). During a conversion, the data are output on the falling edges of SCLK and are valid on the subsequent rising edges.
8	SCLK	Digital input	Serial clock. SCLK is used to control data transfer and serves as the conversion clock.
9	V_{IO}	Supply	Digital input/output power-supply input. A voltage source between 4.5 V and 5.5 V must be applied to this input. V_{IO} must be decoupled to GND with a minimum ceramic capacitor value of 0.1 µF.
10	V_A	Supply	Analog power-supply input. A voltage source between 4.5 V and 5.5 V must be applied to this input. V_A must be decoupled to GND with a minimum ceramic capacitor value of 0.1 µF.

6 Specifications

6.1 Absolute Maximum Ratings

If military/aerospace specified devices are required, please contact the Texas Instruments sales office, distributors for availability and specifications.(1)(2)

	MIN	MAX	UNIT
V_A relative to GND	–0.3	6	V
V_{IO} relative to GND	–0.3	6	V
Voltage between any two pins(3)		6	V
Current in or out of any pin(3)		±10	mA
Package input current(3)		±50	mA
Power consumption at T_A = 25°C		See (4)	
Junction temperature		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are measured with respect to GND = 0 V, unless otherwise specified.
(3) When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < GND or V_{IN} > V_A), the current at that pin must be limited to 10 mA and V_{IN} must be within the absolute maximum rating for that pin. The 50-mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to five.
(4) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula P_DMAX = ($T_J$max – T_A) / θ_{JA}. The values for maximum power dissipation listed above are reached only when the ADC141S628Q is operated in a severe fault condition (for example, when input or output pins are driven beyond the power supply voltages, or the power-supply polarity is reversed). These conditions must be avoided.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1250	
		Machine model (MM)	±300	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions(1)(2)

	MIN	NOM	MAX	UNIT
Operating temperature range	–40		105	°C
Supply voltage, V_A	4.5		5.5	V
Supply voltage, V_{IO}	4.5		5.5	V
Reference voltage, V_{REF}	1.0		V_A	V
SCLK frequency, f_{SCLK}	0.9		3.6	MHz
Analog input pin, +IN	GND		V_A	V
Analog input pin, –IN			GND ±150 mV	mV
Analog input voltage	GND		V_{REF}	V
Digital input pins voltage range	GND		V_{IO}	V
Clock frequency	50k		3.6M	Hz

(1) All voltages are measured with respect to GND = 0 V, unless otherwise specified.
(2) For soldering specifications, see the *Absolute Maximum Ratings for Soldering* application report.

6.4 ADC141S628Q Converter Electrical Characteristics

The following specifications apply for $V_A = V_{IO}$ = 5 V, V_{REF} = 4.096 V, and f_{SCLK} = 0.9 MHz to 3.6 MHz; f_{IN} = 20 kHz and C_L = 25 pF, unless otherwise noted. All specifications are at T_A = 25°C, unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CONVERTER CHARACTERISTICS						
	Resolution with no missing codes	T_A = –40°C to +105°C			14	Bits
INL	Integral nonlinearity			±0.5		LSB
		T_A = –15°C to +65°C			±0.95	
		T_A = –40°C to +105°C			±1	
DNL	Differential nonlinearity			±0.5		LSB
		T_A = –40°C to +105°C			±0.95	
PCTUE	Post calibration total unadjusted error	–15°C ≤ T_A ≤ 65°C			±0.5	mV
		–40°C ≤ T_A ≤ 105°C	–0.85		1	
OE	Offset error			–1		LSB
		T_A = –40°C to +105°C			±5	
FSE	Full-scale error			–3		LSB
		T_A = –40°C to +105°C			±7	
GE	Gain error			–1.5		LSB
		T_A = –40°C to +105°C			±6	
DYNAMIC CONVERTER CHARACTERISTICS						
SINAD	Signal-to-noise and distortion ratio	V_{IN} = –0.1 dBFS		82		dBc
		V_{IN} = –0.1 dBFS, T_A = –40°C to +105°C	80			
SNR	Signal-to-noise ratio	V_{IN} = –0.1 dBFS		82		dBc
		V_{IN} = –0.1 dBFS, T_A = –40°C to +105°C	80			
THD	Total harmonic distortion	V_{IN} = –0.1 dBFS		–97		dBc
SFDR	Spurious-free dynamic range	V_{IN} = –0.1 dBFS		98		dBc
ENOB	Effective number of bits	V_{IN} = –0.1 dBFS		13.4		Bits
		V_{IN} = –0.1 dBFS, T_A = –40°C to +105°C	13.0			
FPBW	–3-dB full-power bandwidth	Output at 70.7%FS with FS input, single-ended input		22		MHz
ANALOG INPUT CHARACTERISTICS						
V_{IN}	(+IN) – (–IN)	T_A = –40°C to +105°C	GND		V_{REF}	V
+IN	Noninverting input	T_A = –40°C to +105°C	–0.15		V_{REF} + 0.15	V
–IN	Inverting input	T_A = –40°C to +105°C	–0.15		0.15	V
I_{DCL}	DC leakage current	$V_{IN} = V_{REF}$ or V_{IN} = 0, T_A = –40°C to +105°C			±1	µA
C_{INA}	Input capacitance	In acquisition mode		14		pF
		In conversion mode		3.4		
CMRR	Common-mode rejection ratio	See the *Specification Definitions* section for the test condition		76		dB

(1) Typical values are at T_J = 25°C and represent most likely parametric norms. Test limits are specified to TI's average outgoing quality level (AOQL).

ADC141S628Q Converter Electrical Characteristics (continued)

The following specifications apply for $V_A = V_{IO} = 5$ V, $V_{REF} = 4.096$ V, and $f_{SCLK} = 0.9$ MHz to 3.6 MHz; $f_{IN} = 20$ kHz and $C_L = 25$ pF, unless otherwise noted. All specifications are at $T_A = 25°C$, unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT CHARACTERISTICS						
V_{IH}	Input high voltage			1.9		V
		T_A = –40°C to +105°C	2.3			
V_{IL}	Input low voltage			1.0		V
		T_A = –40°C to +105°C			0.7	
I_{IN}	Input current	V_{IN} = 0 V or V_A, T_A = –40°C to +105°C			±1	µA
C_{IND}	Input capacitance			2		pF
		T_A = –40°C to +105°C			4	
DIGITAL OUTPUT CHARACTERISTICS						
V_{OH}	Output high voltage	I_{SOURCE} = 200 µA		V_A – 0.05		V
		I_{SOURCE} = 200 µA, T_A = –40°C to +105°C	V_A – 0.2			
		I_{SOURCE} = 1 mA		V_A – 0.16		
V_{OL}	Output low voltage	I_{SINK} = 200 µA		0.01		V
		I_{SINK} = 200 µA, T_A = –40°C to +105°C			0.4	
		I_{SINK} = 1 mA		0.05		
I_{OZH}, I_{OZL}	Tri-state leakage current	Force 0 V or V_A, T_A = –40°C to +105°C			±1	µA
C_{OUT}	Tri-state output capacitance	Force 0 V or V_A		2		pF
		Force 0 V or V_A, T_A = –40°C to +105°C			4	
	Output coding			Straight binary		
POWER-SUPPLY CHARACTERISTICS						
V_A	Analog supply voltage range	T_A = –40°C to +105°C	4.5		5.5	V
V_{IO}	Digital input/output supply voltage range(2)	T_A = –40°C to +105°C	4.5		5.5	V
V_{REF}	Reference voltage range	T_A = –40°C to +105°C	1.0		V_A	V
I_{VA} (Conv)	Analog supply current, conversion mode	f_{SCLK} = 3.6 MHz, f_S = 200 kSPS		740		µA
		f_{SCLK} = 3.6 MHz, f_S = 200 kSPS, T_A = –40°C to +105°C			970	
I_{VIO} (Conv)	Digital I/O supply current, conversion mode	f_{SCLK} = 3.6 MHz, f_S = 200 kSPS		170		µA
		f_{SCLK} = 3.6 MHz, f_S = 200 kSPS, T_A = –40°C to +105°C			260	
I_{VREF} (Conv)	Reference current, conversion mode	f_{SCLK} = 3.6 MHz, f_S = 200 kSPS		45		µA
		f_{SCLK} = 3.6 MHz, f_S = 200 kSPS, T_A = –40°C to +105°C			80	
I_{VA} (PD)	Analog supply current, power-down mode ($\overline{CS}$ high)	f_{SCLK} = 3.6 MHz		8		µA
		f_{SCLK} = low		2		
		f_{SCLK} = low, T_A = –40°C to +105°C			3	
I_{VIO} (PD)	Digital I/O supply current, power-down mode ($\overline{CS}$ high)	f_{SCLK} = 3.6 MHz		3		µA
		f_{SCLK} = low		0.1		
		f_{SCLK} = low, T_A = –40°C to +105°C			0.7	

(2) The value of V_{IO} is independent of the value of V_A. For example, V_{IO} can be operating at 5 V while V_A is operating at 4.5 V or V_{IO} can be operating at 4.5 V while V_A is operating at 5 V.

ADC141S628Q Converter Electrical Characteristics (continued)

The following specifications apply for $V_A = V_{IO} = 5$ V, $V_{REF} = 4.096$ V, and $f_{SCLK} = 0.9$ MHz to 3.6 MHz; $f_{IN} = 20$ kHz and $C_L = 25$ pF, unless otherwise noted. All specifications are at $T_A = 25°C$, unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-SUPPLY CHARACTERISTICS (continued)						
I_{VREF} (PD)	Reference current, power-down mode ($\overline{CS}$ high)	f_{SCLK} = 3.6 MHz		0.1		µA
		f_{SCLK} = low		0.1		
		f_{SCLK} = low, T_A = –40°C to +105°C			0.2	
PWR (Conv)	Power consumption, conversion mode	f_{SCLK} = 3.6 MHz, f_S = 200 kSPS		4.8		mW
		f_{SCLK} = 3.6 MHz, f_S = 200 kSPS, T_A = –40°C to +105°C			6.5	
PWR (PD)	Power consumption, power-down mode ($\overline{CS}$ high)	f_{SCLK} = 0, $V_A = V_{IO} = V_{REF}$ = 5.0 V		11		µW
		f_{SCLK} = 0, $V_A = V_{IO} = V_{REF}$ = 5.0 V, T_A = –40°C to +105°C			19.5	
PSRR	Power-supply rejection ratio	See the *Specification Definitions* section for the test condition		–85		dB
AC ELECTRICAL CHARACTERISTICS						
f_{SCLK}	Minimum clock frequency	T_A = –40°C to +105°C	3.6		0.9	MHz
f_S	Maximum sample rate	T_A = –40°C to +105°C	200			kSPS
t_{ACQ}	Acquisition, track time	T_A = –40°C to +105°C	833			ns
t_{CONV}	Conversion, hold time	T_A = –40°C to +105°C	15			SCLK cycles
t_{AD}	Aperture delay	See the *Specification Definitions* section		6		ns

6.5 ADC141S628Q Timing Requirements

The following specifications apply for $V_A = V_{IO} = 5$ V, $V_{REF} = 4.096$ V, $f_{SCLK} = 0.9$ MHz to 3.6 MHz, and $C_L = 25$ pF, unless otherwise noted. All specifications are at $T_A = 25°C$, unless otherwise noted.(1)

			MIN	NOM	MAX	UNIT
t_{CSS}	$\overline{CS}$ setup time prior to an SCLK rising edge			3		ns (min)
		–40°C to +105°C	6			ns
				1 / f_{SCLK} – 3		ns (max)
		–40°C to +105°C			1 / f_{SCLK} – 6	ns
t_{DH}	D_{OUT} hold time after an SCLK falling edge			10		ns (min)
		–40°C to +105°C	6			ns
t_{DA}	D_{OUT} access time after an SCLK falling edge			28		ns (max)
		–40°C to +105°C			40	ns
t_{DIS}	D_{OUT} disable time after the rising edge of $\overline{CS}$(2)			10		ns (max)
					20	ns
t_{CS}	Minimum $\overline{CS}$ pulse duration			5		ns (min)
		–40°C to +105°C	20			ns
t_{EN}	D_{OUT} enable time after the falling edge of $\overline{CS}$			32		ns (max)
					51	ns
t_{CH}	SCLK high time	–40°C to +105°C	111			ns
t_{CL}	SCLK low time	–40°C to +105°C	111			ns
t_r	D_{OUT} rise time			7		ns
t_f	D_{OUT} fall time			7		ns

(1) Typical values are at T_J = 25°C and represent most likely parametric norms. Test limits are specified to TI's average outgoing quality level (AOQL).
(2) t_{DIS} is the time for D_{OUT} to change 10% while being loaded by the timing test circuit (see Figure 2).

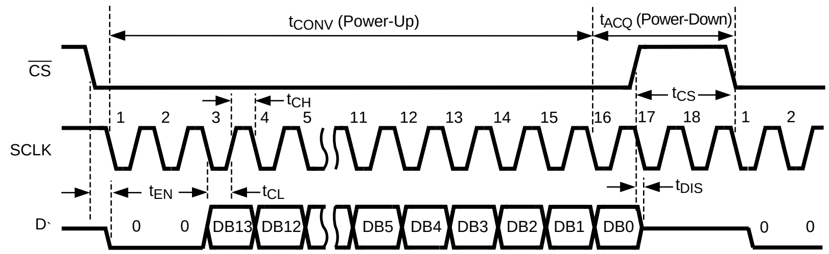


Figure 1. ADC141S628Q Single Conversion Timing Diagram

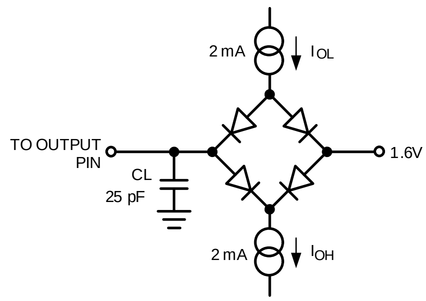


Figure 2. Timing Test Circuit

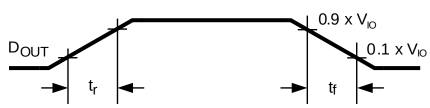


Figure 3. D_{OUT} Rise and Fall Times

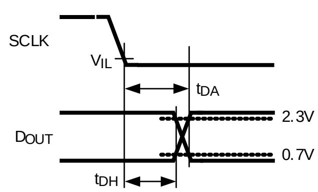


Figure 4. D_{OUT} Hold and Access Times

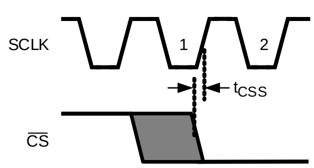


Figure 5. Valid $\overline{CS}$ Assertion Times

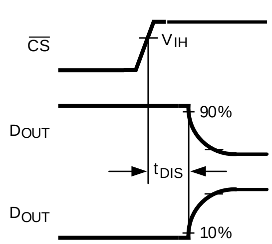


Figure 6. Voltage Waveform for t_{DIS}

6.6 Typical Characteristics

V_A = $_{VIO}$ = V_{REF} = 5 V, f_{SCLK} = 3.6 MHz, f_{SAMPLE} = 200 kSPS, T_A = +25°C, and f_{IN} = 20 kHz (unless otherwise noted)

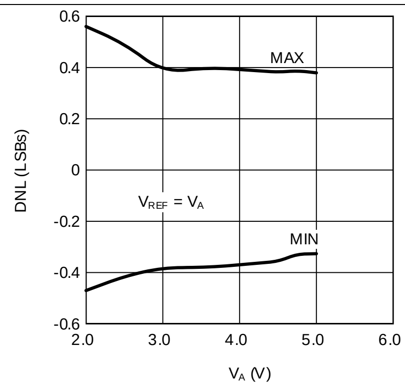


Figure 7. DNL vs V_A

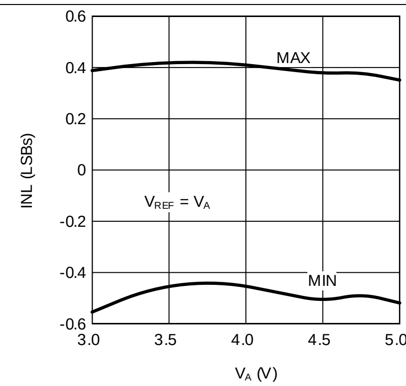


Figure 8. INL vs V_A

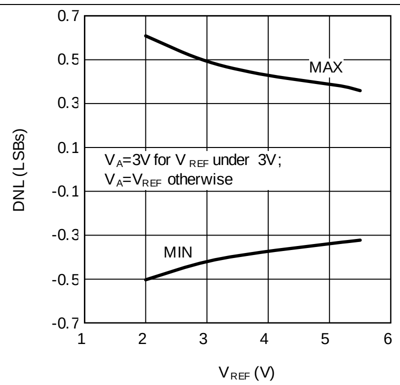


Figure 9. DNL vs V_{REF}

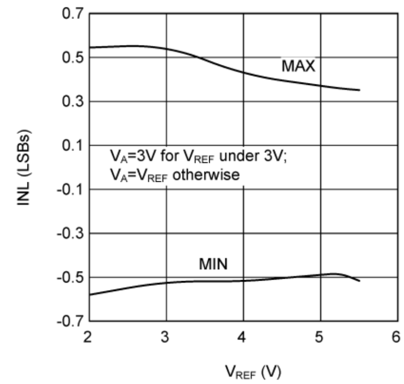


Figure 10. INL vs V_{REF}

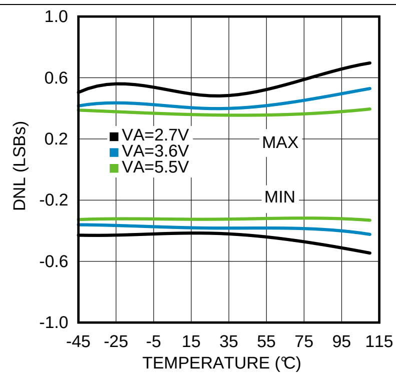


Figure 11. DNL vs Temperature

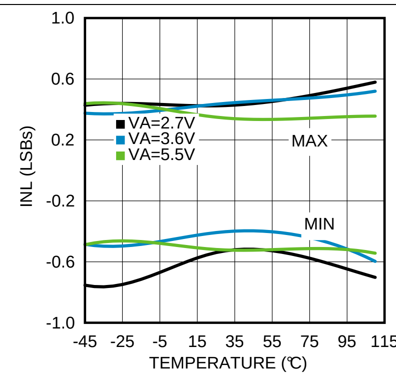


Figure 12. INL vs Temperature

Typical Characteristics (continued)

$V_A = V_{IO} = V_{REF} = 5$ V, $f_{SCLK} = 3.6$ MHz, $f_{SAMPLE} = 200$ kSPS, $T_A = +25°C$, and $f_{IN} = 20$ kHz (unless otherwise noted)

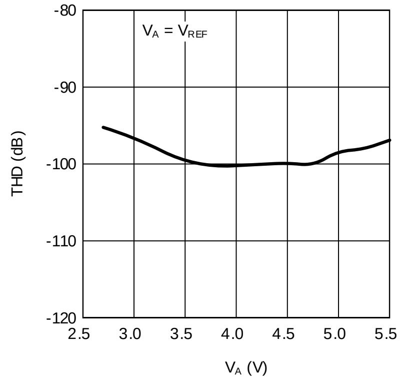


Figure 13. THD vs V_A

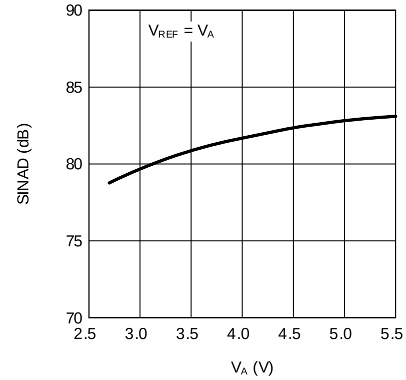


Figure 14. SINAD vs V_A

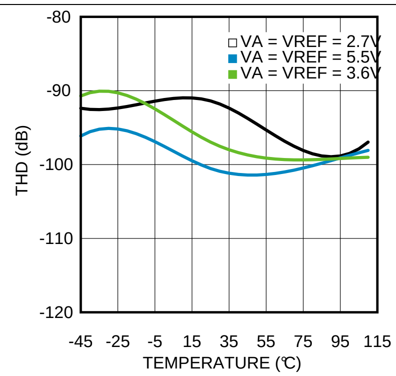


Figure 15. THD vs Temperature

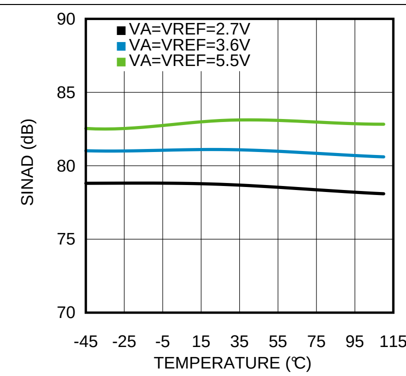


Figure 16. SINAD vs Temperature

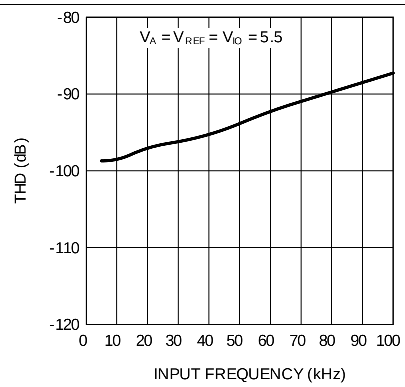


Figure 17. THD vs Input Frequency

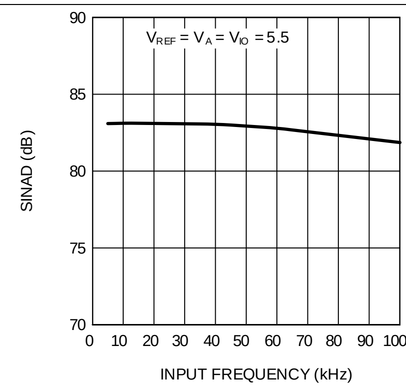


Figure 18. SINAD vs Input Frequency

Typical Characteristics (continued)

$V_A = V_{IO} = V_{REF} = 5$ V, $f_{SCLK} = 3.6$ MHz, $f_{SAMPLE} = 200$ kSPS, $T_A = +25°C$, and $f_{IN} = 20$ kHz (unless otherwise noted)

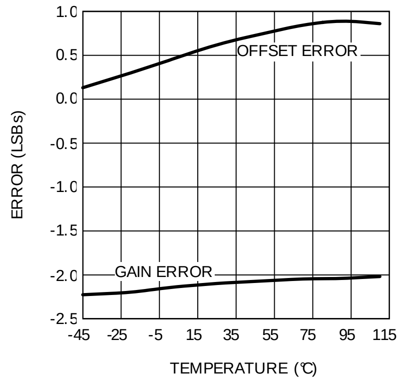


Figure 19. Gain and Offset Error vs Temperature

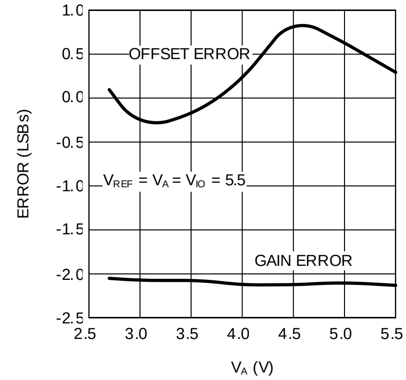


Figure 20. Gain and Offset Error vs V_A

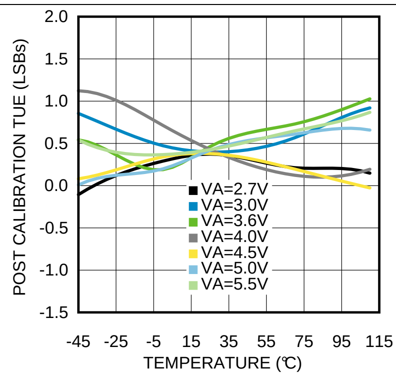


Figure 21. Max TUE vs Temperature

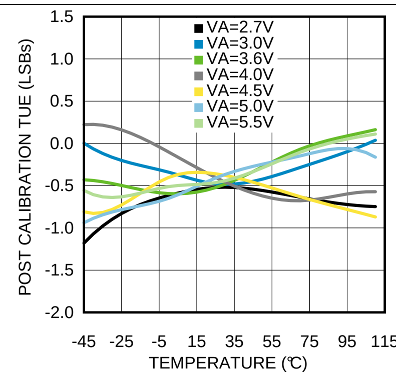


Figure 22. Min TUE vs Temperature

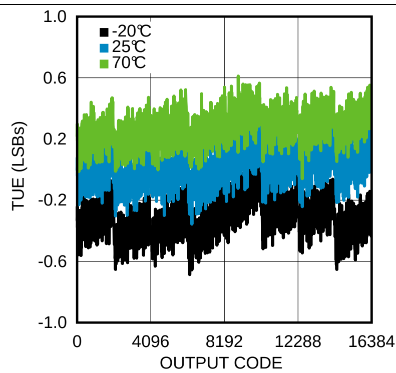


Figure 23. TUE vs Code Over Temperature

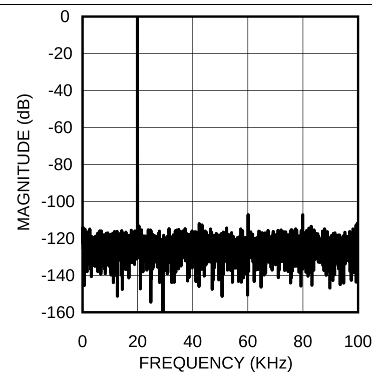


Figure 24. Typical Spectrum

Typical Characteristics (continued)

V_A = V_{IO} = V_{REF} = 5 V, f_{SCLK} = 3.6 MHz, f_{SAMPLE} = 200 kSPS, T_A = +25°C, and f_{IN} = 20 kHz (unless otherwise noted)

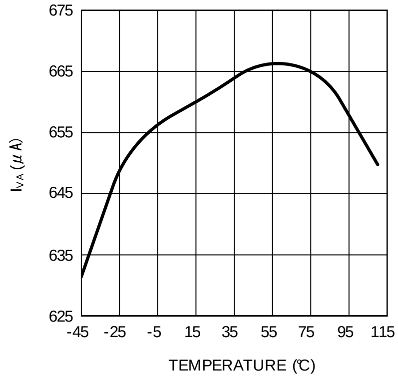


Figure 25. V_A Current vs Temperature

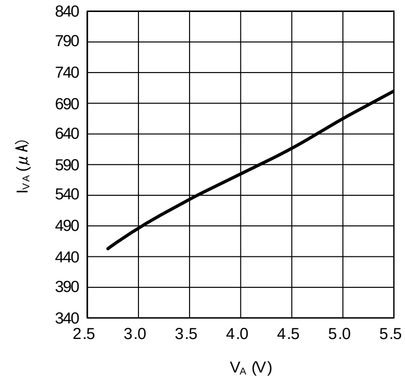


Figure 26. V_A Current vs V_A

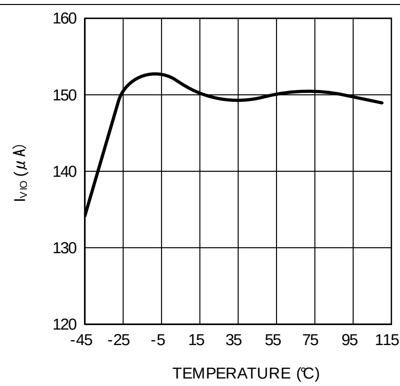


Figure 27. V_{IO} Current vs Temperature

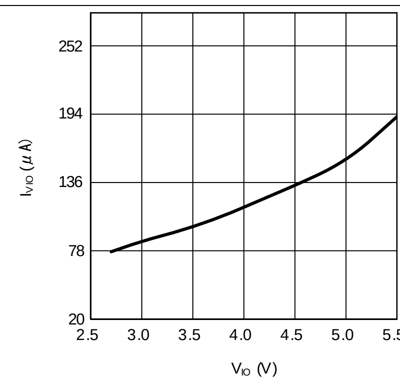


Figure 28. V_{IO} Current vs V_{IO}

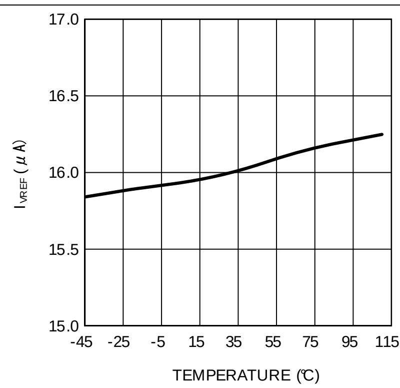


Figure 29. V_{REF} Current vs Temperature

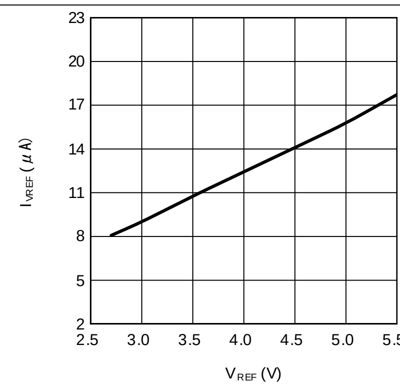


Figure 30. V_{REF} Current vs V_{REF}

7 Detailed Description

7.1 Overview

The ADC141S628Q is a 14-bit, 200-kSPS, sampling analog-to-digital converter (ADC). The converter uses a successive-approximation register (SAR) architecture based upon capacitive redistribution containing an inherent sample-and-hold function. The pseudo-differential nature of the analog inputs is maintained from the internal sample-and-hold circuits throughout the ADC to provide excellent common-mode signal rejection.

The ADC141S628Q operates from independent analog and digital supplies. The analog supply (V_A) can range from 4.5 V to 5.5 V and the digital input/output supply (V_{IO}) can range from 4.5 V to 5.5 V. The ADC141S628Q uses an external reference (V_{REF}), which can be any voltage between 1 V and V_A. The value of V_{REF} determines the range of the analog input, while the reference input current (I_{REF}) depends upon the conversion rate.

The analog input is presented across the two input pins: +IN and –IN. The –IN pin is connected to the sensor ground in order to reject any small ground noise that is common to the +IN and –IN. Upon initiation of a conversion, the differential input is sampled on the internal capacitor array. The inputs are disconnected from the internal circuitry while a conversion is in progress. The ADC141S628Q features a zero-power track mode where the ADC is consuming the minimum amount of supply current while the internal sampling capacitor is tracking the applied analog input voltage. Zero-power track mode starts after the 16th falling edge of the serial clock.

The ADC141S628Q communicates with other devices via a serial peripheral interface (SPI) that operates using three pins: chip-select bar ($\overline{CS}$), serial clock (SCLK), and serial data out (D_{OUT}). The external SCLK controls data transfer and serves as the conversion clock. The duty cycle of SCLK is essentially unimportant, provided the minimum clock high and low times are met. The minimum SCLK frequency is set by internal capacitor leakage. Each conversion requires 18 SCLK cycles to complete. If less than 14 bits of conversion data are required, $\overline{CS}$ can be brought high at any point during the conversion. This procedure of terminating a conversion prior to completion is commonly referred to as short cycling.

The digital conversion result is clocked out by the SCLK input and is provided serially, most significant bit (MSB) first, at the D_{OUT} pin. The digital data that is provided at the D_{OUT} pin is that of the conversion currently in progress and thus there is no pipe line delay.

7.2 Feature Description

7.2.1 Reference Input (V_{REF})

The externally supplied reference voltage (V_{REF}) sets the analog input range. The ADC141S628Q will operate with V_{REF} in the range of 1 V to V_A.

Operation with V_{REF} below 1 V is also possible with slightly diminished performance. As V_{REF} is reduced, the range of acceptable analog input voltages is reduced. The peak-to-peak input range is limited to (V_{REF}).

Reducing V_{REF} also reduces the size of the least significant bit (LSB). The size of one LSB is equal to [(V_{REF}) / 2n], where n is 14. When the LSB size goes below the noise floor of the ADC141S628Q, the noise spans an increasing number of codes and overall performance suffers. For example, the SNR from dynamic signals degrades, while code uncertainty increases in DC measurements. Because the noise is Gaussian in nature, the effects of this noise can be reduced by averaging the results of a number of consecutive conversions.

Additionally, because offset and gain errors are specified in LSB, any offset or gain errors inherent in the ADC increase in terms of LSB size as V_{REF} is reduced.

V_{REF} and analog inputs (+IN and –IN) are connected to the capacitor array through a switch matrix when the input is sampled. Hence, I_{REF}, I_{+IN}, and $I_{–IN}$ are a series of transient spikes that occur at a frequency dependent on the operating sample rate of the ADC141S628Q.

I_{REF} changes only slightly with temperature. See Figure 29 for additional details.

Feature Description (continued)

7.2.2 Analog Signal Inputs

The ADC141S628Q has a pseudo-differential input where the effective input voltage that is digitized is (+IN) – (–IN) and –IN is restricted to be close to ground. By using this differential input, small signals common to both inputs are rejected. As shown in Figure 31, noise is rejected well at low frequencies where the common-mode rejection ratio (CMRR) is 90 dB. As the frequency increases to 1 MHz, the CMRR rolls off to 40 dB.

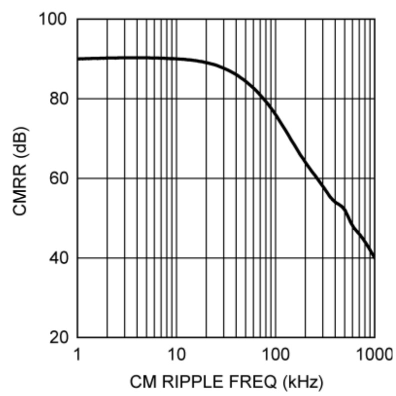


Figure 31. Analog Input CMRR vs Frequency

The current required to recharge the input sampling capacitor causes voltage spikes at +IN and –IN. Do not try to filter out these noise spikes. Rather, ensure that the transients settle out during the acquisition period.

7.2.3 Pseudo-Differential Operation

For pseudo-differential operation, the noninverting input (+IN) of the ADC141S628Q can be driven with a signal that goes from GND to a voltage equal to or less than V_{REF}. Connect the inverting input (–IN) to either the local GND or the remote sensor ground. This connection allows +IN a maximum swing range of ground to V_{REF}. Figure 32 shows the ADC141S628Q being driven by a full-scale single-ended source.

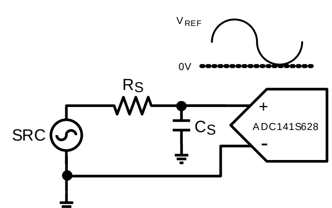


Figure 32. Single-Ended Input

Feature Description (continued)

7.2.4 Serial Digital Interface

The ADC141S628Q communicates via a synchronous 3-wire serial interface as described in Figure 1 or re-shown in Figure 33 for convenience. $\overline{CS}$, chip-select bar, initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. D_{OUT} is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first.

A serial frame is initiated on the falling edge of $\overline{CS}$ and ends on the rising edge of $\overline{CS}$. The ADC141S628Q D_{OUT} pin is in a high-impedance state when $\overline{CS}$ is high and is active when $\overline{CS}$ is low; thus, $\overline{CS}$ acts as an output enable.

The ADC141S628Q samples the input upon the assertion of $\overline{CS}$. Assertion is defined as bringing the $\overline{CS}$ pin to a logic low state. For the first 15 periods of the SCLK following the assertion of $\overline{CS}$, the ADC141S628Q is converting the analog input voltage. On the 16th falling edge of SCLK, the ADC141S628Q enters acquisition (t_{ACQ}) mode. For the next three periods of SCLK, the ADC141S628Q is operating in acquisition mode where the ADC input is tracking the analog input signal applied across +IN and –IN. During acquisition mode, the ADC141S628Q is consuming a minimal amount of power.

The ADC141S628Q can enter conversion mode (t_{CONV}) under three different conditions. The first condition involves $\overline{CS}$ going low (asserted) with SCLK high. In this case, the ADC141S628Q enters conversion mode on the first falling edge of SCLK after $\overline{CS}$ is asserted. In the second condition, $\overline{CS}$ goes low with SCLK low. Under this condition, the ADC141S628Q automatically enters conversion mode and the falling edge of $\overline{CS}$ is seen as the first falling edge of SCLK. In the third condition, $\overline{CS}$ and SCLK go low simultaneously and the ADC141S628Q enters conversion mode. While there is no timing restriction with respect to the falling edges of $\overline{CS}$ and SCLK, there is a minimum and maximum setup time requirements for the falling edge of $\overline{CS}$ with respect to the rising edge of SCLK. See Figure 5 for more information.

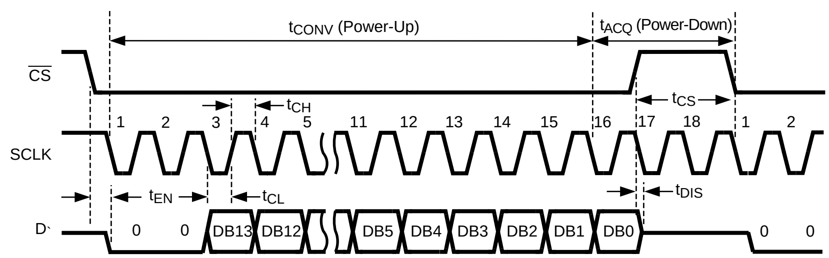


Figure 33. ADC141S628Q Single Conversion Timing Diagram

7.2.5 $\overline{CS}$ Input

The $\overline{CS}$ (chip-select bar) input is active low and is TTL- and CMOS-compatible. The ADC141S628Q enters conversion mode when $\overline{CS}$ is asserted and the SCLK pin is in a logic low state. When $\overline{CS}$ is high, the ADC141S628Q is always in acquisition mode and thus consuming the minimum amount of power. Because $\overline{CS}$ must be asserted to begin a conversion, the sample rate of the ADC141S628Q is equal to the assertion rate of $\overline{CS}$.

Proper operation requires that the fall of $\overline{CS}$ not occur simultaneously with a rising edge of SCLK. If the fall of $\overline{CS}$ occurs during the rising edge of SCLK, the data may be clocked out one bit early. Whether or not the data are clocked out early depends upon how close the $\overline{CS}$ transition is to the SCLK transition, the device temperature, and the characteristics of the individual device. To ensure that the MSB is always clocked out at a given time (the third falling edge of SCLK), the fall of $\overline{CS}$ must always meet the timing requirement specified in the *ADC141S628Q Timing Requirements* table.

7.2.6 SCLK Input

The SCLK (serial clock) is used as the conversion clock to shift out the conversion result. SCLK is TTL- and CMOS-compatible. Internal settling time requirements limit the maximum clock frequency while internal capacitor leakage limits the minimum clock frequency. The ADC141S628Q offers specified performance with the clock rates indicated in the *ADC141S628Q Converter Electrical Characteristics* table.

Feature Description (continued)

The ADC141S628Q enters acquisition mode on the 16th falling edge of SCLK during a conversion frame. Assuming that the LSB is clocked into a controller on the 16th rising edge of SCLK, there is a minimum acquisition time period that must be met before a new conversion frame can begin. Other than the 16th rising edge of SCLK that was used to latch the LSB into a controller, there is no requirement for the SCLK to transition during acquisition mode. Therefore, SCLK can be idle after the LSB is latched into the controller.

7.2.7 Data Output

The data output format of the ADC141S628Q is straight binary, as shown in Figure 34. This figure indicates the ideal output code for a given input voltage and does not include the effects of offset, gain error, linearity errors, or noise. Each data output bit is output on the falling edges of SCLK. The first and second SCLK falling edges clock out leading zeros while the third to 16th SCLK falling edges clock out the conversion result, MSB first.

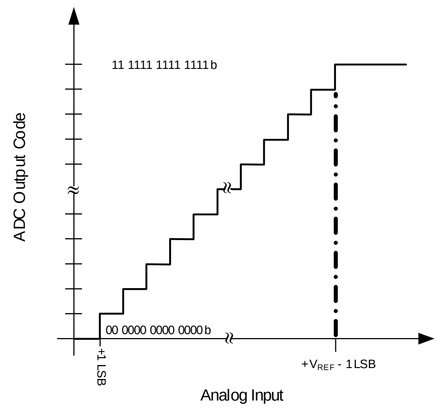


Figure 34. ADC Output vs Input

While most receiving systems capture the digital output bits on the rising edges of SCLK, the falling edges of SCLK may be used to capture the conversion result if the minimum hold time for D_{OUT} is acceptable. See Figure 4 for D_{OUT} hold (t_{DH}) and access (t_{DA}) times.

D_{OUT} is enabled on the falling edge of $\overline{CS}$ and disabled on the rising edge of $\overline{CS}$. If $\overline{CS}$ is raised prior to the 16th falling edge of SCLK, the current conversion is aborted and D_{OUT} goes into its high impedance state. A new conversion begins when $\overline{CS}$ is driven LOW.

7.3 Device Functional Modes

7.3.1 Power Consumption

The architecture, design, and fabrication process allow the ADC141S628Q to operate at conversion rates up to 200 kSPS while consuming very little power. The ADC141S628Q consumes the least amount of power while operating in acquisition (power-down) mode. For applications where power consumption is critical, operate the ADC141S628Q in acquisition mode as often as the application tolerates. To further reduce power consumption, stop the SCLK while $\overline{CS}$ is high.

7.3.1.1 Short Cycling

Short cycling refers to the process of halting a conversion after the last needed bit is outputted. Short cycling can be used to lower the power consumption in those applications that do not need a full 14-bit resolution, or where an analog signal is being monitored until some condition occurs. In some circumstances, the conversion can be terminated after the first few bits. This termination lowers power consumption in the converter because the ADC141S628Q spends more time in acquisition mode and less time in conversion mode.

Short cycling is accomplished by pulling $\overline{CS}$ high after the last required bit is received from the ADC141S628Q output. This cycling is possible because the ADC141S628Q places the latest converted data bit on D_{OUT} as the bit is generated. If only 10-bits of the conversion result are needed, for example, the conversion can be terminated by pulling $\overline{CS}$ high after the 10th bit has been clocked out.

Device Functional Modes (continued)

7.3.1.2 Burst Mode Operation

Normal operation of the ADC141S628Q requires the SCLK frequency to be 18 times the sample rate and the $\overline{CS}$ rate to be the same as the sample rate. However, in order to minimize power consumption in applications requiring sample rates below 200 kSPS, run the ADC141S628Q with an SCLK frequency of 3.6 MHz and a $\overline{CS}$ rate as slow as the system requires. When this set up is accomplished, the ADC141S628Q operates in burst mode. The ADC141S628Q enters into acquisition mode at the end of each conversion, minimizing power consumption, which causes the converter to spend the longest possible time in acquisition mode. Because power consumption scales directly with conversion rate, minimizing power consumption requires determining the lowest conversion rate that will satisfy the requirements of the system.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Application Circuits

The following figure is an example of the ADC141S628Q in a typical application circuit. This circuit is basic and generally requires modification for specific circumstances.

8.1.1.1 Data Acquisition

Figure 35 shows a typical connection diagram for the ADC141S628Q operating at V_A of 5 V. V_{REF} is connected to a 4.1-V shunt reference, the LM4040-4.1, to define the analog input range of the ADC141S628Q independent of supply variation on the 5-V supply line. Decouple the V_{REF} pin to the ground plane by a 0.1-µF ceramic capacitor and a tantalum capacitor of 10 µF. The 0.1-µF capacitor must be placed as close as possible to the V_{REF} pin while the placement of the tantalum capacitor is less critical. The V_A and V_{IO} pins of the ADC141S628Q are also recommended to be decoupled to ground by a 0.1-µF ceramic capacitor in parallel with a 10-µF tantalum capacitor.

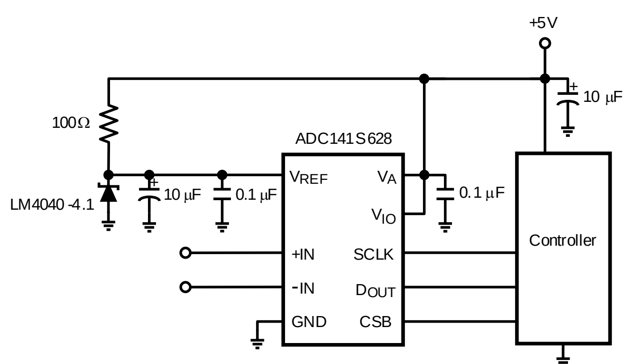


Figure 35. Low-Cost, Low-Power Data Acquisition System

9 Power Supply Recommendations

9.1 Analog and Digital Power Supplies

Any ADC architecture is sensitive to spikes on the power supply, reference, and ground pins. These spikes may originate from switching power supplies, digital logic, high power devices, and other sources. Power to the ADC141S628Q must be clean and well bypassed. Use a 0.1-µF ceramic bypass capacitor and a 1-µF to 10-µF capacitor to bypass the ADC141S628Q supply, with the 0.1-µF capacitor placed as close to the ADC141S628Q package as possible.

Because the ADC141S628Q has both the V_A and V_{IO} pins, the user has three options on how to connect these pins. The first option is to tie V_A and V_{IO} together and power them with the same power supply. This connection is the most cost effective way of powering the ADC141S628Q but is also the least ideal. As stated previously, noise from V_{IO} can couple into V_A and adversely affect performance. The other two options involve the user powering V_A and V_{IO} with separate supply voltages. These supply voltages can have the same amplitude or they can be different. These voltages may be set independent of each other and can be any value between 4.5 V and 5.5 V.

Best performance is typically achieved with V_A operating at 5 V. Operating V_A at 5 V offers the best linearity and dynamic performance when V_{REF} is also set to 5 V.

9.2 Voltage Reference

The reference source must have a low output impedance and must be bypassed with a minimum capacitor value of 0.1 µF. A larger capacitor value of 1 µF to 10 µF placed in parallel with the 0.1-µF capacitor is preferred. While the ADC141S628Q draws very little current from the reference on average, there are higher instantaneous current spikes at the reference.

The V_{REF} of the ADC141S628Q, like all ADCs, does not reject noise or voltage variations. Keep this fact in mind if V_{REF} is derived from the power supply. Any noise or ripple from the supply that is not rejected by the external reference circuitry appears in the digital results. The use of an active reference source is recommended. The LM4040 and LM4050 shunt reference families and the LM4132 and LM4140 series reference families are excellent choices for a reference source.

10 Layout

10.1 Layout Guidelines

For best performance, care must be taken with the physical layout of the printed circuit board, which is especially true with a low V_{REF} or when the conversion rate is high. At high clock rates there is less time for settling, so any noise must settle out before the conversion begins.

10.1.1 PCB Layout

Capacitive coupling between the noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry and the clock line as short as possible. Digital circuits create substantial supply and ground current transients. The logic noise generated can have significant impact upon system noise performance. To avoid performance degradation of the ADC141S628Q because of supply noise, avoid using the same supply for the V_A and V_{REF} of the ADC141S628Q that is used for digital circuitry on the board.

Generally, analog and digital lines must cross each other at 90° to avoid crosstalk. However, to maximize accuracy in high resolution systems, avoid crossing analog and digital lines altogether. Clock lines must be kept as short as possible and isolated from all other lines, including other digital lines. In addition, the clock line must also be treated as a transmission line and be properly terminated. Isolate the analog input from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (for example, a filter capacitor) connected between the converter input pins and ground or to the reference input pin and ground must be connected to a very clean point in the ground plane.

A single, uniform ground plane and the use of split power planes are recommended. Place the power planes within the same board layer. All analog circuitry (input amplifiers, filters, reference components, and so forth) must be placed over the analog power plane. Place all digital circuitry over the digital power plane. Furthermore, the GND pins on the ADC141S628Q and all the components in the reference circuitry and input signal chain that are connected to ground must be connected to the ground plane at a quiet point. Avoid connecting these points too close to the ground point of a microprocessor, microcontroller, digital signal processor, or other high power digital device.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

11.1.1.1 Specification Definitions

APERTURE DELAY is the time between the first falling edge of SCLK and the time when the input signal is sampled for conversion.

COMMON-MODE REJECTION RATIO (CMRR) is a measure of how well in-phase signals common to both input pins are rejected.

To calculate CMRR, the change in output offset is measured while the common mode input voltage is changed from 2 V to 3 V.

$$CMRR = 20\ LOG\ (\ \Delta\ Common\ Input\ /\ \Delta\ Output\ Offset) \quad (1)$$

CONVERSION TIME is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word.

DIFFERENTIAL NONLINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying signal-to-noise and distortion or SINAD. ENOB is defined as (SINAD − 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full-scale input.

FULL-SCALE ERROR is the difference between the input voltage at which the output code transitions to positive full-scale and V_{REF} minus 1 LSB.

GAIN ERROR is the deviation from the ideal slope of the transfer function. Gain error is the difference between positive full-scale error and negative full-scale error and can be calculated as:

$$Gain\ Error = Positive\ Full\text{-}Scale\ Error - Negative\ Full\text{-}Scale\ Error \quad (2)$$

INTEGRAL NONLINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from ½ LSB below the first code transition through ½ LSB above the last code transition. The deviation of any given code from this straight line is measured from the center of that code value.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC141S628Q is specified not to have any missing codes.

OFFSET ERROR is the difference between the input voltage at which the output code transitions from code 0000h to 0001h and 1 LSB.

POST CALIBRATION TOTAL UNADJUSTED ERROR is the total unadjusted error over the temperature range after system calibration to remove gain and offset errors at 25°C.

POWER-SUPPLY REJECTION RATIO (PSRR) is a measure of how well a change in the analog supply voltage is rejected. PSRR is calculated from the ratio of the change in offset error for a given change in supply voltage, expressed in dB. For the ADC141S628Q, V_A is changed from 4.5 V to 5.5 V.

$$PSRR = 20\ LOG\ (\Delta\ Output\ Offset\ /\ \Delta\ V_A) \quad (3)$$

SIGNAL-TO-NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below one-half the sampling frequency, including harmonics but excluding DC.

Device Support (continued)

SPURIOUS-FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the desired signal amplitude to the amplitude of the peak spurious spectral component below one-half the sampling frequency, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

TOTAL HARMONIC DISTORTION (THD) is the ratio of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output, expressed in dB. THD is calculated as:

$$THD = 20 \cdot \log_{10} \sqrt{\frac{A_{f2}^2 + \cdots + A_{f6}^2}{A_{f1}^2}}$$

where

- A_{f1} is the RMS power of the input frequency at the output
- A_{f2} through A_{f6} are the RMS power in the first five harmonic frequencies (4)

TOTAL UNADJUSTED ERROR is the difference between the parts transfer function and the ideal transfer function.

THROUGHPUT TIME is the minimum time required between the start of two successive conversion.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *LM4040xxx Precision Micropower Shunt Voltage Reference*
- *LM4050-N/-Q1 Precision Micropower Shunt Voltage Reference*
- *LM4132, LM4132-Q1 SOT-23 Precision Low Dropout Voltage Reference*
- *LM4140 High Precision Low Noise Low Dropout Voltage Reference*
- *Absolute Maximum Ratings for Soldering*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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