DS10CP154A 1.5 Gbps 4x4 LVDS Crosspoint Switch

Check for Samples: DS10CP154A

FEATURES

- **DC - 1.5 Gbps Low Jitter, Low Skew, Low Power Operation**
- **Pin and SMBus Configurable, Fully Differential, Non-Blocking Architecture**
- **Wide Input Common Mode Range Enables DC Coupled Interface to CML or LVPECL Drivers**
- **$\overline{\text{LOS}}$ Circuitry Detects Open Inputs Fault Condition**
- **On-chip 100 Ω Input and Output Termination Minimizes Insertion and Return Losses, Reduces Component Count and Minimizes Board Space**
- **8 kV ESD on LVDS I/O Pins Protects Adjoining Components**
- **Small 6 mm x 6 mm WQFN-40 Space Saving Package**

APPLICATIONS

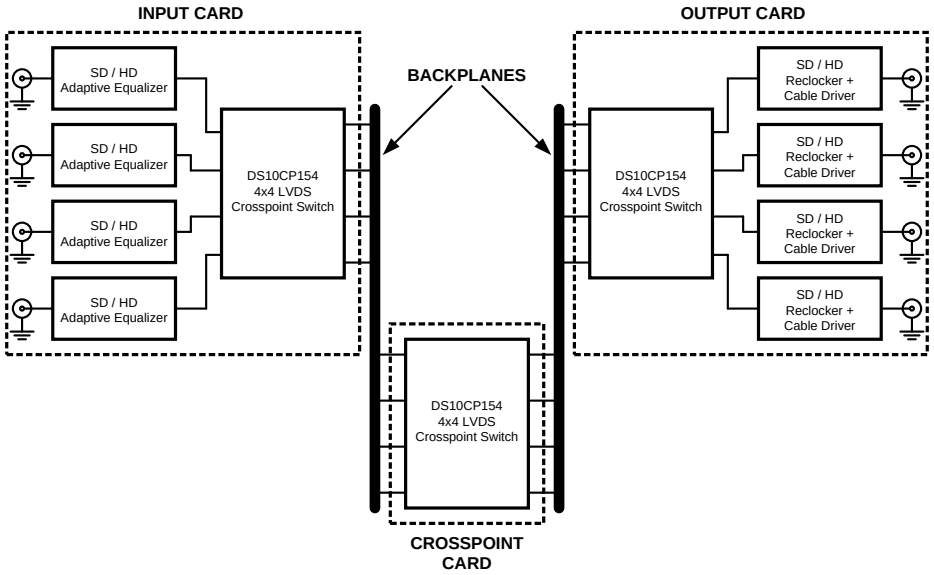
- **High-speed Channel Select Applications**
- **Clock and Data Buffering and Muxing**
- **SD / HD SDI Routers**

DESCRIPTION

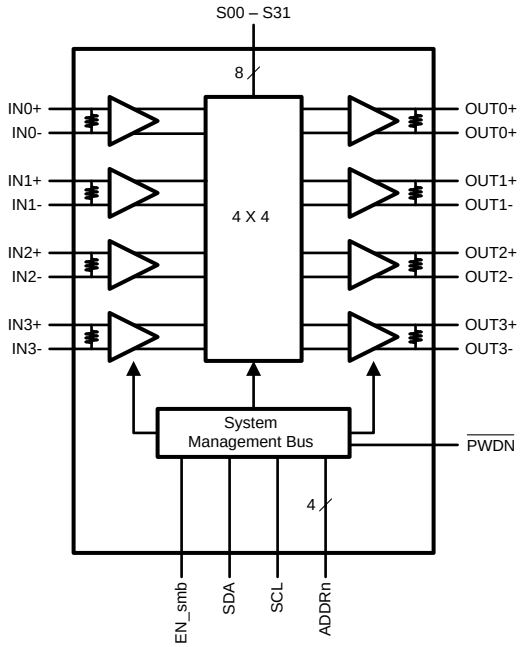
The DS10CP154A is a 1.5 Gbps 4x4 LVDS crosspoint switch optimized for high-speed signal routing and switching over FR-4 printed circuit board backplanes and balanced cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity. The non-blocking architecture allows connections of any input to any output or outputs. The switch configuration can be accomplished via external pins or the System Management Bus (SMBus) interface. In addition, the SMBus circuitry enables the loss of signal ($\overline{\text{LOS}}$) monitors that can inform a system of the presence of an open inputs condition (e.g. disconnected cable).

Wide input common mode range allows the switch to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires a minimal space on the board while the flow-through pinout allows easy board layout. Each differential input and output is internally terminated with a 100Ω resistor to lower return losses, reduce component count and further minimize board space.

Typical Application



Block Diagram



Connection Diagram

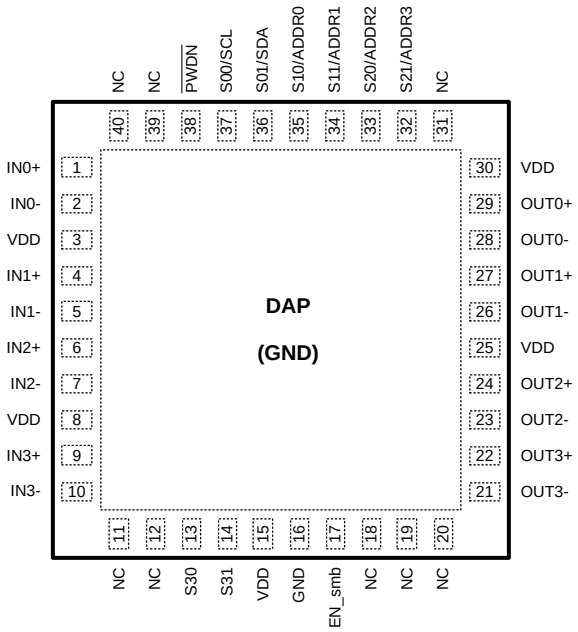


Figure 1. WQFN Package
See Package Number RTA0040A

PIN DESCRIPTIONS

Pin Name	Pin Number	I/O, Type	Pin Description
IN0+, IN0- , IN1+, IN1-, IN2+, IN2-, IN3+, IN3-	1, 2, 4, 5, 6, 7, 9, 10	I, LVDS	Inverting and non-inverting high speed LVDS input pins.
OUT0+, OUT0-, OUT1+, OUT1-, OUT2+, OUT2-, OUT3+, OUT3-	29, 28, 27, 26, 24, 23, 22, 21	O, LVDS	Inverting and non-inverting high speed LVDS output pins.
EN_smb	17	I, LVCMOS	System Management Bus (SMBus) mode enable pin. The pin has an internal 20k pull down. When the pin is set to a [1], the device is in the SMBus mode. All SMBus registers are reset when the pin is toggled.
S00/SCL, S01/SDA	37, 36	I/O, LVCMOS	For EN_smb = [0], these pins select which LVDS input is routed to the OUT0. In the SMBus mode, when the EN_smb = [1], these pins are the SMBus clock input and data I/O pins respectively.
S10/ADDR0, S11/ADDR1	35, 34	I/O, LVCMOS	For EN_smb = [0], these pins select which LVDS input is routed to the OUT1. In the SMBus mode, when the EN_smb = [1], these pins are the User-Set SMBus Slave Address inputs.
S20/ADDR2, S21/ADDR3	33, 32	I/O, LVCMOS	For EN_smb = [0], these pins select which LVDS input is routed to the OUT2. In the SMBus mode, when the EN_smb = [1], these pins are the User-Set SMBus Slave Address inputs.
S30, S31	13, 14	I, LVCMOS	For EN_smb = [0], these pins select which LVDS input is routed to the OUT3. In the SMBus mode, when the EN_smb = [1], these pins are non-functional and should be tied to either logic [0] or [1].
$\overline{\text{PWDN}}$	38	I, LVCMOS	For EN_smb = [0], this is the power down pin. When the $\overline{\text{PWDN}}$ is set to a [0], the device is in the power down mode. The SMBus circuitry can still be accessed provided the EN_smb pin is set to a [1]. In the SMBus mode, the device is powered up by either setting the $\overline{\text{PWDN}}$ pin to [1] **OR** by writing a [1] to the Control Register D[7] bit ($\overline{\text{SoftPWDN}}$). The device will be powered down by setting the $\overline{\text{PWDN}}$ pin to [0] **AND** by writing a [0] to the Control Register D[7] bit ($\overline{\text{SoftPWDN}}$).
NC	11, 12, 18, 19, 20, 31, 39, 40		No connect pins. May be left floating.
VDD	3, 8, 15,25, 30	Power	Power supply pins.
GND	16, DAP	Power	Ground pin and pad (DAP - die attach pad).

Absolute Maximum Ratings[1][2]

Supply Voltage		−0.3V to +4V
LVCMOS Input Voltage		−0.3V to (V_{CC} + 0.3V)
LVCMOS Output Voltage		−0.3V to (V_{CC} + 0.3V)
LVDS Input Voltage		−0.3V to +4V
Differential Input Voltage |VID|		1.0V
LVDS Output Voltage		−0.3V to (V_{CC} + 0.3V)
LVDS Differential Output Voltage		0V to 1.0V
LVDS Output Short Circuit Current Duration		5 ms
Junction Temperature		+150°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature Range	Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	RTA0040A Package	4.65W
	Derate RTA0040A Package	37.2 mW/°C above +25°C
Package Thermal Resistance	θ_{JA}	+26.9°C/W
	θ_{JC}	+3.8°C/W
ESD Susceptibility	HBM[3]	≥8 kV
	MM[4]	≥250V
	CDM[5]	≥1250V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. JESD22-A114C
(4) Machine Model, applicable std. JESD22-A115-A
(5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Receiver Differential Input Voltage (V_{ID})	0		1.0	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C
SMBus (SDA, SCL)			3.6	V

Electrical Characteristics[1][2][3]

Over recommended operating supply and temperature ranges unless otherwise specified.

Parameter		Test Conditions		Min	Typ	Max	Units
LVCMOS DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IH}	High Level Input Current	V_{IN} = 3.6V, V_{CC} = 3.6V			0	±10	µA
			EN_smb pin	40	175	250	µA
I_{IL}	Low Level Input Current	V_{IN} = GND, V_{CC} = 3.6V			0	±10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA, V_{CC} = 0V			−0.9	−1.5	V
V_{OL}	Low Level Output Voltage	I_{OL}= 4 mA	SDA pin			0.4	V

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.
(3) Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.

Electrical Characteristics[1][2][3] (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Parameter		Test Conditions	Min	Typ	Max	Units
LVDS INPUT DC SPECIFICATIONS						
V_{ID}	Input Differential Voltage		0		1	V
V_{TH}	Differential Input High Threshold	V_{CM} = +0.05V or V_{CC}-0.05V		0	+100	mV
V_{TL}	Differential Input Low Threshold		−100	0		mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 100 mV	0.05		V_{CC} - 0.05	V
I_{IN}	Input Current	V_{IN} = 3.6V or 0V V_{CC} = 3.6V or 0V		±1	±10	µA
C_{IN}	Input Capacitance	Any LVDS Input Pin to GND		1.7		pF
R_{IN}	Input Termination Resistor	Between IN+ and IN-		100		Ω
LVDS OUTPUT DC SPECIFICATIONS						
V_{OD}	Differential Output Voltage	R_L = 100Ω	250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States		-35		35	mV
V_{OS}	Offset Voltage	R_L = 100Ω	1.05	1.2	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States		-35		35	mV
I_{OS}	Output Short Circuit Current[4]	OUT to GND		-25	-55	mA
		OUT to V_{CC}		7	55	mA
C_{OUT}	Output Capacitance	Any LVDS Output Pin to GND		1.2		pF
R_{OUT}	Output Termination Resistor	Between OUT+ and OUT-		100		Ω
SUPPLY CURRENT						
I_{CC1}	Supply Current	$\overline{PWDN}$ = 0		40	50	mA
I_{CC2}	Supply Current	$\overline{PWDN}$ = 1; Broadcast Mode (1:4)		103	125	mA
I_{CC3}	Supply Current	$\overline{PWDN}$ = 1; Quad Buffer Mode (4:4)		115	140	mA

(4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

AC Electrical Characteristics[1][2]

Over recommended operating supply and temperature ranges unless otherwise specified.

Parameter		Test Conditions	Min	Typ	Max	Units
LVDS OUTPUT AC SPECIFICATIONS[3]						
t_{PLHD}	Differential Propagation Delay Low to High	R_L = 100Ω		500	675	ps
t_{PHLD}	Differential Propagation Delay High to Low			460	675	ps
t_{SKD1}	Pulse Skew $\lvert t_{PLHD} - t_{PHLD} \rvert$[4]			40	100	ps
t_{SKD2}	Channel to Channel Skew[5]			40	125	ps
t_{SKD3}	Part to Part Skew[6]			50	225	ps
t_{LHT}	Rise Time	R_L = 100Ω		145	350	ps
t_{HLT}	Fall Time			145	350	ps

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(3) Specification is ensured by characterization and is not tested in production.
(4) t_{SKD1}, $\lvert t_{PLHD} - t_{PHLD} \rvert$, Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(5) t_{SKD2}, Channel to Channel Skew, is the difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels in Broadcast mode (any one input to all outputs).
(6) t_{SKD3}, Part to Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

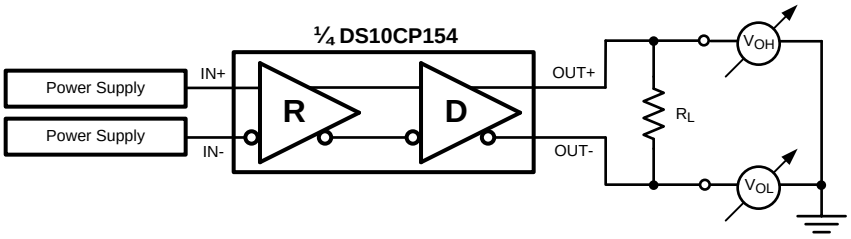
AC Electrical Characteristics[1][2] (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

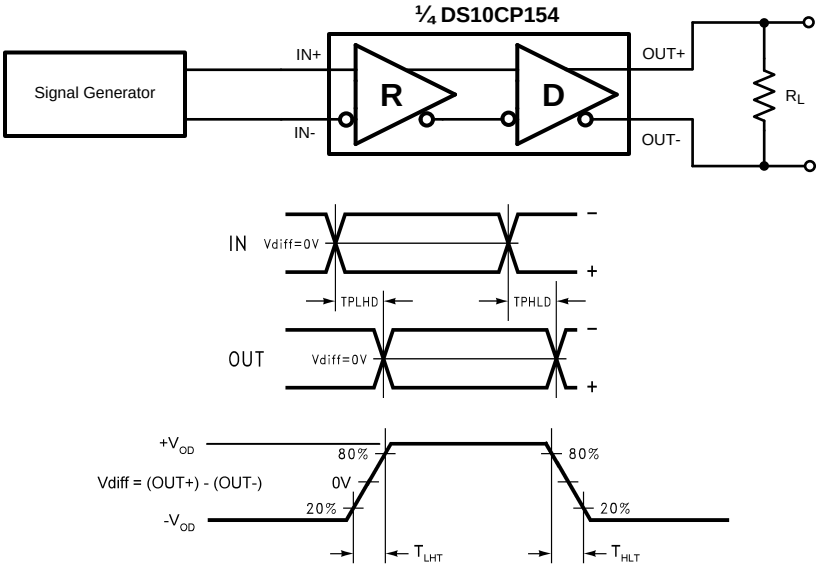
Parameter		Test Conditions		Min	Typ	Max	Units
t_{ON}	Power Up Time	Time from $\overline{PWDN}$ = LH to OUTn active			7	20	µs
t_{OFF}	Power Down Time	Time from $\overline{PWDN}$ = HL to OUTn inactive			6	25	ns
t_{SEL}	Select Time	Time from Sn = LH or HL to new signal at OUTn			8	12	ns
JITTER PERFORMANCE[3]							
t_{RJ1}	Random Jitter (RMS Value)[7]	V_{ID} = 350 mV, V_{CM} = 1.2V, Clock (RZ)	135 MHz		1	2.0	ps
t_{RJ2}			311 MHz		0.5	1.2	ps
t_{RJ3}			503 MHz		0.5	1.0	ps
t_{RJ4}			750 MHz		0.5	1.0	ps
t_{DJ1}	Deterministic Jitter (Peak to Peak Value)[8]	V_{ID} = 350 mV, V_{CM} = 1.2V, K28.5 (NRZ)	270 Mbps		7	30	ps
t_{DJ2}			622 Mbps		12	26	ps
t_{DJ3}			1.06 Gbps		9	24	ps
t_{DJ4}			1.5 Gbps		12	28	ps
t_{TJ1}	Total Jitter (Peak to Peak Value)[9]	V_{ID} = 350 mV, V_{CM} = 1.2V, PRBS-23 (NRZ)	270 mbps		0.008	0.036	UI_{P-P}
t_{TJ2}			622 Mbps		0.007	0.043	UI_{P-P}
t_{TJ3}			1.06Gbps		0.008	0.064	UI_{P-P}
t_{TJ4}			1.5 Gbps		0.007	0.072	UI_{P-P}
SMBus AC SPECIFICATIONS							
f_{SMB}	SMBus Operating Frequency			10		100	kHz
t_{BUF}	Bus free time between Stop and Start Conditions			4.7			µs
$t_{HD:SDA}$	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.			4.0			µs
$t_{SU:SDA}$	Repeated Start Condition setup time.			4.7			µs
$t_{SU:SDO}$	Stop Condition setup time			4.0			µs
$t_{HD:DAT}$	Data hold time			300			ns
$t_{SU:DAT}$	Data setup time			250			ns
$t_{TIMEOUT}$	Detect clock low timeout			25		35	ms
t_{LOW}	Clock low period			4.7			µs
t_{HIGH}	Clock high period			4.0		50	µs
t_{POR}	Time in which a device must be operational after power-on reset					500	ms

(7) Measured on a clock edge with a histogram and an accumulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.
(8) Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.
(9) Measured on an eye diagram with a histogram and an accumulation of 3500 histogram hits. Input stimulus jitter is subtracted.

DC Test Circuits



AC Test Circuits and Timing Diagrams



FUNCTIONAL DESCRIPTION

The DS10CP154A is a 1.5 Gbps 4x4 LVDS digital crosspoint switch optimized for high-speed signal routing and switching over lossy FR-4 printed circuit board backplanes and balanced cables. The DS10CP154A operates in two modes: Pin Mode (EN_smb = 0) and SMBus Mode (EN_smb = 1).

When in the Pin Mode, the switch is fully configurable with external pins. This is possible with two input select pins per output (e.g. S00 and S01 pins for OUT0).

In the Pin Mode, feedback from the $\overline{\text{LOS}}$ (**L**oss **O**f **S**ignal) monitor circuitry is not available (there is not an $\overline{\text{LOS}}$ output pin).

When in the SMBus Mode, the full switch configuration and $\overline{\text{SoftPWDN}}$ can be programmed via the SMBus interface. In addition, by using the SMBus interface, a user can obtain the feedback from the built-in $\overline{\text{LOS}}$ circuitry which detects an open inputs fault condition.

In the SMBus Mode, the S00 and S01 pins become SMBus clock (SCL) input and data (SDA) input pins respectively; the S10, S11, S21 and S21 pins become the User-Set SMBus Slave Address input pins (ADDR0, 1, 2 and 3) while the S30 and S31 pins become non-functional (tieing these two pins to either H or L is recommended if the device will function only in the SMBus mode).

In the SMBus Mode, the $\overline{\text{PWDN}}$ pin remains functional. How this pin functions in each mode is detailed in the following sections.

DS10CP154A OPERATION IN THE PIN MODE

Power Up

In the Pin Mode, when the power is applied to the device power suppy pins, the DS10CP154A enters the Power Up mode when the PWDN pin is set to logic H. When in the Power Down mode (PWDN pin is set to logic L), all circuitry is shut down except the minimum required circuitry for the LOS and SMBus Slave operation.

Switch Configuration

In the Pin Mode, the DS10CP154A operates as a fully pin-configurable crosspoint switch. The following truth tables illustrate how the swich can be configured with external pins.

Switch Configuration Truth Tables

Table 1. Input Select Pins Configuration for the Output OUT0

S01	S00	INPUT SELECTED
0	0	IN0
0	1	IN1
1	0	IN2
1	1	IN3

Table 2. Input Select Pins Configuration for the Output OUT1

S11	S10	INPUT SELECTED
0	0	IN0
0	1	IN1
1	0	IN2
1	1	IN3

Table 3. Input Select Pins Configuration for the Output OUT2

S21	S20	INPUT SELECTED
0	0	IN0
0	1	IN1
1	0	IN2
1	1	IN3

Table 4. Input Select Pins Configuration for the Output OUT3

S31	S30	INPUT SELECTED
0	0	IN0
0	1	IN1
1	0	IN2
1	1	IN3

DS10CP154A OPERATION IN THE SMBUS MODE

The DS10CP154A operates as a slave on the System Management Bus (SMBus) when the EN_smb pin is set to a high (1). Under these conditions, the SCL pin is a clock input while the SDA pin is a serial data input pin.

Device Address

Based on the SMBus 2.0 specification, the DS10CP154A has a 7-bit slave address. The three most significant bits of the slave address are hard wired inside the DS10CP154A and are “101”. The four least significant bits of the address are assigned to pins ADDR3-ADDR0 and are set by connecting these pins to GND for a low (0) or to VCC for a high (1). The complete slave address is shown in the following table:

Table 5. DS10CP154A Slave Address

1	0	1	ADDR3	ADDR2	ADDR1	ADDR0
MSB						LSB

This slave address configuration allows up to sixteen DS10CP154A devices on a single SMBus bus.

Transfer of Data via the SMBus

During normal operation the data on SDA must be stable during the time when SCK is high.

There are three unique states for the SMBus:

START: A HIGH to LOW transition on SDA while SCK is high indicates a message START condition.

STOP: A LOW to HIGH transition on SDA while SCK is high indicates a message STOP condition.

IDLE: If SCK and SDA are both high for a time exceeding tBUF from the last detected STOP condition or if they are high for a total exceeding the maximum specification for tHIGH then the bus will transfer to the IDLE state.

SMBus Transactions

A transaction begins with the host placing the DS10CP154A SMBus into the START condition, then a byte (8 bits) is transferred, MSB first, followed by a ninth ACK bit. ACK bits are ‘0’ to signify an ACK, or ‘1’ to signify NACK, after this the host holds the SCL line low, and waits for the receiver to raise the SDA line as an ACKnowledge that the byte has been received.

Writing to a Register

To write a register, the following protocol is used (see SMBus 2.0 specification):

1) The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.

2) The Device (Slave) drives an ACK bit (“0”).

3) The Host drives the 8-bit Register Address.

4) The Device drives an ACK bit (“0”).

5) The Host drives the 8-bit data byte.

6) The Device drives an ACK bit “0”.

7) The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes Idle and communication with other SMBus devices may now occur.

Reading From a Register

To read a register, the following protocol is used (see SMBus 2.0 specification):

1) The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.

2) The Device (Slave) drives an ACK bit (“0”).

3) The Host drives the 8-bit Register Address.

4) The Device drives an ACK bit (“0”).

5) The Host drives a START condition.

6) The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.

7) The Device drives an ACK bit “0”.

8) The Device drives the 8-bit data value (register contents).

9) The Host drives a NACK bit “1” indicating end of READ transfer.

10) The Host drives a STOP condition.

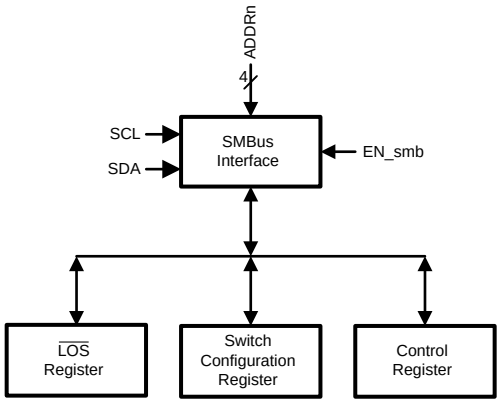
The READ transaction is completed, the bus goes Idle and communication with other SMBus devices may now occur.

REGISTER DESCRIPTIONS

There are three data registers in the DS10CP154A accessible via the SMBus interface.

Table 6. DS10CP154A SMBus Data Registers

Address (hex)	Name	Access	Description
0	Switch Configuration	R/W	Switch Configuration Register
3	Control	R/W	Powerdown, $\overline{\text{LOS}}$ Enable and Pin Control Register
4	$\overline{\text{LOS}}$	RO	**L**oss **O**f **S**ignal ($\overline{\text{LOS}}$) Reporting Register



Switch Configuration Register

The Switch Configuration register is utilized to configure the switch. The following two tables show the Switch Configuration Register mapping and associated truth table.

Bit	Default	Bit Name	Access	Description
D[1:0]	00	Input Select 0	R/W	Selects which input is routed to the OUT0.
D[3:2]	00	Input Select 1	R/W	Selects which input is routed to the OUT1.
D[5:4]	00	Input Select 2	R/W	Selects which input is routed to the OUT2.
D[7:6]	00	Input Select 3	R/W	Selects which input is routed to the OUT3.

Table 7. Switch Configuration Register Truth Table

D1	D0	Input Routed to the OUT0
0	0	IN0
0	1	IN1
1	0	IN2
1	1	IN3

The switch configuration logic has a SmartPWDN circuitry which automatically optimizes the device's power consumption based on the switch configuration (i.e. It places unused I/O blocks and other unused circuitry in the power down state).

Control Register

The Control register enables $\overline{\text{SoftPWDN}}$ control, individual output power down ($\overline{\text{PWDNn}}$) control and $\overline{\text{LOS}}$ Circuitry Enable control via the SMBus. The following table shows the register mapping.

Bit	Default	Bit Name	Access	Description
D[3:0]	1111	$\overline{\text{PWDNn}}$	R/W	Writing a [0] to the bit D[n] will power down the output OUTn when either the $\overline{\text{PWDN}}$ pin OR the Control Register bit D[7] ($\overline{\text{SoftPWDN}}$) is set to a high [1].
D[4]	x	n/a	R/W	Undefined.
D[5]	x	n/a	R/W	Undefined.
D[6]	0	EN_$\overline{\text{LOS}}$	R/W	Writing a [1] to the bit D[6] will enable the $\overline{\text{LOS}}$ circuitry and receivers on all four inputs. The SmartPWDN circuitry will not disable any of the inputs nor any supporting $\overline{\text{LOS}}$ circuitry depending on the switch configuration.
D[7]	0	$\overline{\text{SoftPWDN}}$	R/W	Writing a [0] to the bit D[7] will place the device into the power down mode. This pin is ORed together with the $\overline{\text{PWDN}}$ pin.

Table 8. DS10CP154A Power Modes Truth Table

$\overline{\text{PWDN}}$	$\overline{\text{SoftPWDN}}$	$\overline{\text{PWDNn}}$	DS25CP104 Power Mode
0	0	x	Power Down Mode. In this mode, all circuitry is shut down except the minimum required circuitry for the $\overline{\text{LOS}}$ and SMBus Slave operation. The SMBus circuitry allows enabling the $\overline{\text{LOS}}$ circuitry and receivers on all inputs in this mode by setting the EN_$\overline{\text{LOS}}$ bit to a [1].
0 1 1	1 0 1	x x x	Power Up Mode. In this mode, the SmartPWDN circuitry will automatically power down any unused I/O and logic blocks and other supporting circuitry depending on the switch configuration. An output will be enabled **only** when the SmartPWDN circuitry indicates that that particular output is needed for the particular switch configuration **and** the respective $\overline{\text{PWDNn}}$ bit has logic high [1]. An input will be enabled when the SmartPWDN circuitry indicates that that particular input is needed for the particular switch configuration **or** the EN_$\overline{\text{LOS}}$ bit is set to a [1].

$\overline{\text{LOS}}$ Register

The $\overline{\text{LOS}}$ register reports an open inputs fault condition for each of the inputs. The following table shows the register mapping.

Bit	Default	Bit Name	Access	Description
D[0]	0	$\overline{\text{LOS0}}$	RO	Reading a [0] from the bit D[0] indicates an open inputs fault condition on the IN0. A [1] indicates presence of a valid signal.
D[1]	0	$\overline{\text{LOS1}}$	RO	Reading a [0] from the bit D[1] indicates an open inputs fault condition on the IN1. A [1] indicates presence of a valid signal.
D[2]	0	$\overline{\text{LOS2}}$	RO	Reading a [0] from the bit D[2] indicates an open inputs fault condition on the IN2. A [1] indicates presence of a valid signal.
D[3]	0	$\overline{\text{LOS3}}$	RO	Reading a [0] from the bit D[3] indicates an open inputs fault condition on the IN3. A [1] indicates presence of a valid signal.
D[7:4]	0000	Reserved	RO	Reserved for future use. Returns undefined value when read.

INPUT INTERFACING

The DS10CP154A accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS10CP154A can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the DS10CP154A inputs are internally terminated with a 100Ω resistor.

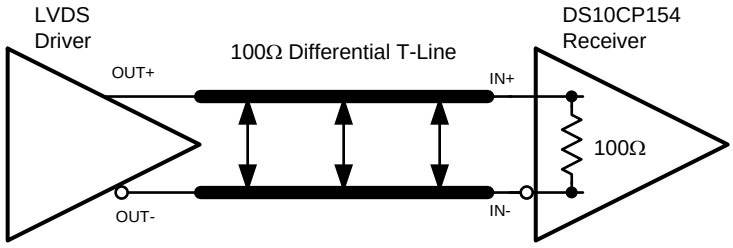


Figure 2. Typical LVDS Driver DC-Coupled Interface to DS10CP154A Input

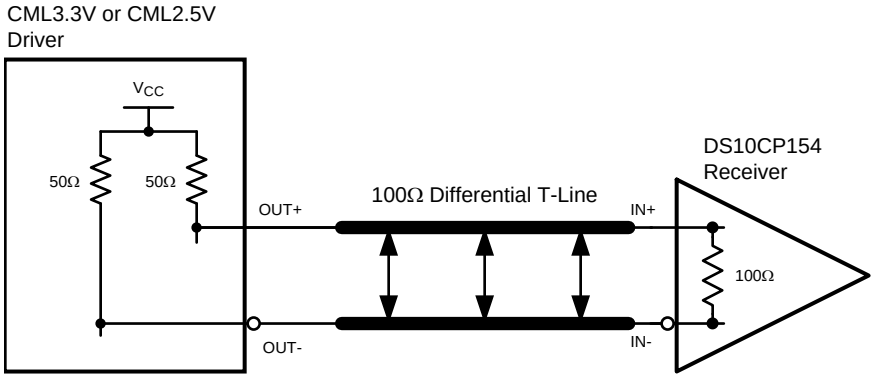


Figure 3. Typical CML Driver DC-Coupled Interface to DS10CP154A Input

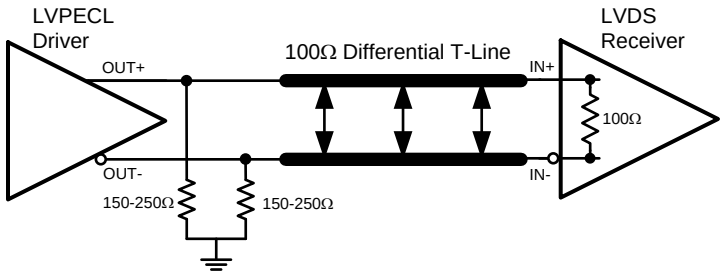


Figure 4. Typical LVPECL Driver DC-Coupled Interface to DS10CP154A Input

OUTPUT INTERFACING

The DS10CP154A outputs signals that are compliant to the LVDS standard. Its outputs can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accomodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.

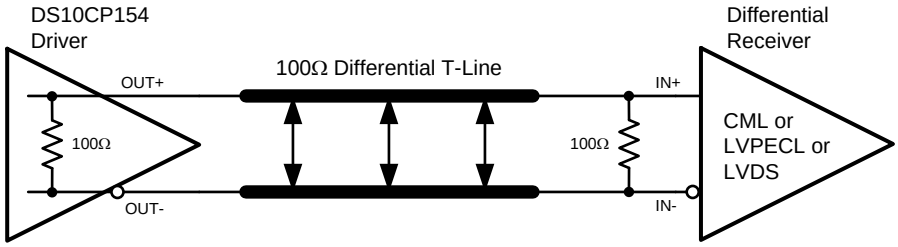


Figure 5. Typical DS10CP154A Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS10CP154ATSQ/NOPB	ACTIVE	WQFN	RTA	40	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	1CP154AS	Samples
DS10CP154ATSQX/NOPB	ACTIVE	WQFN	RTA	40	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	1CP154AS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

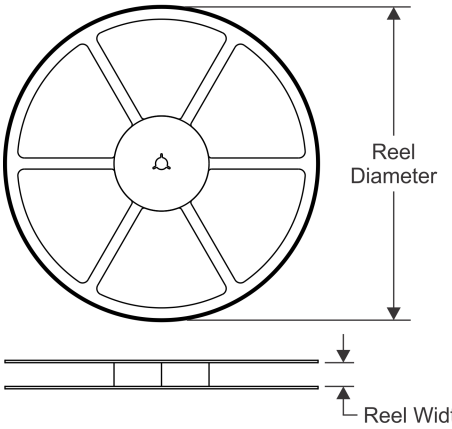
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

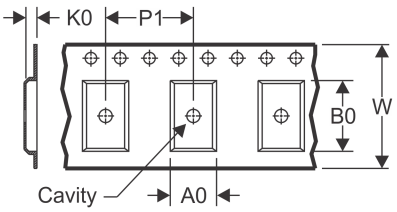
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

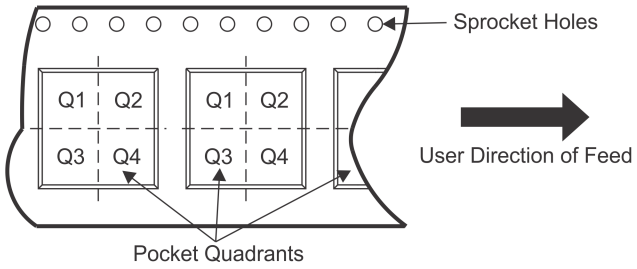


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

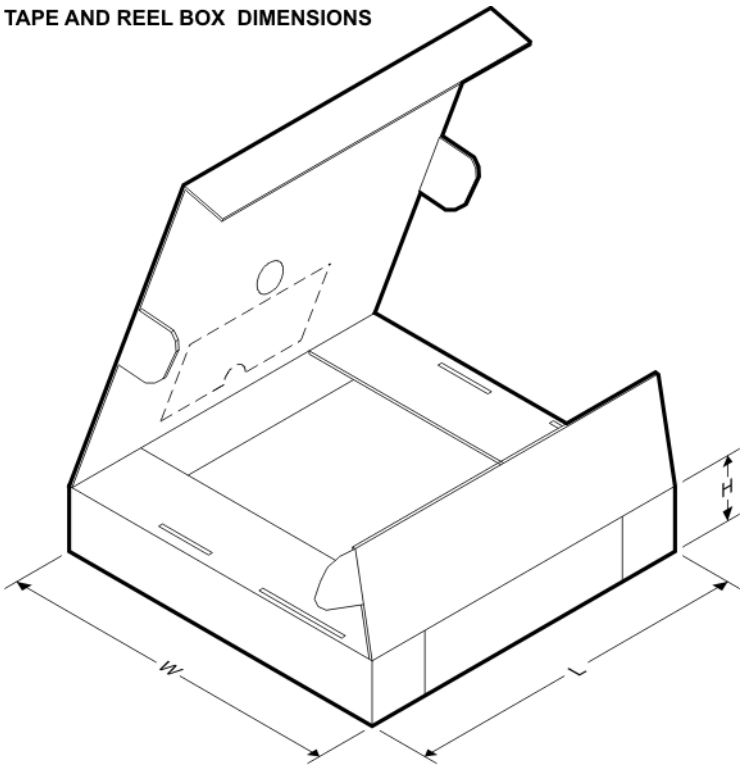
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS10CP154ATSQ/NOPB	WQFN	RTA	40	250	178.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1
DS10CP154ATSQX/NOPB	WQFN	RTA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS10CP154ATSQ/NOPB	WQFN	RTA	40	250	210.0	185.0	35.0
DS10CP154ATSQX/NOPB	WQFN	RTA	40	2500	367.0	367.0	38.0

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