

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Max  $t_{pd}$  of 3 ns at 3.3 V
- $\pm 24$ -mA Output Drive at 3.3 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## DESCRIPTION/ORDERING INFORMATION

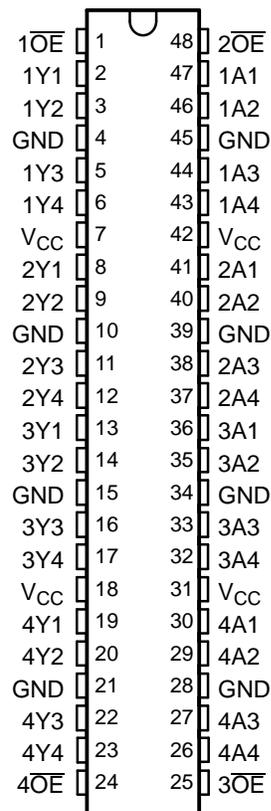
This 16-bit buffer/driver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74ALVC16244A is designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**DGG OR DL PACKAGE  
(TOP VIEW)**



## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	FBGA – GRD	Tape and reel	SN74ALVC16244AGRDR	VC244A
	FBGA – ZRD (Pb-free)		SN74ALVC16244AZRDR	
	SSOP – DL	Tube	SN74ALVC16244ADL	ALVC16244A
		Tape and reel	SN74ALVC16244ADLR	
	TSSOP – DGG	Tape and reel	SN74ALVC16244ADGGR	ALVC16244A
			SN74ALVC16244ADGGRE4	
VFBGA – GQL	Tape and reel	SN74ALVC16244AGQLR	VC244A	
VFBGA – ZQL (Pb-free)		SN74ALVC16244AZQLR		

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



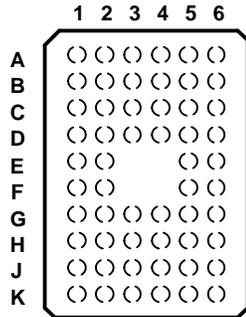
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

**SN74ALVC16244A**  
**16-BIT BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

SCAS2500—JANUARY 1993—REVISED OCTOBER 2005

**GQL OR ZQL PACKAGE**  
**(TOP VIEW)**

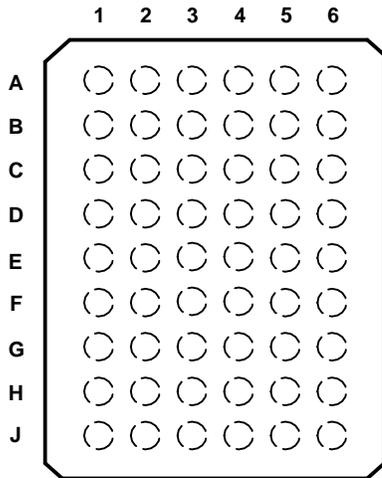


**TERMINAL ASSIGNMENTS<sup>(1)</sup>**  
**(56-Ball GQL/ZQL Package)**

	1	2	3	4	5	6
<b>A</b>	1 $\overline{OE}$	NC	NC	NC	NC	2 $\overline{OE}$
<b>B</b>	1Y2	1Y1	GND	GND	1A1	1A2
<b>C</b>	1Y4	1Y3	V <sub>CC</sub>	V <sub>CC</sub>	1A3	1A4
<b>D</b>	2Y2	2Y1	GND	GND	2A1	2A2
<b>E</b>	2Y4	2Y3			2A3	2A4
<b>F</b>	3Y1	3Y2			3A2	3A1
<b>G</b>	3Y3	3Y4	GND	GND	3A4	3A3
<b>H</b>	4Y1	4Y2	V <sub>CC</sub>	V <sub>CC</sub>	4A2	4A1
<b>J</b>	4Y3	4Y4	GND	GND	4A4	4A3
<b>K</b>	4 $\overline{OE}$	NC	NC	NC	NC	3 $\overline{OE}$

(1) NC – No internal connection

**GRD OR ZRD PACKAGE**  
**(TOP VIEW)**



**TERMINAL ASSIGNMENTS<sup>(1)</sup>**  
**(54-Ball GRD/ZRD Package)**

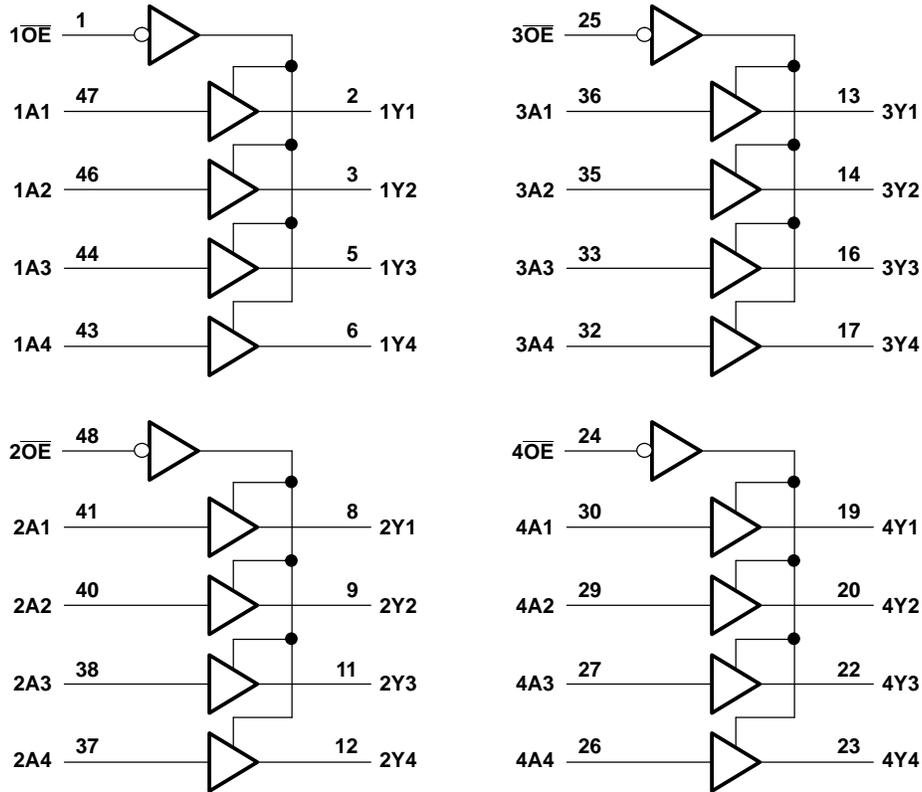
	1	2	3	4	5	6
<b>A</b>	1Y1	NC	1 $\overline{OE}$	2 $\overline{OE}$	NC	1A1
<b>B</b>	1Y3	1Y2	NC	NC	1A2	1A3
<b>C</b>	2Y1	1Y4	V <sub>CC</sub>	V <sub>CC</sub>	1A4	2A1
<b>D</b>	2Y3	2Y2	GND	GND	2A2	2A3
<b>E</b>	3Y1	2Y4	GND	GND	2A4	3A1
<b>F</b>	3Y3	3Y2	GND	GND	3A2	3A3
<b>G</b>	4Y1	3Y4	V <sub>CC</sub>	V <sub>CC</sub>	3A4	4A1
<b>H</b>	4Y3	4Y2	NC	NC	4A2	4A3
<b>J</b>	4Y4	NC	4 $\overline{OE}$	3 $\overline{OE}$	NC	4A4

(1) NC – No internal connection

**FUNCTION TABLE**  
**(EACH 4-BIT BUFFER)**

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	H
L	L	L
H	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG and DL packages.

**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage range	-0.5	4.6	V	
$V_I$	Input voltage range <sup>(2)</sup>	Control Inputs <sup>(3)</sup>	-0.5	$V_{CC} + 0.5$	V
		Data Inputs	-0.5	4.6	
$V_O$	Output voltage range <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V	
$I_{IK}$	Input clamp current		-50	mA	
$I_{OK}$	Output clamp current		-50	mA	
$I_O$	Continuous output current		±50	mA	
	Continuous current through each $V_{CC}$ or GND		±100	mA	
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGG package		70	°C/W
		DL package		63	
		GQL/ZQL package		42	
		GRD/ZRD package		36	
$T_{stg}$	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**SN74ALVC16244A**  
**16-BIT BUFFER/DRIVER**  
**WITH 3-STATE OUTPUTS**

SCAS2500–JANUARY 1993–REVISED OCTOBER 2005

**Recommended Operating Conditions<sup>(1)</sup>**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	1.65	3.6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V	2	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8	
V <sub>I</sub>	Input voltage	Control Inputs	0	V <sub>CC</sub>
		Data Inputs	0	3.6
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V	–4	mA
		V <sub>CC</sub> = 2.3 V	–12	
		V <sub>CC</sub> = 2.7 V	–12	
		V <sub>CC</sub> = 3 V	–24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V	4	mA
		V <sub>CC</sub> = 2.3 V	12	
		V <sub>CC</sub> = 2.7 V	12	
		V <sub>CC</sub> = 3 V	24	
Δt/Δv	Input transition rise or fall rate		10	ns/V
T <sub>A</sub>	Operating free-air temperature	–40	85	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = –100 μA	1.65 V to 3.6 V	V <sub>CC</sub> – 0.2		V	
	I <sub>OH</sub> = –4 mA	1.65 V	1.2			
	I <sub>OH</sub> = –6 mA	2.3 V	2			
	I <sub>OH</sub> = –12 mA	2.3 V	1.7			
		2.7 V	2.2			
	I <sub>OH</sub> = –24 mA	3 V	2.4			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V	0.2		V	
	I <sub>OL</sub> = 4 mA	1.65 V	0.45			
	I <sub>OL</sub> = 6 mA	2.3 V	0.4			
	I <sub>OL</sub> = 12 mA	2.3 V	0.7			
		2.7 V	0.4			
	I <sub>OL</sub> = 24 mA	3 V	0.55			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	±5		μA	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V	±10		μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	40		μA	
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V	750		μA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3		pF	
	Data inputs		6			

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

### Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
C <sub>o</sub>	Outputs	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V		7		pF

### Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	(1)	1	3.7	3.6		1	3	ns
t <sub>en</sub>	$\overline{OE}$	Y	(1)	1	5.7	5.4		1	4.4	ns
t <sub>dis</sub>	$\overline{OE}$	Y	(1)	1	5.2	4.6		1	4.1	ns

(1) This information was not available at the time of publication.

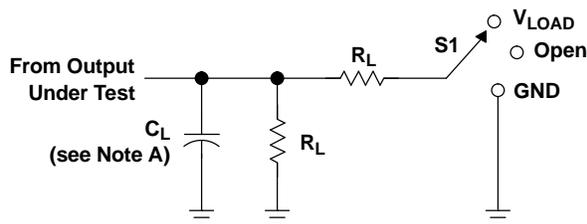
### Operating Characteristics

T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
			TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation	C <sub>L</sub> = 50 pF, f = 10 MHz	(1)	16	19	pF
	capacitance		(1)	4	5	

(1) This information was not available at the time of publication.

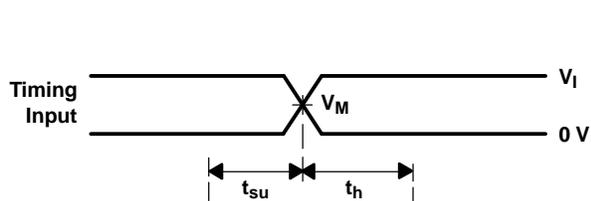
PARAMETER MEASUREMENT INFORMATION



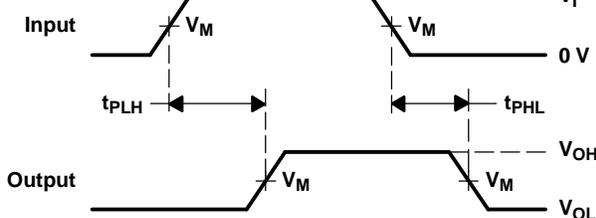
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZH}$	$V_{LOAD}$
$t_{PHZ}/t_{PHZ}$	GND

LOAD CIRCUIT

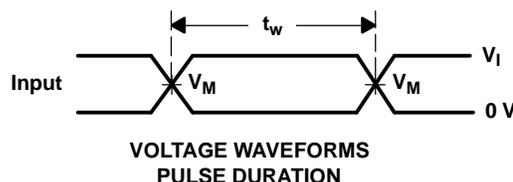
$V_{CC}$	INPUT		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
1.8 V	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5 V \pm 0.2 V$	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5$ ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3 V \pm 0.3 V$	2.7 V	$\leq 2.5$ ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



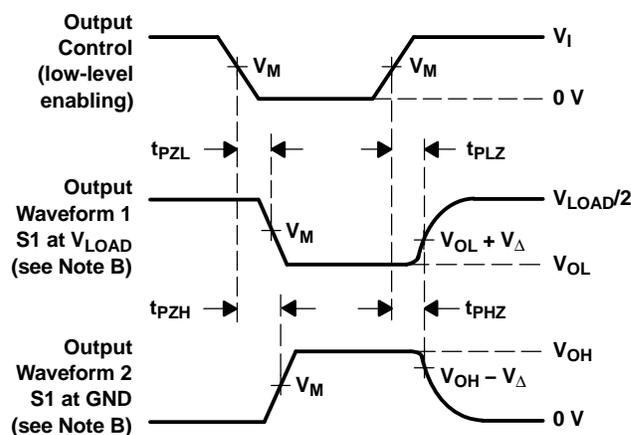
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ .  
D. The outputs are measured one at a time, with one transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74ALVC16244ADGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC16244A	<a href="#">Samples</a>
SN74ALVC16244ADGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC16244A	<a href="#">Samples</a>
SN74ALVC16244ADL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC16244A	<a href="#">Samples</a>
SN74ALVC16244ADLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC16244A	<a href="#">Samples</a>
SN74ALVC16244ADLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC16244A	<a href="#">Samples</a>
SN74ALVC16244AZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	VC244A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

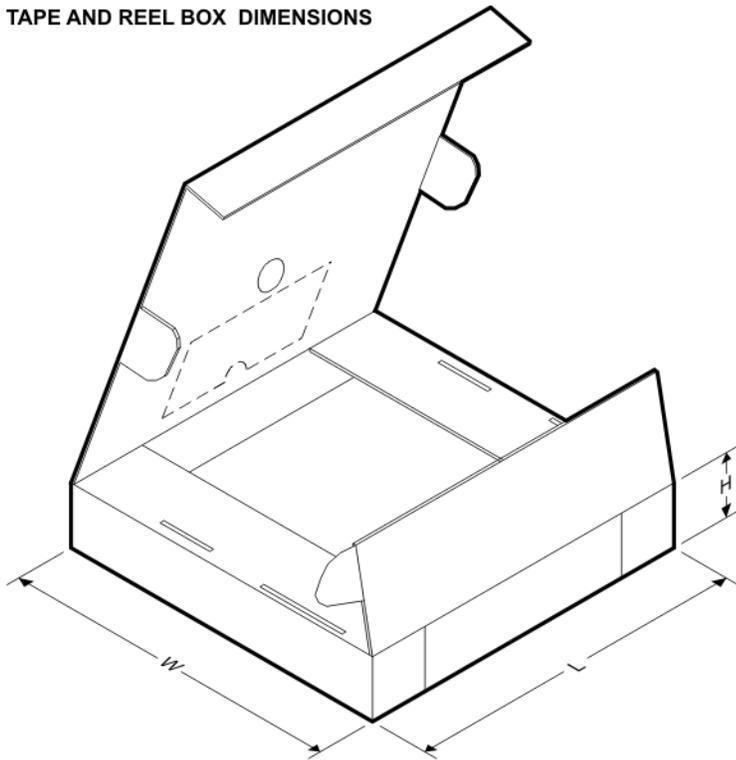


### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVC16244ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ALVC16244ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74ALVC16244AZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


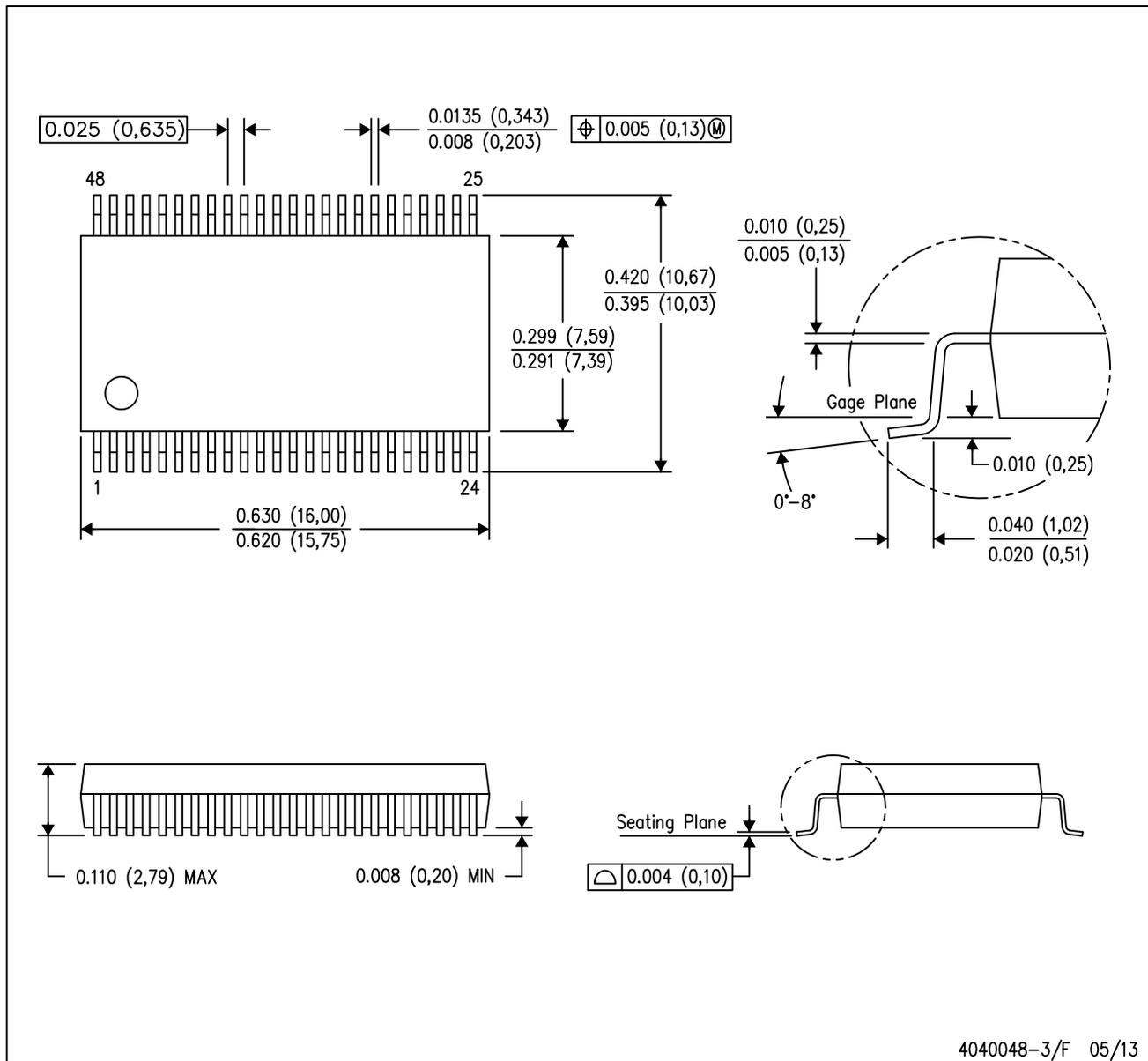
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVC16244ADGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ALVC16244ADLR	SSOP	DL	48	1000	367.0	367.0	55.0
SN74ALVC16244AZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	336.6	336.6	28.6

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



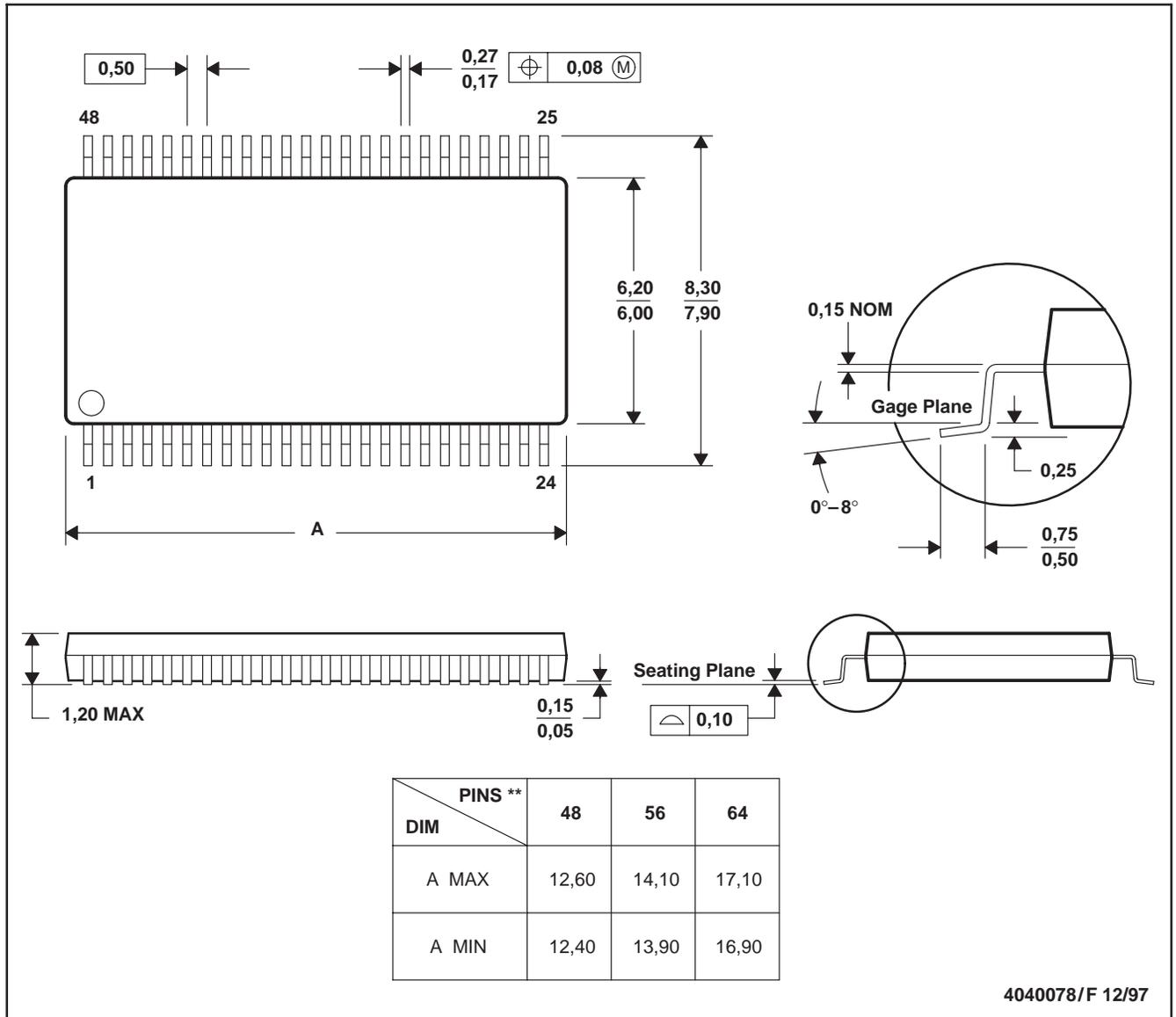
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

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DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

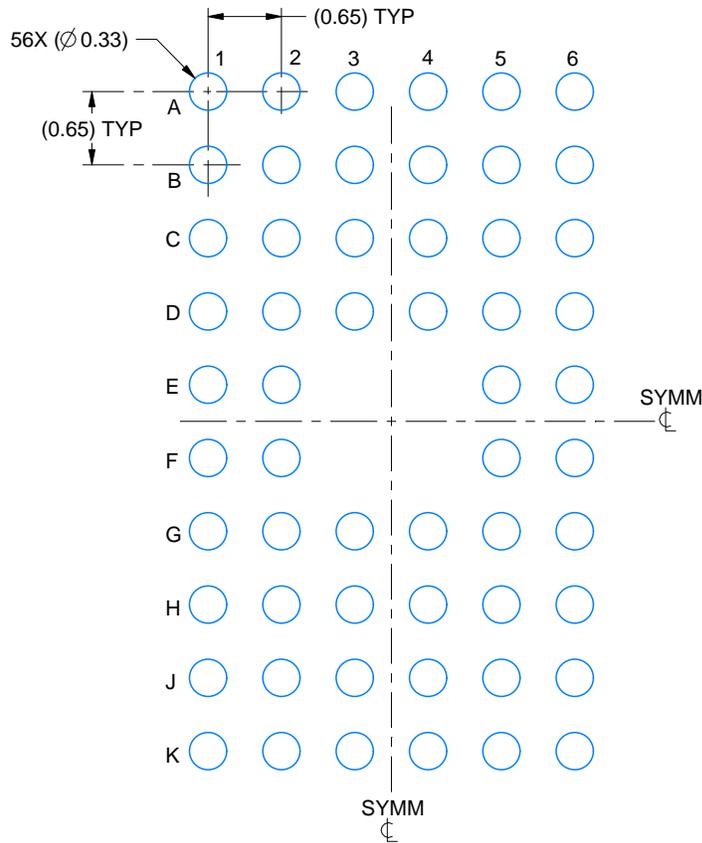


# EXAMPLE BOARD LAYOUT

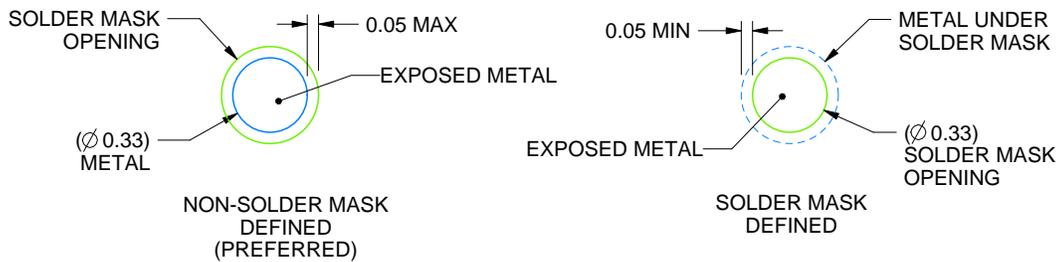
ZQL0056A

JRBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS  
NOT TO SCALE

4219711/B 01/2017

NOTES: (continued)

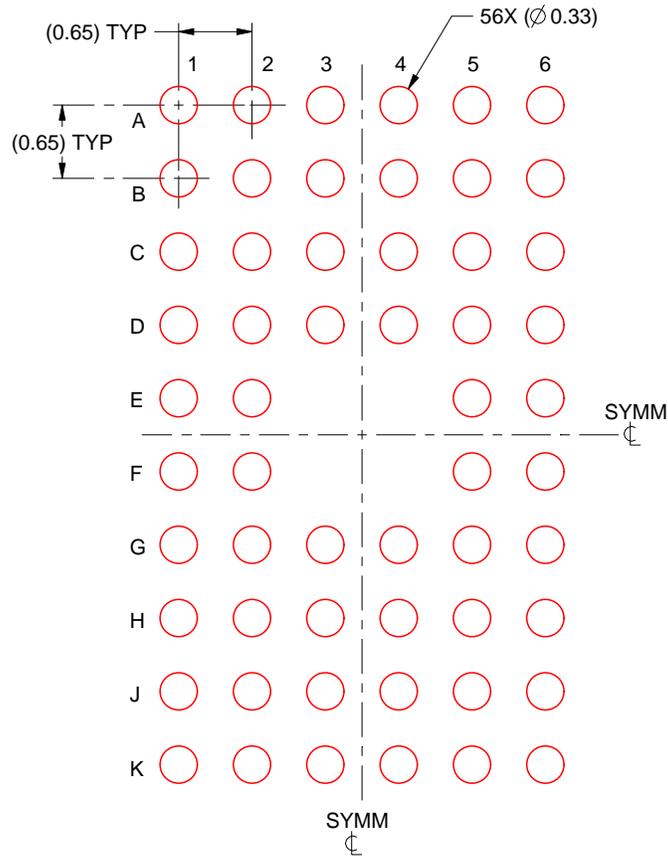
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 ([www.ti.com/lit/spraa99](http://www.ti.com/lit/spraa99)).

# EXAMPLE STENCIL DESIGN

ZQL0056A

JRBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4219711/B 01/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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