DS90UR910-Q1 10 to 75 MHz 24-bit Color FPD-Link II to CSI-2 Converter

1 Features

- Automotive Grade Product: AEC-Q100 Grade 2 Qualified
- 10- to 75-MHz PCLK Support (280-Mbps to 2.1-Gbps FPD-Link II Linerate)
- Compatible to DC Balanced, AC-Coupled for FPD-Link II Serial Bit Stream
- Capable to Recover Data up to 10 Meters STP Cable
- MIPI D-PHY Modules Conform to v1.00.00
- Compatible With MIPI CSI-2 Version 1.01
- Supports Data Rate up to 900 Mbps per Data Lane With Two Lanes
- Video Stream Packet Formats: RGB888
- Continuous and Non-Continuous Clocking Mode
- Ultra Low Power, Escape, High Speed, and Control Modes Support
- Integrated Input Terminations and Adjustable Receive Equalization
- Fast Random Lock (No Reference Clock Required)
- CCI (Camera Control Interface) and I2C Compatible Control Bus
- @Speed BIST and Reporting Pin
- Single 1.8-V Power Supply
- 1.8-V or 3.3-V Compatible LVCMOS I/O Interface
- 8-kV ISO 10605 ESD Rating
- Leadless 40-Pin WQFN Package (6 mm × 6 mm)

2 Applications

- Automotive Infotainment:
  - Central Information Displays
  - Rear Seat Entertainment Systems
  - Digital Instrument Clusters

3 Description

The DS90UR910-Q1 is an interface bridge chip that recovers data from the FPD-Link II serial bit stream and converts into a Camera Serial Interface (CSI-2) format compatible with Mobile Industry Processor Interface (MIPI) specifications. It recovers the 24- or 18-bit RGB data and 3 video sync-signals from the serial bit stream compatible to FPD-Link II serializers. The recovered data is packetized and serialized over two data lanes strobed by a half-rate serial clock compliant with the MIPI DPHY and CSI-2 specifications, each running up to 900 Mbps. The FPD-Link II receiver supports pixel clocks of up to 75 MHz. The CSI-2 output serial bus greatly reduces the interconnect and signal count to a graphic processing unit (GPU) and eases system designs for video streams from multiple automotive driver assist cameras.

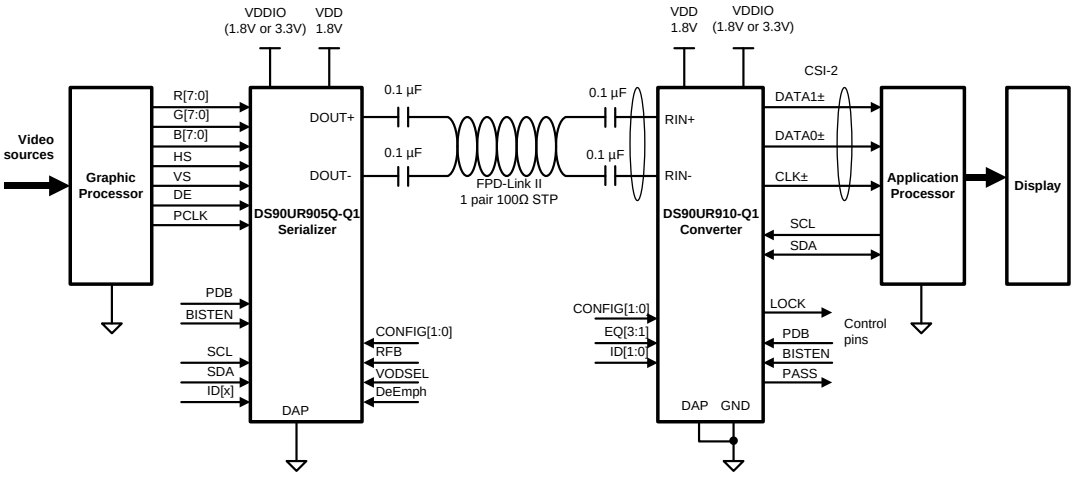
The DS90UR910-Q1 is available in a 40-pin WQFN package. Electrical performance is qualified for automotive AEC-Q100 grade 2 temperature range –40°C to 105°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
DS90UR910-Q1	WQFN (40)	6.00 mm x 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Applications Diagram



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4 Revision History

Changes from Revision D (July 2015) to Revision E — **Page**

- Added *Device Functional Modes* and *Application Information* sections ... 1
- Added *Thermal Information* table ... 6

Changes from Revision C (May 2013) to Revision D — **Page**

- Changed device status from Product Preview to Production Data ... 1
- Added new section titles to update to new TI format. ... 1

Changes from Revision B (October 2012) to Revision C — **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 1
- Changed Pin # for VDDL and VDDA Power pins for clarification ... 4

Changes from Revision A (September 2012) to Revision B — **Page**

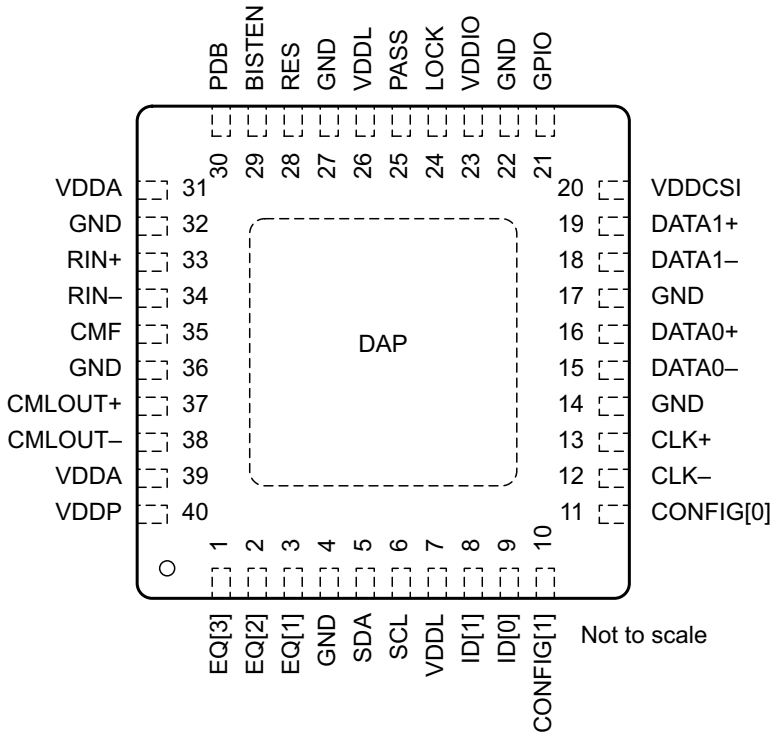
- Changed Pin Diagram ... 3

Changes from Original (June 2012) to Revision A — **Page**

- DS90UR910-Q1 DATASHEET – Initial Release ... 1

5 Pin Configuration and Functions

RTA Package
40-Pin WQFN
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME(2)	NO.		
FPD-LINK II SERIAL INTERFACE			
RIN+	33	I	CML, inverting and noninverting differential inputs. The inputs must be AC-coupled with a 100-nF capacitor.
RIN–	34	I	CML, inverting and noninverting differential inputs. The inputs must be AC-coupled with a 100-nF capacitor.
CMF	35	I	Analog, common mode filter pin for the differential inputs. CMP is the virtual ground of the differential input stage. A bypass capacitor is connected from CMP to ground to increase the receiver's common mode noise immunity. TI recommends a 4.7-µF ceramic capacitor.
CMLOUT+	37	O	CML, inverting and noninverting differential outputs. Single 100-Ω (1%) termination resistor must be placed across the CMLOUT± pins. Optional loop-through output to monitor post equalizer and requires use of the Serial Control Bus to enable.
CMLOUT–	38	O	CML, inverting and noninverting differential outputs. Single 100-Ω (1%) termination resistor must be placed across the CMLOUT± pins. Optional loop-through output to monitor post equalizer and requires use of the Serial Control Bus to enable.
MIPI INTERFACE			
DATA1+	19	O	DPHY, inverting and noninverting data output of DPHY Lane 1.
DATA1–	18	O	DPHY, inverting and noninverting data output of DPHY Lane 1.
DATA0+	16	O	DPHY, inverting and noninverting data output of DPHY Lane 0.
DATA0–	15	O	DPHY, inverting and noninverting data output of DPHY Lane 0.
CLK+	13	O	DPHY, inverting and noninverting half-rate DPHY clock lane.
CLK–	12	O	DPHY, inverting and noninverting half-rate DPHY clock lane.

(1) G = Ground, I = Input, O = Output, P = Power
(2) 1 = HIGH, 0 = LOW

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME(2)	NO.		
CONTROL AND CONFIGURATION			
PDB	30	I	LVCMOS with pulldown, power down mode input; PDB = 1, Device is enabled (normal operation), PDB = 0, Device is in power-down, When the device is in the power-down, outputs are TRI-STATE, control registers are RESET.
CONFIG[1:0]	10, 11	I	LVCMOS with pulldown, operating mode select; CONFIG[1:0] selects compatibility to FPD-Link II serializers. See Table 1.
EQ[3:1]	1, 2, 3	I	LVCMOS with pulldown, receive equalization control; EQ[3:1] provides 8 combinations of the receive equalization gain settings. See Table 2. EQ[3:1] optimizes the input equalizer's ability to reduce inter-symbol interference from the loss characteristics of different cable lengths.
BISTEN	29	I	LVCMOS with pulldown, BIST enable input; BISTEN = 1, BIST is enabled, BISTEN = 0, BIST is disabled.
LOCK	24	O	LVCMOS, LOCK status output; LOCK = 1, PLL acquired lock to the reference clock input; DPHY outputs are active LOCK = 0, PLL is unlocked
PASS	25	O	LVCMOS, normal mode status output pin (BISTEN = 0); PASS = 1: No fault detected on input display timing, PASS = 0: Indicates an error condition or corruption in display timing. Fault condition occurs if: 1) DE length value mismatch measured once in succession, 2) VSync length value mismatch measured twice in succession, BIST mode status output pin (BISTEN = 1); PASS = 1: No error detected, PASS = 0: Error detected.
CCI AND I2C SERIAL CONTROL BUS			
SCL	6	I	LVCMOS open drain, serial control bus clock input, SCL requires an external pullup resistor to V_{DDIO}.
SDA	5	I/O	LVCMOS open drain, serial control bus data input and output, SDA requires an external pullup resistor to V_{DDIO}.
ID[1:0]	8, 9	I	LVCMOS with pulldown, serial control bus device ID address select, see Table 6.
RESERVED PINS			
GPIO	21	I/O	General purpose I/O; Pin must be left floating during initial power-up.
RES	28	I	LVCMOS with pulldown, reserved pin (must tie low)
POWER AND GROUND			
VDDL	7, 26	P	Power to logic circuitry, 1.8 V ±5%
VDDA	31, 39	P	Power to analog circuitry, 1.8 V ±5%
VDDP	40	P	Power to PLL, 1.8 V ±5%
VDDCSI	20	P	Power to DPHY CSI-2 drivers, 1.8 V ±5%
VDDIO	23	P	Power to LVCMOS I/O circuitry, 1.8 V ±5% or 3.3 V ±10% (V_{DDIO})
GND	4, 14, 17, 22, 27, 32, 36	G	Ground return
GND	DAP	G	DAP is the metal contact at the bottom side, located at the center of the WQFN package. It must be connected to the GND plane with multiple via to lower the ground impedance and improve the thermal performance of the package. Connected to the ground plane (GND) with at least 9 vias.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply voltage	V_{DDA}, V_{DDP}, V_{DDL}, V_{DDCSI} (1.8 V)	−0.3	2.5	V
	V_{DDIO} (1.8-V I/O)	−0.3	2.5	
	V_{DDIO} (3.3-V I/O)	–0.3	4	
LVCMOS I/O voltage		−0.3	V_{DDIO} + 0.3	V
Receiver input voltage		−0.3	V_{DDA} + 0.3	V
CSI-2 output voltage		−0.3	V_{DDCSI} + 0.3	V
40L WQFN package, maximum power dissipation capacity at 25°C (derate above 25°C)			$1/R_{\theta JA}$	mW/°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For soldering specifications, see product folder at www.ti.com and *Absolute Maximum Ratings for Soldering* (SNOA549).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per AEC Q100-002, all pins(1)		±8000	V
	Charged device model (CDM), per AEC Q100-011, all pins		±1000	
	Machine model (MM)		±250	
	IEC, powered-up only, R_D = 330 Ω, C_S = 150 pF	Air discharge (R_{IN+}, $R_{IN–}$)	±30000	
		Contact discharge (R_{IN+}, $R_{IN–}$)	±10000	
	ISO10605, R_D = 330 Ω, C_S = 150 pF	Air discharge (R_{IN+}, $R_{IN–}$)	±30000	
		Contact discharge (R_{IN+}, $R_{IN–}$)	±10000	
	ISO10605, R_D = 2 kΩ, C_S = 150 pF or 330 pF	Air discharge (R_{IN+}, $R_{IN–}$)	±30000	
		Contact discharge (R_{IN+}, $R_{IN–}$)	±10000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DDA}, V_{DDP}, V_{DDL}, V_{DDCSI}	Supply voltage		1.71	1.8	1.89	V
V_{DDIO}	LVCMOS supply voltage	1.8-V I/O	1.71	1.8	1.89	V
		3.3-V I/O	3	3.3	3.6	
PCLK	Clock frequency		10		75	MHz
V_{DDn}	Supply noise (1.8 V)				25	mV_{P-P}
V_{DDIO}	Supply noise	1.8-V I/O			25	mV_{P-P}
		3.3-V I/O			50	
T_A	Operating free-air temperature		–40	25	105	°C

6.4 Thermal Information

THERMAL METRIC[1]		DS90UB921Q-1 RTA (WQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: DC

over operating free-air temperature range (unless otherwise noted)[1][2][3]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
3.3-V I/O LVCMOS, V_{DDIO} = 3 to 3.6 V (BISTEN, LOCK, PASS, PDB, EQ[3:1], ID[1:0], CONFIG[1:0], GPIO)							
V_{IH}	High-level input voltage	V_{IN} = 3 V to 3.6 V		2.2		V_{DDIO}	V
V_{IL}	Low-level input voltage	V_{IN} = 3 V to 3.6 V		GND		0.8	V
I_{IN}	Input current	V_{IN} = 0 V or V_{DDIO}		–15		15	µa
V_{OH}	High-level output voltage	I_{OH} = −2 mA		2.4		V_{DDIO}	V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA		GND		0.4	V
I_{OZ}	TRI-STATE® output current	PDB = 0 V		–15		15	µa
1.8-V I/O LVCMOS, V_{DDIO} = 1.71 to 1.89 V (BISTEN, LOCK, PASS, PDB, EQ[3:1], ID[1:0], CONFIG[1:0], GPIO)							
V_{IH}	High-level input voltage	V_{IN} = 1.71 V to 1.89 V		0.65 × V_{DDIO}		V_{DDIO}	V
V_{IL}	Low-level input voltage	V_{IN} = 1.71 V to 1.89 V		GND		0.35 × V_{DDIO}	V
I_{IN}	Input current	V_{IN} = 0 V or V_{DDIO}		–15		15	µa
V_{OH}	High-level output voltage	I_{OH} = –2 mA		V_{DDIO} – 0.45		V_{DDIO}	V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA		GND		0.45	V
I_{OZ}	TRI-STATE output current	PDB = 0 V		–15		15	µa
SUPPLY CURRENT							
I_{DD1}	Supply current	Supply current drawn from 1.8-V rail (V_{DDL}, V_{DDP}, V_{DDA}), checker board pattern	V_{DDL}, V_{DDP}, V_{DDA} = 1.89 V, f = 75 MHz (900 Mbps)		88	95	mA
			V_{DDL}, V_{DDP}, V_{DDA} = 1.89 V, f = 10 MHz (120 Mbps)		38		
I_{DDTX1}	Supply current	Supply current drawn at V_{DDCSI}, checker board pattern	V_{DDCSI} = 1.89 V, f = 75 MHz (900 Mbps)		50	65	mA
			V_{DDCSI} = 1.89 V, f = 10 MHz (120 Mbps)		22		
I_{DDIO1}	Supply current	Supply current drawn at V_{DDIO}, checker board pattern	V_{DDIO} = 1.89 V, f = 75 MHz (900 Mbps)			10	mA
			V_{DDIO} = 3.6 V, f = 75 MHz (900 Mbps)			15	

(1) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.
(2) Typical values represent most likely parametric norms at V_{DD} = 3.3 V, T_A = 25°C, and at the recommended operation conditions at the time of product characterization and are not ensured.
(3) The Electrical Characteristics tables list ensured specifications in *Recommended Operating Conditions* except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.

Electrical Characteristics: DC (continued)

over operating free-air temperature range (unless otherwise noted)[1][2][3]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DDZ}	Supply current at power down mode	Supply current drawn from 1.8-V rail (V_{DDL}, V_{DDP}, V_{DDA}), PDB = 0 V, V_{DDL}, V_{DDP}, V_{DDA} = 1.89 V (all other LVCMOS inputs low)				5	mA
I_{DDTXZ}	Supply current at power down mode	Supply current drawn at V_{DDCSI}, PDB = 0 V, V_{DDCSI} = 1.89 V (all other LVCMOS inputs low)				5	mA
I_{DDIOZ}	Supply current at power down mode	Supply current drawn at V_{DDIO}, PDB = 0 V (all other LVCMOS inputs low)	V_{DDIO} = 1.89 V			3	mA
			V_{DDIO} = 3.6 V			3	
I_{DDUPLS}	Ultra-low power state current	Supply current drawn from 1.8 V at (V_{DDL}, V_{DDP}, V_{DDA}, V_{DDCSI} and V_{DDIO}), V_{DD} = 1.89 V, V_{DDIO} = 3.6 V, PLL off, no change in all input signals, Register: 0x19h = 0x03h 0x01h = 0x02h				20	mA
FPD-LINK II RECEIVER (RIN±)							
V_{TH}	Differential input threshold high voltage	V_{CM} = 1.2 V (internal V_{BIAS})				50	mV
V_{TL}	Differential input threshold low voltage	V_{CM} = 1.2 V (internal V_{BIAS})		–50			mV
V_{CM}	Common mode voltage, internal V_{BIAS}				1.2		V
I_{IN}	Input current	V_{IN} = 0 V or V_{DD}		−15		15	µa
R_T	Internal termination resistor	Differential across RIN+ and RIN–		80	100	120	Ω
CMLOUT± DRIVER OUTPUT (CMLOUT±)							
V_{OD}	Differential output voltage[4]	R_L = 100 Ω			500		mV
V_{OS}	Offset voltage, single-ended	R_L = 100 Ω			1.3		V
R_T	Internal termination resistor	Differential across CMLOUT+ and CMLOUT–		80	100	120	Ω
HSTX DRIVER (DATA0±, DATA1±, CLK±)							
V_{CMTX}	HS transmit static common-mode voltage			150	200	250	mV
$\lvert\Delta V_{CMTX(1,0)}\rvert$	VCMTX mismatch when output is 1 or 0 state					5	mV
$\lvert V_{OD}\rvert$	HS transmit differential voltage			140	200	270	mV
$\lvert\Delta V_{OD}\rvert$	VOD mismatch when output is 1 or 0 state					10	mV
V_{OHHS}	HS output high voltage					360	mV
Z_{OS}	Single ended output impedance			40	50	62.5	Ω
ΔZ_{OS}	Mismatch in single ended output impedance					10%	
LPTX DRIVER (DATA0±, DATA1±, CLK±)							
V_{OH}	Output high level[5]			1.1	1.2	1.3	V
V_{OL}	Output low level			−50		50	mV
Z_{OLP}	Output impedance			110			Ω

(4) Voltage difference compared to the DC average common mode potential.
(5) Specification is ensured by characterization.

6.6 Switching Characteristics: AC

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FPD-LINK II RECEIVER (RIN±)							
t_{IJT}	Input jitter tolerance, see Figure 1	EQ = OFF, PCLK = 65 MHz	jitter freq < 2 MHz		0.9		UI(1)
			jitter freq > 6 MHz		0.5		UI
t_{DDLT}	Deserializer lock time see Figure 2	PCLK = 75 MHz			10		ms
HSTX DRIVER (DATA0±, DATA1±, CLK±)							
$HSTX_{DBR}$	Data bit rate	DATA0±, DATA1±, PCLK = 10 to 75 MHz(2)		120	PCLK × 12	900	Mbps
f_{CLK}	DDR Clock frequency	CLK±, PCLK = 10 to 75 MHz(2)		60	PCLK × 6	450	MHz
$\Delta V_{CMTX(HF)}$	Common mode voltage variations HF	Common-level variations above 450 MHz(2)				15	mV_{RMS}
$\Delta V_{CMTX(LF)}$	Common mode voltage variations LF	Common-level variations between 50 to 450 MHz(2)				25	mV_{PEAK}
t_{RHS}	Rise time HS	20% to 80% rise time(3)				0.3	UI_{INST}
				150			ps
t_{FHS}	Fall time HS	20% to 80% rise time(3)				0.3	UI_{INST}
				150			ps
SDD_{TX}	TX differential return loss(2)	f_{LPMAX}				–18	dB
		f_H				–12	dB
		f_{MAX}				–6	dB
SCC_{TX}	TX common mode return loss(2)	f_{LPMAX} to f_{MAX}				–6	dB
LPTX DRIVER (DATA0±, DATA1±, CLK±)(4)							
t_{RLP}	Rise time	LP 15% to 85% rise time C_{LOAD} = 70 pF lumped capacitance				25	ns
t_{FLP}	Fall time	LP 15% to 85% fall time C_{LOAD} = 70 pF lumped capacitance				25	ns
t_{REOT}	Post-EoT rise and fall time	30% to 85% rise time and fall time(2)				35	ns
$t_{LP-PULSE-TX}$	Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state (2)		40			ns
		All other pulses(2)		20			ns
$t_{LP-PER-TX}$	Period of the LP exclusive-OR clock(2)			90			ns
σV/σtSR	Slew rate	C_{LOAD} = 0 pF(5)(4)(6)				500	mV/ns
		C_{LOAD} = 5 pF(5)(4)(6)				300	mV/ns
		C_{LOAD} = 20 pF(5)(4)(6)				250	mV/ns
		C_{LOAD} = 70 pF(3)(4)(6)				150	mV/ns
		C_{LOAD} = 0 to 70 pF (falling edge only)(3)(4)(6)(7)		30			mV/ns
		C_{LOAD} = 0 to 70 pF (rising edge only)(3)(4)(6)		30			mV/ns
		C_{LOAD} = 0 to 70 pF (rising edge only)(3)(4)(8)(9)		30 – 0.075 × ($V_{O,INST}$ – 700)			mV/ns
C_{LOAD}	Load capacitance(4)			0		70	pF

(1) UI is equivalent to one serialized data bit width (1UI = 1 / 28 × PCLK). The UI scales with PCLK frequency.
(2) Specification is ensured by design and is not tested in production.
(3) Specification is ensured by characterization.
(4) C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10 pF. The distributed line capacitance can be up to 50 pF for a transmission line with 2-ns delay.
(5) Specification is ensured by characterization.
(6) Measured as average across any 50 mV segment of the output signal transition.
(7) When the output voltage is between 400 mV and 930 mV.
(8) Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.
(9) When the output voltage is between 700 mV and 930 mV.

Switching Characteristics: AC (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DATA-CLOCK TIMING SPECIFICATIONS (DATA0±, DATA1±, CLK±)						
UI_{INST}	Instantaneous unit interval, see Figure 3	PCLK = 10 to 75 MHz (10)		1/(PCLK × 12)		ns
$t_{SKEW(TX)}$	Data to clock skew see Figure 3	Skew between clock and data from ideal center (2)	0.5 – 0.15	0.5	0.5 + 0.15	UI_{INST}
CSI-2 TIMING SPECIFICATIONS (DATA0±, DATA1±, CLK±) (2) (see Figure 4 and Figure 5)						
$t_{CLK–POST}$	HS exit		60 + 52 × UI_{INST}			ns
$t_{CLK–PRE}$	Time HS clock shall be driver prior to any associated Data Lane beginning the transition from LP to HS mode		8			UI_{INST}
$t_{CLK–PREPARE}$	Clock lane HS entry		38		95	ns
$t_{CLK–SETTLE}$	Time interval during which the HS receiver shall ignore any clock lane HS transitions		95		300	ns
$t_{CLK–TERM-EN}$	Time-out at clock lane display module to enable HS termination				38	ns
$t_{CLK–TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst		30			ns
$t_{CLK–PREPARE}$ + $t_{CLK–ZERO}$	TCLK–PREPARE + time that the transmitter drives the HS-0 state prior to starting the clock		300			ns
$t_{D-TERM-EN}$ (11)	Time for the data lane receiver to enable the HS line termination		35 + 4 × UI_{INST}			ns
t_{LPX}	Transmitted length of LP state		50			ns
$t_{HS-PREPARE}$	Data lane HS entry		40 + 4 × UI_{INST}		85 + 6 × UI_{INST}	ns
$t_{HS-PREPARE}$ + $t_{HS-ZERO}$	tHS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the sync sequence		145 + 10 × UI_{INST}			ns
$t_{HS-SETTLE}$	Interval HS receiver shall ignore any data lane HS transitions		85 + 6 × UI_{INST}		145 + 10 × UI_{INST}	ns
$t_{HS-TRAIL}$	Data lane HS exit		60 + 4 × UI_{INST}			ns
t_{EOT}	Transmitted time interval from the start of tHS-TRAIL to the start of the LP-11 state following a HS burst				105 + 12 × UI_{INST}	ns
$t_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.		100			ns
t_{WAKEUP}	Recovery time from ultra-low power state (ULPS)		1			ms

(10) UI_{INST} is equal to 1 / (12 × PCLK), where PCLK is the fundamental frequency for data transmission.
(11) This parameter value can be lower then TLPX due to differences in rise versus fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior as described in D-PHY ver 1.00.00.

6.7 Timing Requirements: Serial Control Bus (CCI and I2C)

over operating free-air temperature range (unless otherwise noted; see Figure 7)(1)

			MIN	NOM	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode	>0		100	kHz
		Fast mode	>0		400	kHz
t_{LOW}	SCL low period	Standard mode	4.7			µs
		Fast mode	1.3			µs
t_{HIGH}	SCL high period	Standard mode	4			µs
		Fast mode	0.6			µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition	Standard mode	4			µs
		Fast mode	0.6			µs
$t_{SU;STA}$	Set-up time for a start or a repeated start condition	Standard mode	4.7			µs
		Fast mode	0.6			µs
$t_{HD;DAT}$	Data hold time	Standard mode	0		3.45	µs
		Fast mode	0		0.9	µs
$t_{SU;DAT}$	Data set-up time	Standard mode	250			ns
		Fast mode	100			ns
$t_{SU;STO}$	Set-up time for STOP condition	Standard mode	4			µs
		Fast mode	0.6			µs
$t_{BµF}$	Bus Free Time between STOP and START	Standard mode	4.7			µs
		Fast mode	1.3			µs
t_r	SCL and SDA rise time	Standard mode			1000	ns
		Fast mode			300	ns
t_f	SCL and SDA fall time	Standard mode			300	ns
		Fast mode			300	ns

(1) Recommended Input Timing Requirements are input specifications and not tested in production.

6.8 Timing Requirements: DC and AC Serial Control Bus (CCI and I2C)

over operating free-air temperature range (unless otherwise noted; see Figure 7)

			MIN	NOM	MAX	UNIT
V_{IH}	Input high level voltage	SDA and SCL	0.65 × V_{DDIO}		V_{DDIO}	V
V_{IL}	Input low level voltage	SDA and SCL	GND		0.35 × V_{DDIO}	V
V_{HY}	Input hysteresis	Fast mode, 3.3-V I/O(1)	0.05 × V_{DDIO}			mV
		Fast mode, 1.8 V I/O		0.1 × V_{DDIO}		mV
V_{OL}	Output low level voltage	SDA, I_{OL} = 1.5 mA	0		0.4	V
t_R	SDA rise time – READ	Total capacitance of one bus line, Cb ≤ 400 pF			300	ns
t_F	SDA fall time – READ	Standard mode			1000	ns
		Fast mode			300	ns
$t_{SU;DAT}$	Set-up time – READ	Standard mode	250			ns
		Fast mode	100			ns
$t_{HD;DAT}$	Hold-up time – READ		0			ns
t_{SP}	Input filter	Fast mode		50		ns
C_{in}	Input capacitance	SDA and SCL		5		pF

(1) Specification is ensured by characterization.

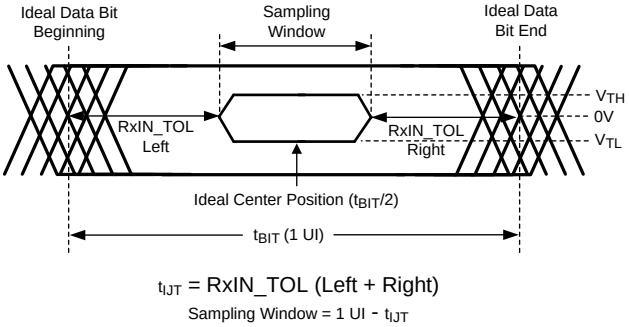


Figure 1. Receiver Input Jitter Tolerance

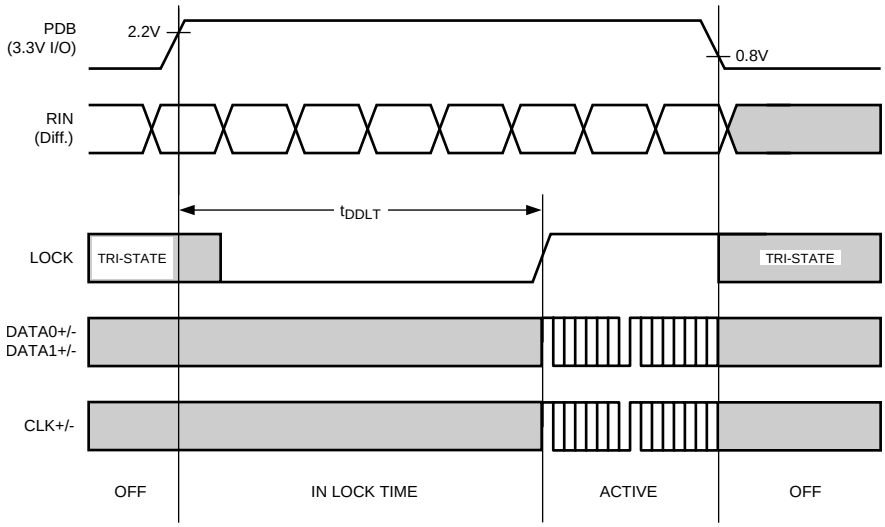


Figure 2. Deserializer PLL Lock Time

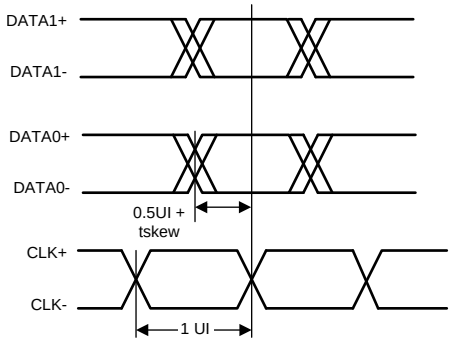


Figure 3. Clock and Data Timing in HS Transmission

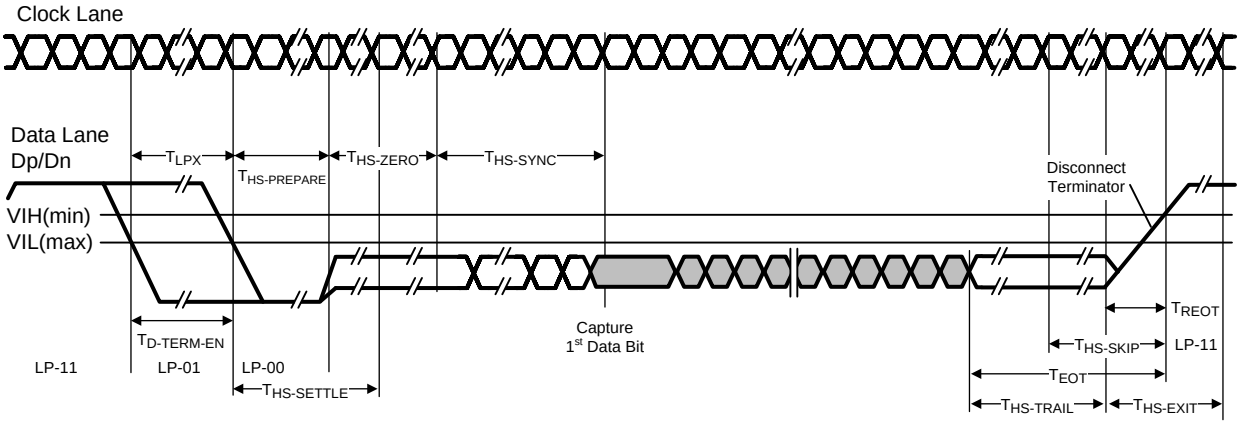


Figure 4. High-Speed Data Transmission Burst

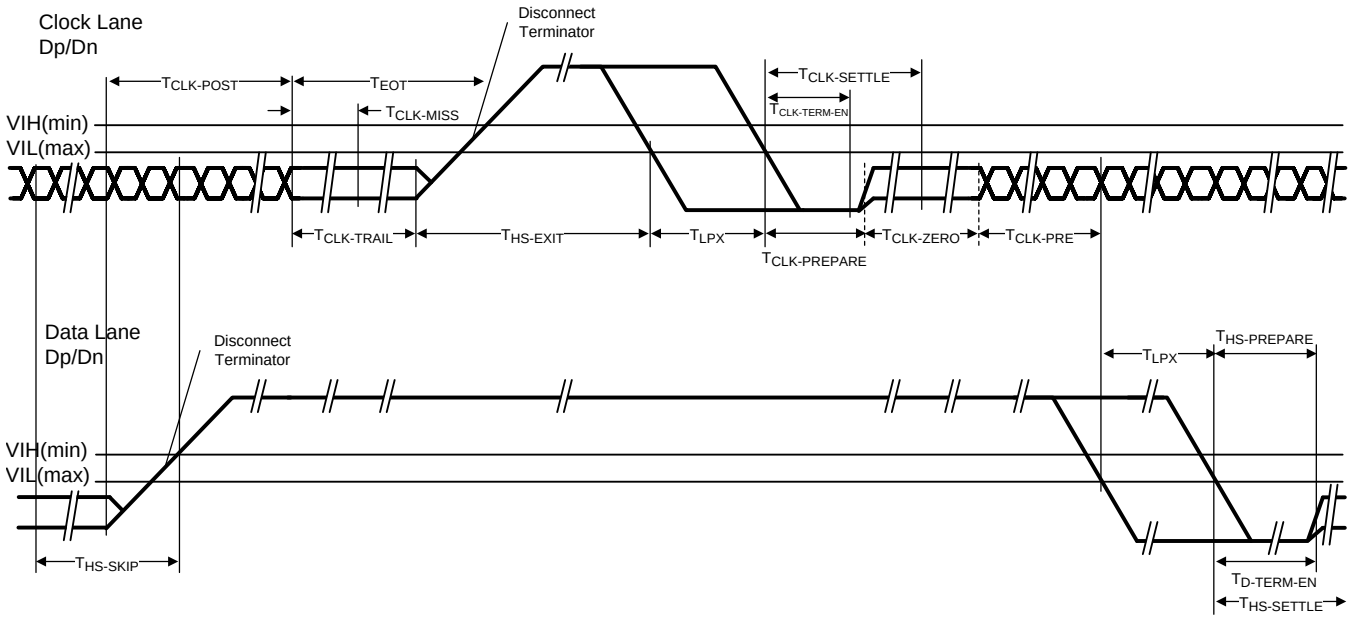


Figure 5. Switching the Clock Lane Between Clock Transmission and Low-Power Mode

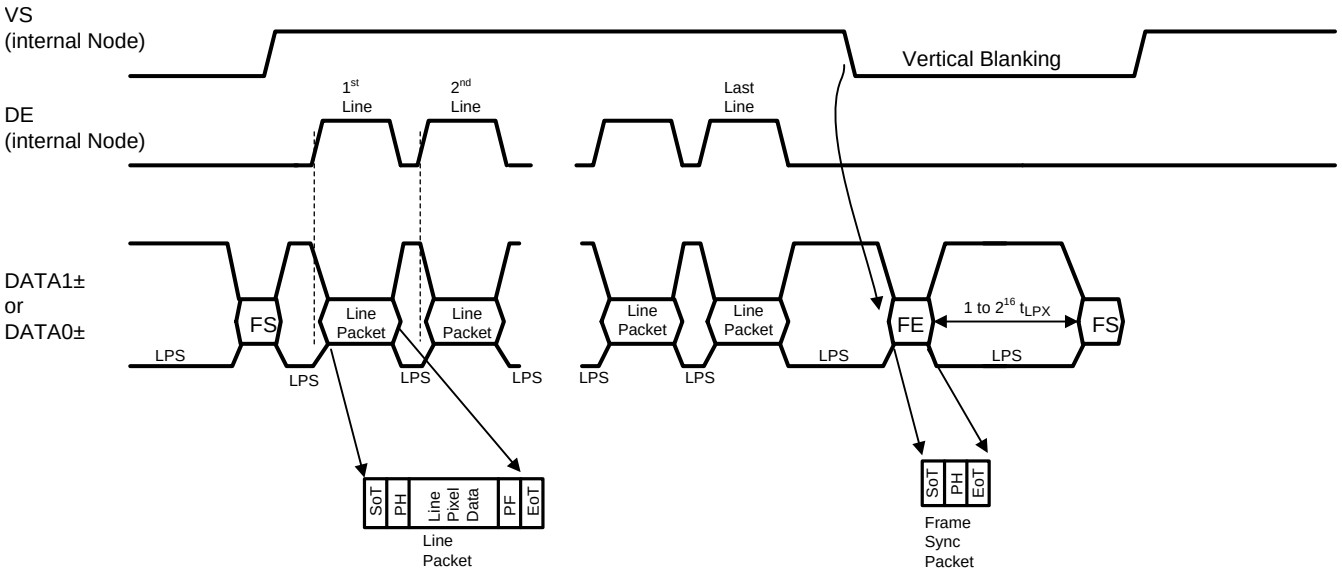


Figure 6. Long Line Packets and Short Frame Sync Packets

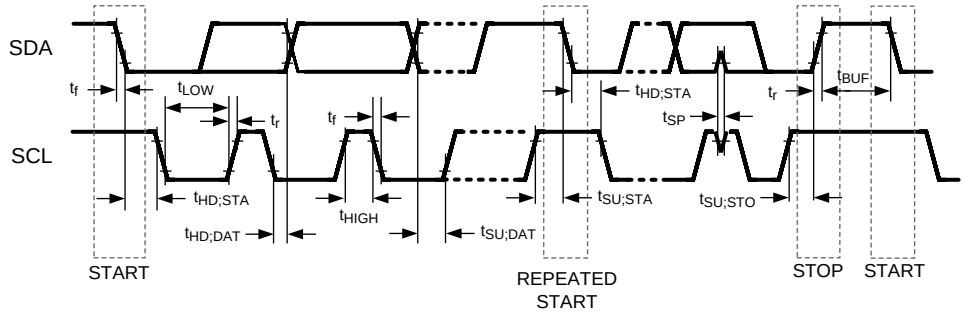


Figure 7. Serial Control Bus Timing Diagram

6.9 Typical Characteristics

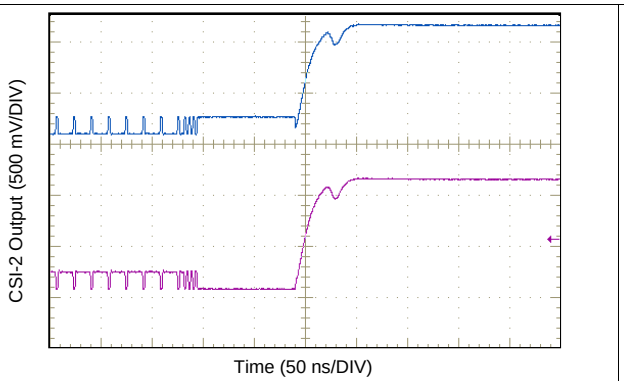


Figure 8. CSI-2 D0± End of Transmission

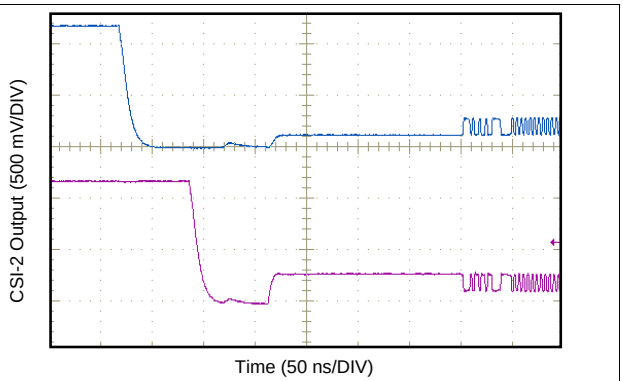


Figure 9. CSI-2 D0± Start of Transmission

7 Detailed Description

7.1 Overview

The DS90UR910-Q1 device recovers RBG data and sync signals from a FPD-Link II AC-coupled serial bit stream, and converts the recovered data into packetized CSI-2 data format. The CSI-2 output serial interface greatly reduces the interconnect and signal count to a graphic processing unit and eases system designs for video streams from multiple automotive driver assist cameras.

The DS90UR910-Q1 is based on the DS90UR906Q de-serializer core. See the DS90UR906Q data sheet, *DS90UR90Q-Q1 5- to 65-MHz, 24-bit Color FPD-Link II Serializer and Deserializer* (SNLS313), for the functionality and performance of the FPD-Link II interface can be found in the DS90UR906Q data sheet.

The DS90UR910-Q1 conforms to the MIPI CSI-2 and DPHY standards for protocol and electrical specifications. Compliant with standards:

- Conforms with MIPI Alliance Specification for D-PHY, version 1.00.00, dated May 14, 2009
- Compatible with MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.01, dated Nov 9, 2010

The DS90UR910-Q1 receives 24-bit (or 18-bit) RGB data and 3 low speed control signals (VS, HS, DE) over a serial FPD-Link II transmitted through a single twisted pair. It supports a pixel clock of 10 MHz to 75 MHz, corresponding to the serial line rate of 280 Mb/s to 2100 Mb/s. The serial bit stream contains the scrambled 24-bit data, an embedded clock, encoded control signals and DC balance information which enhances signal quality and supports AC coupling.

The DS90UR910-Q1 is compatible with FPD-Link II serializers such as DS90UR905Q, DS90UR241Q, DS90C241Q, DS90UR907Q, DS99R421Q, and DS90Ux92x FPD-Link III serializers in backward compatibility mode. Figure 10 shows the serial bit stream. In each pixel clock cycle, a 28-bit frame is transmitted over the FPD-Link. The frame contains C1 and C0 representing the embedded clock information. C1 is always high and C0 is always low. Payload bits b[23:0] contain the scrambled 24-bit RGB data. DCB is the DC balance bit and is used to minimize the DC offset on the signal line. DCA is used to validate the data integrity in the embedded data stream and contain the encoded control signals VS, HS and DE (DS90UR905Q, DS90UR907Q, and DS90Ux92x in backward compatible mode).

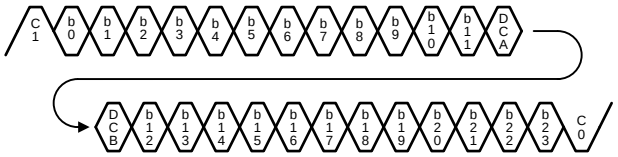


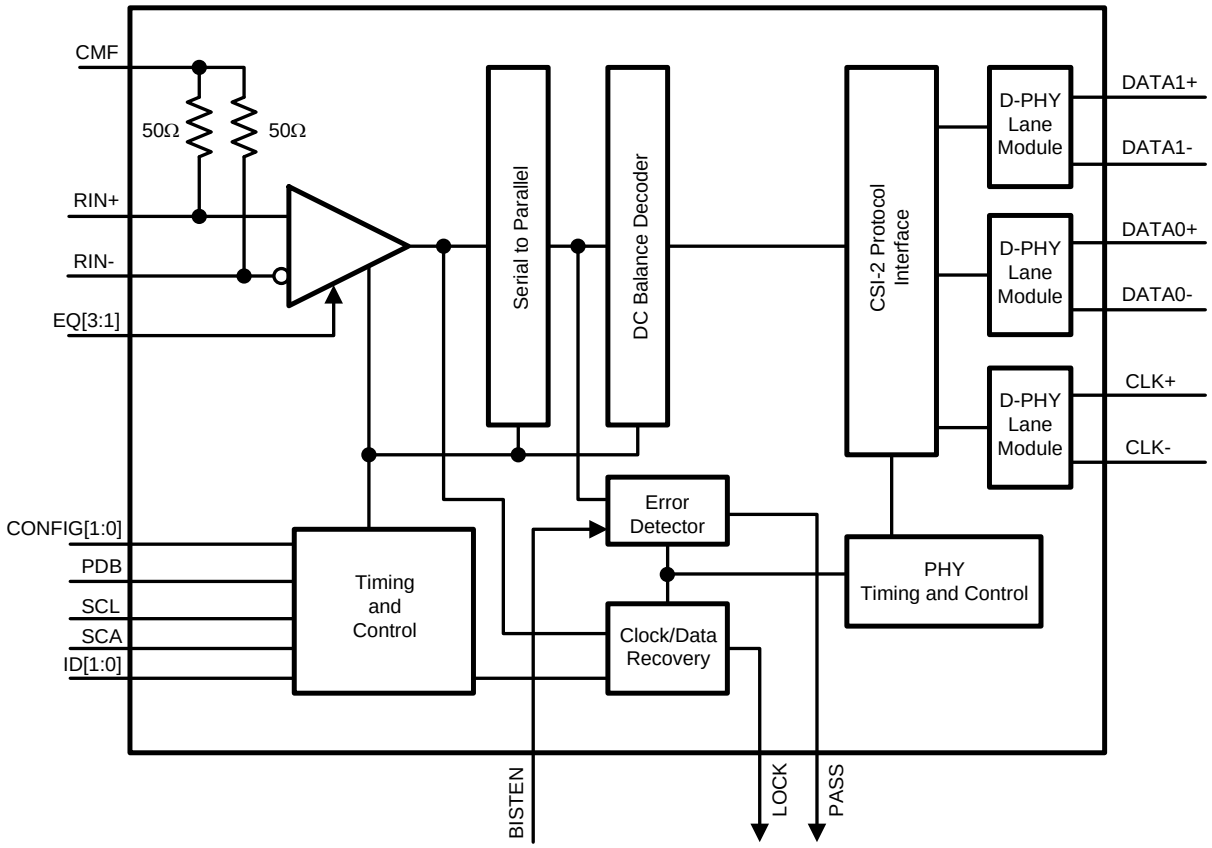
Figure 10. FPD-Link II Serial Stream

The DS90UR910-Q1 supports compatibility to FPD-Link II serializers and FPD-Link III serializers in backward compatible mode as defined in Table 1.

Table 1. DS90UR910-Q1 Configuration Modes

CONFIG1	CONFIG0	MODE	FPD-LINK II COMPATIBILITY	CSI-2 DATA FORMAT
0	0	Normal mode, Control signal filter disabled	DS90UR905Q 24-bit, DS90UR907Q 24-bit, DS90Ux92x Serializers 24-bit	RGB888
0	1	Normal mode, Control signal filter enabled	DS90UR905Q 24-bit, DS90UR907Q 24-bit, DS90Ux92x Serializers 24-bit	RGB888
1	0	Backwards compatible GEN2	DS90UR241Q 18-bit, DS99R421Q 18-bit	RGB888
1	1	Backwards compatible GEN1	DS90C241Q 18-bit	RGB888

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Receive Equalization

The input equalizer of the DS90UR910-Q1 is designed to compensate the attenuation distortion results from cable of different length or wire gauge. The equalizer gain setting is controlled by the control pins EQ[3:1] or through register programming. Users can optimize the equalizer's gain setting along with the de-emphasis level of the DS90UR90xQ to achieve the optimum jitter performance.

Note this function cannot be seen at the RIN± input but can be observed at the serial test port (CMLOUT±) enabled through the serial bus control registers. The equalization feature may be controlled by the external pin or by register.

Table 2. Receiver Equalization Configuration

INPUTS EQ[3:1]			EQ BOOST
EQ3	EQ2	EQ1	
0	0	1	Approximately 3 dB
0	1	0	Approximately 4.5 dB
0	1	1	Approximately 6 dB
1	0	0	Approximately 7.5 dB
1	0	1	Approximately 9 dB
1	1	0	Approximately 10.5 dB
1	1	1	Approximately 12 dB
0	0	0	See(1)

(1) Default Setting is EQ = Off

7.3.2 CSI-2 Interface

The DS90UR910-Q1 (in default mode) takes the RGB data bits R[7:0], G[7:0] and B[7:0] defined in the 24-bit serializer pinout and directly maps to the RGB888 color space in the data frame. The DS90UR910-Q1 follows the general frame format (see Figure 11). Upon the end of the vertical sync pulse (VS), the DS90UR910-Q1 generates the frame end and frame start synchronization packets within the vertical blanking period. The timing of the frame start does not reflect the timing of the VS signal.

Upon the rising edge of the DE signal, each active line is output in a long data packet with the RGB888 data format. At the end of each packet, the data lanes DATA0± and DATA1± return to the LP-11 state, while the clock lane CLK± continue outputting the high-speed clock.

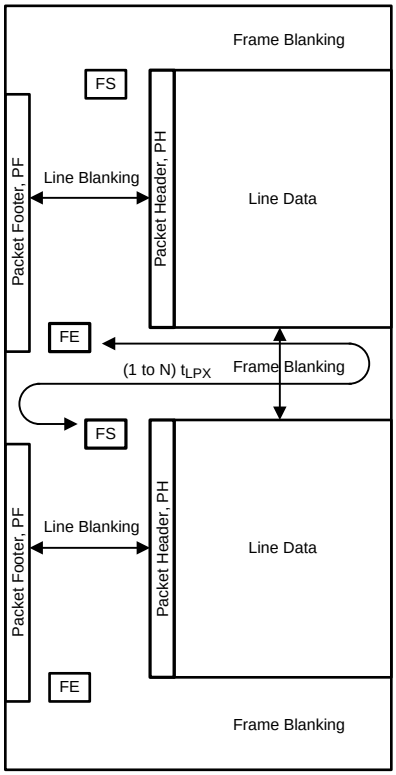


Figure 11. General Frame Format

7.3.3 High-Speed Clock and Data

The high-speed clock and data outputs are source synchronous interface. The half rate clock at CLK± is derived from the pixel clock sourced by the clock or data recovery circuit of the DS90UR910-Q1. The clock frequency is 6 times the pixel clock frequency. The 24-bit recovered RGB data is serialized and output at the 2 high-speed data lanes DATA0± and DATA1± in according to the CSI-2 protocol. The data rate of each lane is 12 times the pixel clock. As an example, at a pixel clock of 75 MHz, the CLK± runs at 450 MHz, and the data lanes run at 900 Mb/s.

The half-rate clock maintains a quadrature phase relationship to the data signals and allows receiver to sample data at the rising and falling edges of the clock. Figure 3 shows the timing relationship of the clock and data lines. The DS90UR910-Q1 supports continuous high-speed clock.

High-speed data are sent out at DATA0± and DATA1± in bursts. In between data bursts, the data lanes return to low power states in according to protocol defined in D-PHY standard. The rising edge of the differential clock (CLK+ – CLK–) is sent during the first payload bit of a transmission burst in the data lanes.

The DS90UR910-Q1 recovers the data bits R[7:0], G[7:0], B[7:0], VS, HS and DE from the serial FPD-Link II bit stream at RIN±. During the vertical blanking period (VS goes low), it sends the short frame end packet, followed by a short frame start packet. User can program the time between frame end to frame start packets from 0 to (2^{16}–1) in units of 8 × pclk_period / 3.

7.3.4 Data Frame RGB Mapping

Table 3 shows the pixel data R[7:0], G[7:0 and B[7:0] defined in DS90UR90xQ and DS90Ux92x serializers pinout, which are recovered by the DS90UR910-Q1 and output in RGB888 format (data type 0x24) at the CSI-2 interface.

Table 3. CSI-2 RGB888 Data Format With FPD-Link II Serializer (24-bit Mode)

FPD-LINK II (24-BIT) PIN NAME	RGB888 DATA BITS
R[0]	R[0]
R[1]	R[1]
R[2]	R[2]
R[3]	R[3]
R[4]	R[4]
R[5]	R[5]
R[6]	R[6]
R[7]	R[7]
G[0]	G[0]
G[1]	G[1]
G[2]	G[2]
G[3]	G[3]
G[4]	G[4]
G[5]	G[5]
G[6]	G[6]
G[7]	G[7]
B[0]	B[0]
B[1]	B[1]
B[2]	B[2]
B[3]	B[3]
B[4]	B[4]
B[5]	B[5]
B[6]	B[6]
B[7]	B[7]
HS	—
VS	—
DE	—

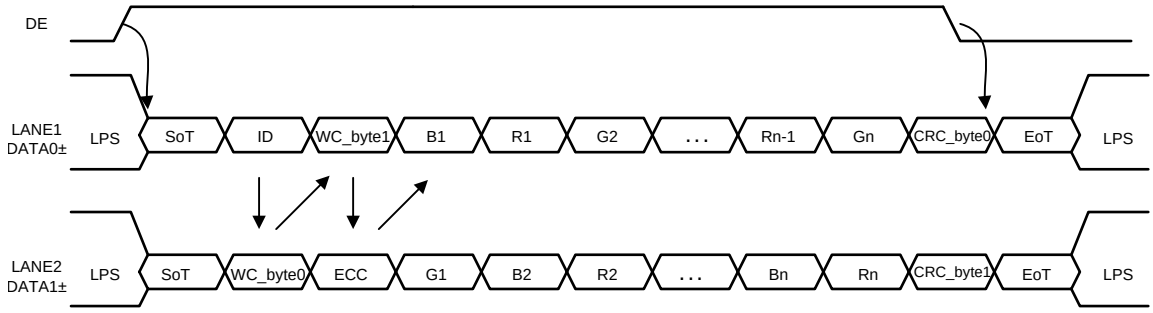


Figure 12. DATA0± and DATA1± Packet Format in According to CSI-2 Protocol for RGB888

Table 4. CSI-2 Data Format With FPD-Link II Serializers (18-Bit Mode)

FPD-LINK II (18-BIT) PIN NAME	RGB DATA BITS	CSI-2 RGB888 DATA BITS
—	—	R[0]
—	—	R[1]
DIN[0]	R[0]	R[2]
DIN[1]	R[1]	R[3]
DIN[2]	R[2]	R[4]
DIN[3]	R[3]	R[5]
DIN[4]	R[4]	R[6]
DIN[5]	R[5]	R[7]
—	—	G[0]
—	—	G[1]
DIN[6]	G[0]	G[2]
DIN[7]	G[1]	G[3]
DIN[8]	G[2]	G[4]
DIN[9]	G[3]	G[5]
DIN[10]	G[4]	G[6]
DIN[11]	G[5]	G[7]
—	—	B[0]
—	—	B[1]
DIN[12]	B[0]	B[2]
DIN[13]	B[1]	B[3]
DIN[14]	B[2]	B[4]
DIN[15]	B[3]	B[5]
DIN[16]	B[4]	B[6]
DIN[17]	B[5]	B[7]
DIN[18]	HS	—
DIN[19]	VS	—
DIN[20]	DE	—

7.3.5 Display Timing Requirements

Table 5 shows the supported display resolutions for the DS90UR910-Q1. The display timings assume an estimated overall blanking rate of 1.2. The DS90UR910-Q1 automatically detects the incoming data rate by from the frame rate (by measuring VS). This timing is then mapped into a look up table. The lookup table is used for any pixel rate of PCLK from 10 MHz to 65 MHz. The limitation that it assumes the frame rate is 60 fps and 30 fps. An override option is available to set each of the parameter individually for a data rate that is not listed in the table. Option is programmed through CCI. Operation of frequencies above 65 MHz require additional I2C or CCI programming of CSI_TIMING registers.

Table 5. DS90UR910-Q1 Supported Resolution and Refresh Rates WITH Expected Blanking Period

RESOLUTION	HACTIVE (PIXELS)	HBLANK (PIXELS)	HTOTAL (PIXELS)	VACTIVE (LINES)	VBLANK (LINES)	VTOTAL (LINES)	FRAME SIZE (PIXELS)	REFRESH (Hz)	PCLK (MHz)
400 × 240	400	40	440	240	5	245	107800	60	6.468
640 × 240	640	40	680	240	5	245	166600	60	9.996
800 × 480	800	40	840	480	5	485	407400	60	24.444
1280 × 480	1280	40	1320	480	5	485	640200	60	38.412
640 × 480	640	144	784	480	29	509	399056	60	23.94336
800 × 600	800	256	1056	600	28	628	663168	60	39.79008
960 × 160	960	40	1000	160	5	165	165000	60	9.9
640 × 160	640	40	680	160	5	165	112200	60	6.732
480 × 240	480	96	576	240	24	264	152064	60	9.12384

Table 5. DS90UR910-Q1 Supported Resolution and Refresh Rates WITH Expected Blanking Period (continued)

RESOLUTION	HACTIVE (PIXELS)	HBLANK (PIXELS)	HTOTAL (PIXELS)	VACTIVE (LINES)	VBLANK (LINES)	VTOTAL (LINES)	FRAME SIZE (PIXELS)	REFRESH (Hz)	PCLK (MHz)
800 × 480	800	160	960	480	48	528	506880	60	30.4128
1280 × 480	1280	256	1536	480	48	528	811008	60	48.66048
960 × 540	960	192	1152	540	54	594	684288	60	41.05728
1440 × 540	1440	288	1728	540	54	594	1026432	60	61.58592
1000 × 600	1000	200	1200	600	60	660	792000	60	47.52
640 × 480	640	160	800	480	45	525	420000	60	25.2
800 × 600	800	256	1056	600	28	628	663168	60	39.79008
1024 × 768	1024	320	1344	768	38	806	1083264	60	64.99584
1440 × 550	1440	144	1584	550	55	605	958320	60	57.4992
800 × 480	800	256	1056	480	45	525	554400	60	33.264
800 × 480	800	256	1056	480	45	525	554400	30	16.632
1024 × 480	1024	52	1076	480	24	504	542304	60	32.53824
1024 × 480	1024	52	1076	480	24	504	542304	30	16.26912
1024 × 480	1024	100	1124	480	48	528	593472	60	35.60832
1024 × 480	1024	100	1124	480	48	528	593472	30	17.80416
1440 × 550	1440	154	1594	550	55	605	964370	60	57.8622
1440 × 550	1440	154	1594	550	55	605	964370	30	28.9311

7.4 Device Functional Modes

7.4.1 Ultra-Low Power State

DS90UR910-Q1 D-PHY lanes enters ULPS mode upon software standby mode through Camera Control Interface (CCI) generated by application processor. When ULPS is entered, all lanes including the clock and data lanes are put in ULPS according to the MIPI D-PHY protocol. D-PHY can reduce power consumption by entering ULPS mode.

Ultra-low power state entry command is sent after an escape mode entry command through CCI, and then lane shall enter the Ultra-Low Power State (ULPS). When ULPS is entered, all lanes including the clock and data lanes are put in ULPS according to the MIPI DPHY protocol. Typically an ULPS entry command is used but other sequences can be used also. ULPS is exited by means of a mark-1 state with a length TWAKEUP followed by a stop state.

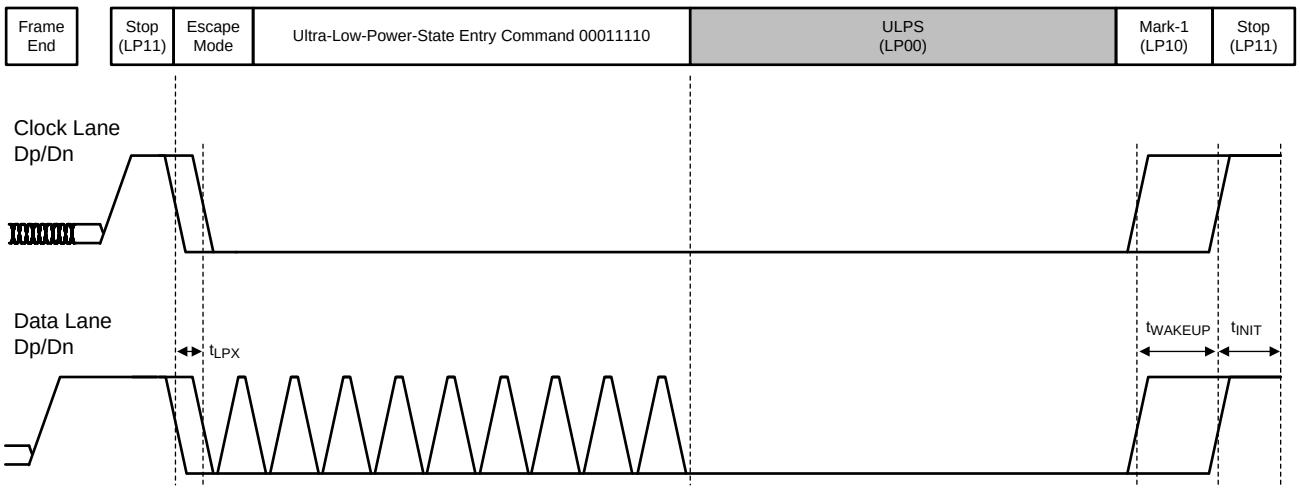


Figure 13. Ultra-Low Power State

Device Functional Modes (continued)

7.4.2 Non-Continuous or Continuous Clock

DS90UR910-Q1 D-PHY supports continuous clock mode and non-continuous clock mode. Default mode is non-continuous clock mode, where the clock lane enters in LP mode between the transmissions of data packets. Non-continuous clock mode is only non-continuous during the vertical blanking period for lower PCLK rates. For higher PCLK rates, the clock is non-continuous between line and frame packets. Operating modes are configurable through CCI.

Clock lane enters LP11 during horizontal blanking if the horizontal blanking period is longer than the overhead time to start or stop the clock lane. There is auto-detection of the length of the horizontal blank period. The threshold is 70 PCLK cycles. Register bit available to disable off the non-continuous clock mode.

7.5 Programming

7.5.1 Serial Control Bus (CCI or I2C)

The DS90UR910-Q1 can be configured by the use of the CCI or I2C as defined by MIPI, which is a bi-directional, half-duplex, serial control bus consists of SCL and SDA. The SDA is the bi-directional data line. The SCL is the serial clock line. Both SCL and SDA are driven by open drain drivers and required external pullup resistors to VDDIO. The signals are either driven low or pulled high.

The DS90UR910-Q1 is a CCI slave. ID[1:0] pins select one of the four CCI slave addresses (see Table 6).

Table 6. CCI or I2C Slave Address

ID[1]	ID[0]	7-BIT SLAVE ADDRESS	8-BIT SLAVE ADDRESS (0 APPENDED WRITE)
0	0	011 1100 (0x3C'h)	0111 1000 (0x78'h)
0	1	011 1101 (0x3D'h)	0111 1010 (0x7A'h)
1	0	011 0110 (0x36'h)	0110 1100 (0x6C'h)
1	1	011 0111 (0x37'h)	0110 1110 (0x6E'h)

The serial bus protocol is initiated by START or START-REPEATED, and terminated by STOP condition. A START occurs when SDA transitions low while SCL is high. A STOP occurs when SDA transitions high when SCL is high (see Figure 14).

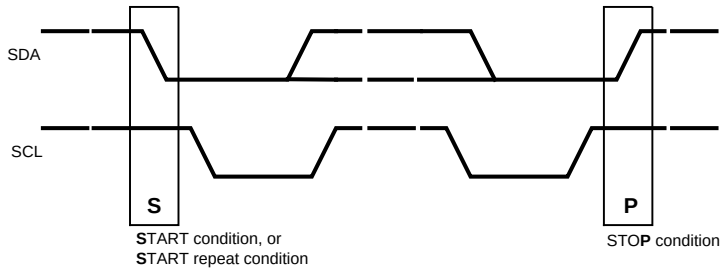


Figure 14. START and STOP Conditions

To communicate with a remote device, the host controller (master) sends the 7-bit slave address followed by a write-bit (0), and listens for a response from the slave. This response is referred to as an acknowledge bit. If the slave on the bus is addressed correctly, it acknowledges the master by driving the SDA low (ACK). If the address does not match the slave address of the device, it negative acknowledges the master by letting SDA be pulled high (NACK). In a write operation from master to slave, the master sends the 8-bit index address of the register that it wants to access. After the slave ACKs, the master sends the 8-bit data byte. The slave ACKs after each data byte is successfully received and is ready to receive another byte into the next sequential index location. At the end of the data transfer, the master ends the transaction with a STOP condition.

In a read operation, the master first sends the 8-bit index address of the register that it wants to access. After receiving an ACK from the slave, it initiates a START-REPEAT condition, sends the 7-bit slave address followed by the read-bit (1). The slave ACKs and sends out the 8-bit data byte. The master acknowledges an ACK when another data byte is sent to the next sequential index address. The master acknowledges an NACK when no more data byte is sent, and ends the transaction with a STOP condition.

The CCI interface of the DS90UR910-Q1 supports standard mode (<100 kHz) or fast mode (<400 kHz) with 8-bit index addressing and 8-bit data transfer. It supports the following read or write operations between the DS90UR910-Q1 and the CCI master:

- Single read from random location
- Single read from current location
- Sequential read starting from a random location
- Sequential read starting from the current location
- Single write to a random location
- Sequential write starting from a random location

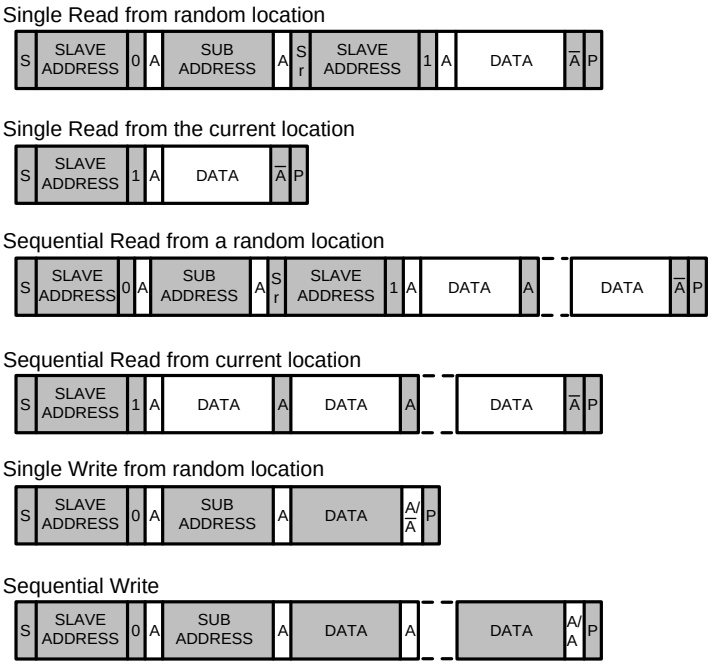


Figure 15. I2C or CCI Read or Write Operations

Table 7. Serial Bus Control Registers

ADD (HEX)	REGISTER NAME	BIT(S)	R/W	DEFAULT	FIELD	DESCRIPTION
0x00	I2C_SLAVE_ID	7:1	R/W	0x30	DEVID	I2C slave ID
		0	R/W	0	DEVID_EN	0: Address from ID[X] Pin 1: Address from Register
0x01	CONFIG1	7	R/W	0	LFMODE	If pin over write bit is one, controls the LF Mode. Debug only
		6	R	0	Reserved	Reserved
		5	R/W	0	SLEW	Control slew rate of LOCK, PASS and GPIO 0: Normal slew 1: Increased Slew
		4	R	0	Reserved	Reserved
		3:2	R/W	0	MODE	00: Normal Mode, Control Signal Filter Disabled 01: Normal Mode, Control Signal Filter Enabled 10: Backwards Compatible (GEN2) 11: Backwards Compatible (GEN1) (See Table 1)
		1	R/W	0	SLEEP	Note – not the same function as PowerDown (PDB pin) 0: Normal mode 1: Sleep Mode – Register settings retained.
		0	R/W	0	USEREG	0: Configurations set from control pins / STRAP pins 1: Override EQ and CONFIG strapped control inputs with register settings
0x02	CONFIG2	7:6	R	0	Reserved	Reserved
		5:4	R/W	00	OMAP	6 bits to 8 bits color mapping 00: bit 4, 5 repeated on LSB 01: LSB zero if all data is zero 10: LSB zero 11: LSB zero
		3	R	0	Reserved	Reserved
		2:0	R/W	3'b100	Reserved	Reserved
0x03	EQ Control	7:4	R/W	000	EQ	Override EQ pin input if USEREG bit set
		3:0	R	0	Reserved	Reserved
0x04	CMLOUT Config	7	R/W	0	CMLOUT	Loop through enable 0: Output CMLOUT± = disabled 1: Output CMLOUT± = enabled
		6:0	R/W	0	VOD	VOD control 000000: min VOD 000001: 000011: 000111: 001111: 011111: 111111: max VOD
0x05→0x10	NA	7:0	R/W	0	Reserved	Reserved

Table 7. Serial Bus Control Registers (continued)

ADD (HEX)	REGISTER NAME	BIT(S)	R/W	DEFAULT	FIELD	DESCRIPTION
0x11	CSI config	7	R/W	0	CCI_INV_VS	0: VS is active low pulse 1: VS is active high pulse
		6	R/W	0	CCI_CONT_CLOCK	0: CSI-2 non-continuous clock 1: CSI-2 continuous clock
		5:2	R/W	0	Reserved	Reserved
		1	R/W	0	CCI_EXTERNAL_TIMING	0: Use computed DPHY timing based on frame length 1: Use manual override values for DPHY timing
		0	R/W	0	CCI_INV_DE	0: DE is active low pulse 1: DE is active high pulse
0x12	CSI_FRM_GAP_0	7:0	R/W	0	CSI_FRM_GAP_0	Defined the delay between the start frame and end frame packet (lower byte)
0x13	CSI_FRM_GAP_1	7:0	R/W	0	CSI_FRM_GAP_1	Defined the delay between the start frame and end frame packet (upper byte)
0x14	CSI_TIMING0	7:5		0	Reserved	Reserved
		4:0	R/W	0	TCLK_PREPARE	Defines the Tclk_prepare parameter if CCI_EXTERNAL_TIMING is set
0x15	CSI_TIMING1	7:3	R/W	0	TCLK_ZERO	Defines the Tclk_zero parameter if CCI_EXTERNAL_TIMING is set
		2:0	R/W	0	TCLK_TRAIL	Defines the Tclk_trail parameter if CCI_EXTERNAL_TIMING is set
0x16	CSI_TIMING2	7:4	R/W	0	TCLK_POST	Defines the Tclk_post parameter if CCI_EXTERNAL_TIMING is set
		3:0	R/W	0	THS_ZERO	Defines the Ths_zero parameter if CCI_EXTERNAL_TIMING is set
0x17	CSI_TIMING3	7	R/W	0	Reserved	Reserved
		6:4	R/W	0	THS_TRAIL	Defines the Ths_trail parameter if CCI_EXTERNAL_TIMING is set
		3:0	R/W	0	THS_EXIT	Defines the Ths_exit parameter if CCI_EXTERNAL_TIMING is set
0x18	CSI_TIMING4	7:3	R/W	0	THS_PREPARE	Defines the Ths_prepare parameter if CCI_EXTERNAL_TIMING is set
		2:0	R/W	0	TLPX	Defines the Ths_exit parameter if CCI_EXTERNAL_TIMING is set
0x19	CSI_ULPS	7:3	R/W	0	Reserved	Reserved
		1	R/W	0	ULPS_MODE	0: In ULPS mode, data lane off 1: In ULPS mode, data lane off, clock lane off, x6 PLL off
		0	R/W	0	ULPS_EN	0: Disable UPLS mode 1: Enable ULPS mode
0x1A	NA	7:0	R/W	0	Reserved	Reserved
0x1B	CSI_UNH1	7	R/W	0	Reserved	Reserved
		6:5	R/W	0x1	ACT_VERT_MSB	MSBs of active vertical UNH image
		4:3	R/W	0x2	TOT_VERT_MSB	MSBs of total vertical UNH image
		2:1	R/W	0	Reserved	Reserved
		0	R/W	0	PATGEN	0: Normal mode 1: Enable pattern generator mode
0x1C	CSI_UNH2	7:0	R/W	0x0F	TOT_VERT_LSB	LSBs of total vertical UNH image
0x1D	CSI_UNH3	7:0	R/W	0xDF	ACT_VERT_LSB	LSBs of active vertical UNH image

Table 7. Serial Bus Control Registers (continued)

ADD (HEX)	REGISTER NAME	BIT(S)	R/W	DEFAULT	FIELD	DESCRIPTION
0x1E	CSI_UNH4	7:6	R/W	0	Reserved	Reserved
		5:3	R/W	0x4	ACT_HORIZ_MSB	MSBs of active horizontal UNH image
		2:0	R/W	0x5	TOT_HORIZ_MSB	MSBs of total horizontal UNH image
0x1F	CSI_UNH5	7:0	R/W	0xFF	ACT_HORIZ_LSB	LSBs of active horizontal UNH image
0x20	CSI_UNH6	7:0	R/W	0xFF	TOT_HORIZ_LSB	LSBs of total horizontal UNH image
0x21	CSI_UNH7	7:0	R/W	0x09	PORCH_VERT	Vertical porch size UNH image
0x22	CSI_UNH8	7:0	R/W	0x09	SYNC_VERT	Vertical sync size UNH image
0x23	CSI_UNH9	7:0	R/W	0x09	PORCH_HORIZ	Horizontal porch size UNH image
0x24→0x2F	NA	7:0	R/W	0	Reserved	Reserved
0x30	CSI_ID0	7:0	R	0x5F	CID0	Chip ID, character _
0x31	CSI_ID1	7:0	R	0x55	CID1	Chip ID, character *U*
0x32	CSI_ID2	7:0	R	0x52	CID2	Chip ID, character *R*
0x33	CSI_ID3	7:0	R	0x39	CID3	Chip ID, character *9*
0x33	CSI_ID4	7:0	R	0x31	CID4	Chip ID, character *1*
0x35	CSI_ID5	7:0	R	0x30	CID5	Chip ID, character *0*
0x36	CSI_REVID	7:0	R	0x01	CID5	Revision ID of the design
0x37→0x3A	NA	7:0	R	0	Reserved	Reserved
0x3B	REVID	7:0	R	0x01	REVID	Revision ID of the design
0x3C→0x3F	NA	7:0	R	0	Reserved	Reserved
0x40→0xFF						Address range 0x00 to 0x3F aliases into the full address space.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DS90UR910-Q1 device recovers data from the FPD-Link II serial bit stream and converts into CSI-2. The recovered data is packetized and serialized over two data lanes strobed by a half-rate serial clock compliant with the MIPI DPHY and CSI-2 specifications, each running up to 900 Mbps. The FPD-Link II receiver supports pixel clocks of up to 75 MHz. The CSI-2 output serial bus greatly reduces the interconnect and signal count to a graphic processing unit (GPU) and eases system designs for video streams from multiple automotive driver assist cameras.

8.2 Typical Application

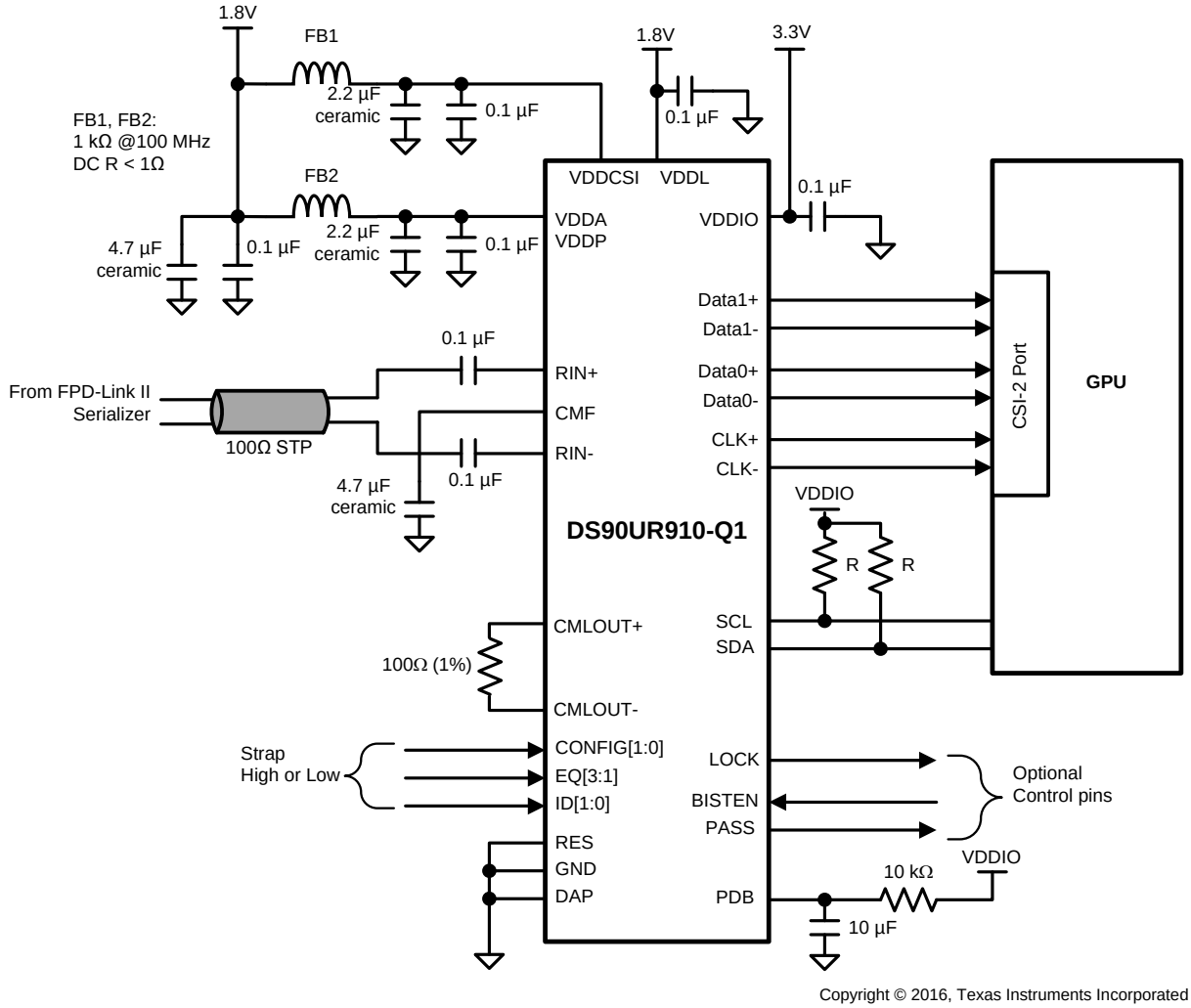


Figure 16. DS90UR910-Q1 Typical Connection Diagram — Pin Control

Typical Application (continued)

8.2.1 Design Requirements

For this typical design application, Table 8 lists the input parameters.

Table 8. Design Parameters

PARAMETER	VALUE
VDDIO	1.8 V or 3.3 V
VDDL, VDDA, VDDP, VDDCSI	1.8 V
AC-coupling capacitor for RIN0± and RIN1±	100 nF

8.2.2 Detailed Design Procedure

Figure 16 shows a typical application of the DS90UR910-Q1 in Pin control mode for a 24-bit Color Display Application. The LVDS signals require 100-nF AC-coupling capacitors to the line. The line driver includes internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, four 0.1-µF capacitors and a 4.7-µF capacitor must be used for local device bypassing. System GPO (General Purpose Output) signals control the PDB and BISTEN pins. The interface to the host is with 1.8-V LVCMOS levels, thus the VDDIO pin is connected also to the 1.8-V rail. The optional I2C or CCI is connected to the Host bus in this example, thus the SCL and SDA pins are using pullup resistors R to VDDIO. A delay cap is placed on the PDB signal to delay the enabling of the device until power is stable.

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC-coupling capacitors must be placed in series in the FPD-Link II signal path as illustrated in Figure 17.

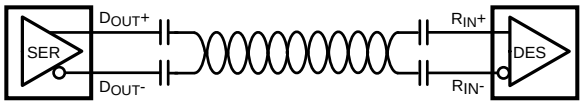


Figure 17. AC-Coupled Connection

For high-speed FPD-Link II transmissions, the smallest available package must be used for the AC coupling capacitor. This helps minimize degradation of signal quality due to package parasitics. The inputs and outputs require 100-nF AC-coupling capacitors to the line.

8.2.3 Application Curves

Figure 18 corresponds to 49-MHz PCLK UNH pattern.

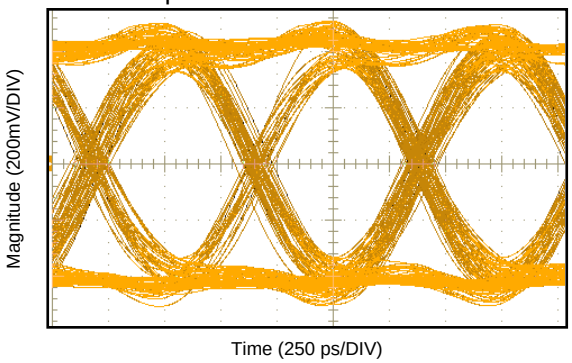


Figure 18. Loop-Through CML Output at 1.372-Gbps Serial Line Rate

9 Power Supply Recommendations

9.1 Power Up Requirements and PDB Pin

The V_{DD} (V_{DDn} and V_{DDIO}) supply ramp must be faster than 1.5 ms with a monotonic rise. If slower than 1.5 ms, then a capacitor on the PDB pin is required to ensure PDB arrives after all the VDD have settled to the recommended operating voltage. When PDB pin is pulled to V_{DDIO}, TI recommends using a 10-kΩ pullup and a >10-µF capacitor to GND to delay the PDB input signal.

10 Layout

10.1 Layout Guidelines

10.1.1 Transmission Media

The serializer or deserializer chipset is intended to be used in a point-to-point configuration, through a PCB trace, or through twisted pair cable. The serializer and deserializer provide internal terminations providing a clean signaling environment. The interconnect for LVDS must present a differential impedance of 100 Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Shielded or un-shielded cables may be used depending upon the noise environment and application requirements.

10.1.2 PCB Layout and Power System Considerations

Circuit board layout and stack-up for the LVDS serializer or deserializer devices must be designed to provide low-noise power feed to the device. Good layout practice also separates high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power or ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors must include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 µF to 0.1 µF. Tantalum capacitors may be in the 2.2-µF to 10-µF range. Voltage rating of the tantalum capacitors must be at least 5× the power supply voltage being used.

TI recommends surface-mount capacitors due to their small parasitics. When using multiple capacitors per supply pin, place the smaller value closer to the pin. TI recommends a large bulk capacitor at the point of power entry. This is typically in the 50-µF to 100-µF range and smooths low frequency switching noise. TI also recommends connecting power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor increases the inductance of the path.

TI recommends a small body size X7R chip capacitor, such as 0603, for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different circuit sections. Separate PCB planes are typically not required. Pin description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Place LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely-coupled differential lines of 100 Ω are typical for LVDS interconnect. The closely coupled lines help ensure that coupled noise appears as common-mode and thus is rejected by the receivers. The tightly coupled lines also radiate less.

Information on the WQFN style package is provided in *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401).

Layout Guidelines (continued)

10.1.3 CSI-2 Guidelines

1. CSI0_D × P/N and CSI1_D × P/N pairs must be routed with controlled 100-Ω differential impedance (± 20%) or 50-Ω single-ended impedance (±15%)
2. Keep away from other high-speed signals
3. Keep length difference between a differential pair to 5 mils maximum
4. Length matching must be near the location of mismatch.
5. Match trace lengths between pairs to be <25 mils.
6. Each pair must be separated at least by 3 times the signal trace width
7. The use of bends in differential traces must be kept to a minimum. When bends are used, the number of left and right bends must be as equal as possible and the angle of the bend must be ≥135°. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI.
8. Route all differential pairs on the same layer
9. The number of vias must be kept to a minimum. TI recommends keeping the via count to 2 or less.
10. Keep traces on layers adjacent to ground plane
11. Do NOT route differential pairs over any plane split
12. Adding test points cause impedance discontinuity and therefore negatively impact signal performance. If test points are used, they must be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair

10.1.4 LVDS Interconnect Guidelines

See *Channel-Link PCB and Interconnect Design-In Guidelines* (SNLA008) and *Transmission Line RAPIDESIGNER© Operation and Applications Guide* (SNLA035) for full details.

- Use 100-Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of vias and skew within the pair
- Use differential connectors when operating above 500-Mbps line speed
- Maintain balance of the traces
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the LVDS Owner's Manual (available in PDF format from the Texas Instruments web site at: www.ti.com/lvds).

10.2 Layout Example

Figure 19 is derived from a layout design of the DS90UR910-Q1 EVM. This graphic and additional layout description are used to demonstrate both proper routing and proper solder techniques when designing in the deserializer.

Layout Example (continued)

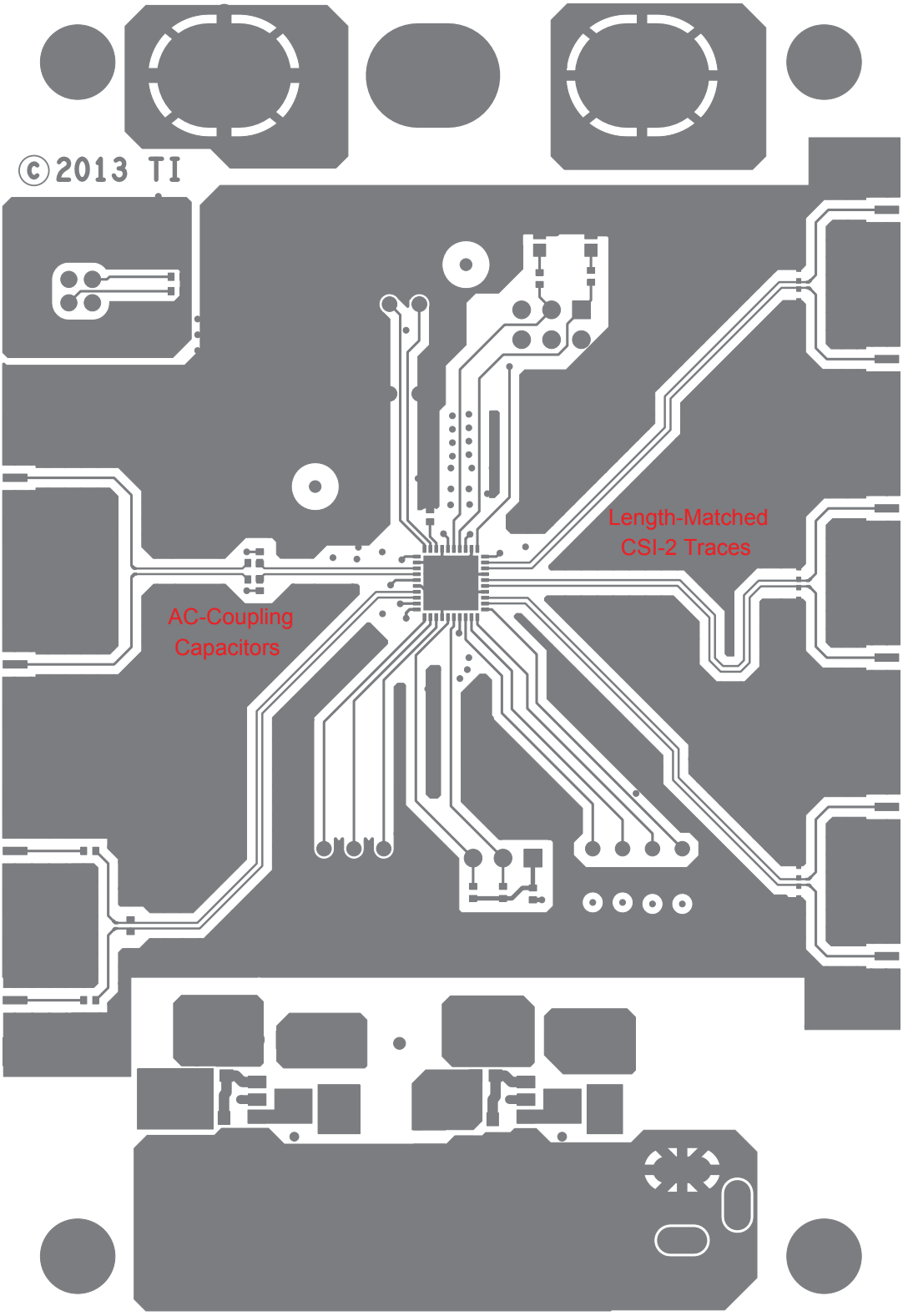


Figure 19. DS90UR910-Q1 Deserializer Example Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Absolute Maximum Ratings for Soldering* (SNOA549)
- *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401)
- *Channel-Link PCB and Interconnect Design-In Guidelines* (SNLA008)
- *Transmission Line RAPIDESIGNER© Operation and Applications Guide* (SNLA035)
- *DS90UR90Q-Q1 5- to 65-MHz, 24-bit Color FPD-Link II Serializer and Deserializer* (SNLS313)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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