

DLPR910 Configuration PROM

1 Features

- Pre-Programmed Xilinx® PROM Configures the DLPC910ZXR
- Data Transfer Up to 33 Mbps
- I/O Pins Compatible With 1.8 V to 3.3 V
- 1.8-V Core Supply Voltage
- –40°C to 85°C Operating Temperature Range

2 Applications

- Lithography
 - Direct Imaging
 - Flat Panel Display
 - Printed Circuit Board Manufacturing
- Industrial
 - 3D Printing
 - 3D Scanners for Machine Vision
 - Quality Control
- Displays
 - 3D Imaging
 - Intelligent and Adaptive Lighting
 - Augmented Reality and Information Overlay

3 Description

The DLPR910 device is a programmed PROM used for properly configuring the DLPC910, which supports reliable operation of the DLP9000X digital micromirror device (DMD) and the DLP6500 family of DMDs. The DLPR910 configuration enables the DLPC910 to operate the DMDs at a pixel data rate greater than 61 Gigabits per second (Gbps) for the DLP9000X and up to 24 Gbps for the DLP6500 family, with the option for random row addressing and Load4 capabilities.

The DLPR910 device is part of a multiple component chipset in the DLP® Advanced Light Control portfolio. A dedicated chipset provides developers easier access to the DMD as well as high speed, independent micromirror control.

The DLPC910 configuration program is only available within the DLPR910. The DLPR910 requires that it be used in conjunction with the DLPC910 and the DLP9000X DMD or the DLP6500 family of DMDs for reliable function and operation of the chipset.

For complete electrical and mechanical specifications of the DLPR910, see the XCF16P product specification at www.xilinx.com.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLPR910	DSBGA (48)	8.00 mm × 9.00 mm × 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Figure 1. Typical Application Diagram

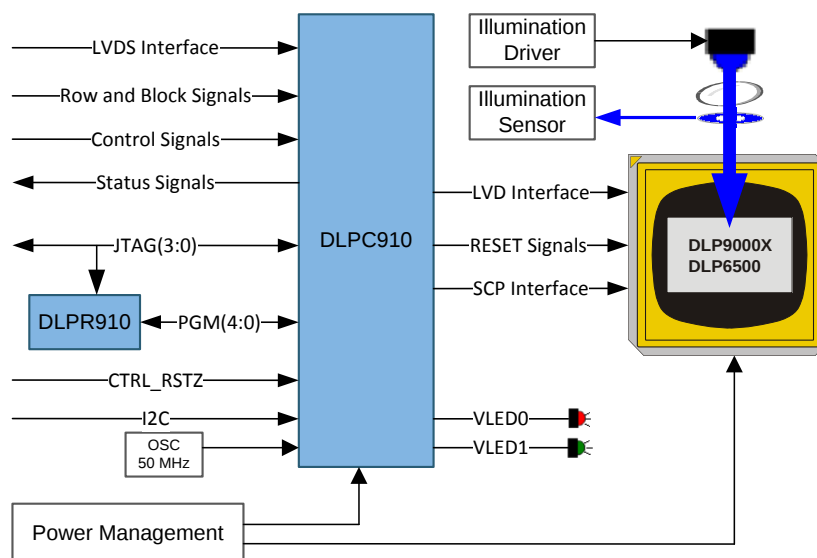


Table of Contents

1 Features	1	7.3 Feature Description.....	7
2 Applications	1	7.4 Device Functional Modes.....	8
3 Description	1	8 Application and Implementation	10
4 Revision History	2	8.1 Application Information.....	10
5 Pin Configuration and Functions	3	8.2 Typical Application	10
6 Specifications	5	9 Power Supply Recommendations	11
6.1 Absolute Maximum Ratings	5	10 Layout	11
6.2 ESD Ratings.....	5	10.1 Layout Guidelines	11
6.3 Recommended Operating Conditions.....	5	11 Device and Documentation Support	12
6.4 Thermal Information	5	11.1 Device Support.....	12
6.5 Electrical Characteristics.....	5	11.2 Documentation Support	13
6.6 Supply Voltage Requirements for Power-On Reset and Power-Down	6	11.3 Community Resources.....	13
6.7 Timing Requirements	6	11.4 Trademarks	13
7 Detailed Description	7	11.5 Electrostatic Discharge Caution.....	13
7.1 Overview	7	11.6 Glossary	13
7.2 Functional Block Diagram	7	12 Mechanical, Packaging, and Orderable Information	13

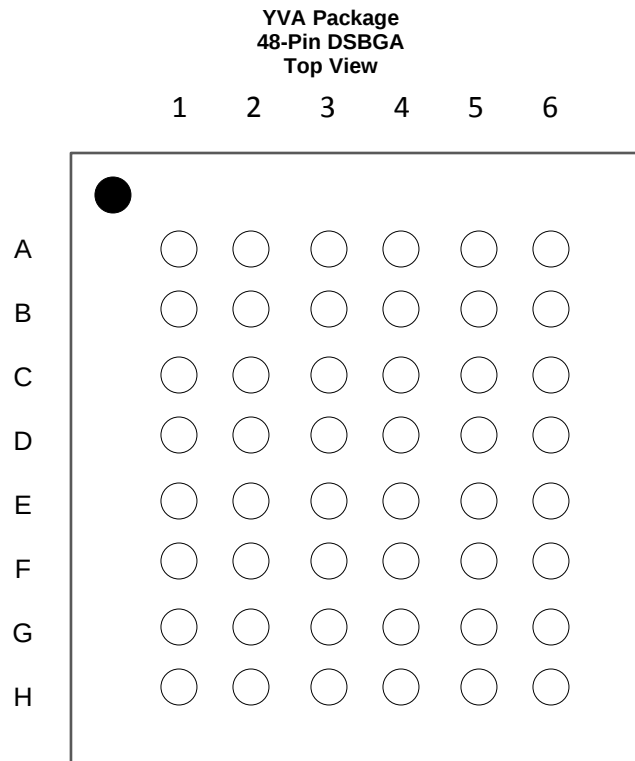
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2015) to Revision B	Page
• Updated Description to include additional supported DMD.....	1
• Update document to include additional supported DMD in Detailed Description	7
• Added typical application schematic for newly supported DMD in Typical Application	10
• Updated Device Markings	12

Changes from Original (September 2015) to Revision A	Page
• Updated device from Product Preview to Production Data	1

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
GND	A1	G	Ground
GND	A2	G	Ground
OE/ $\overline{\text{RESET}}$	A3	I/O	Output Enable/ $\overline{\text{RESET}}$ (Open-Drain I/O). When Low, this input holds the address counter reset and the DATA and CLKOUT outputs are placed in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM completes the internal power-on reset sequence. Polarity is not programmable. Pin must be pulled High using an external 4.7-kΩ pull-up to V_{CCO}.
DNC	A4	—	Do Not Connect. Leave unconnected.
D6	A5	—	Do Not Connect. Leave unconnected.
D7	A6	—	Do Not Connect. Leave unconnected.
V _{CCINT}	B1	P	Positive 1.8-V supply voltage for internal logic.
V _{CCO}	B2	P	Positive 3.3-V and 1.8-V supply voltage connected to the output voltage drivers and internal buffers.
CLK	B3	I	Configuration clock input. Each rising edge on the CLK input increments the internal address counter. Pin must be pulled High and Low using an external 100-Ω pull-up to V_{CCO} and an external 100-Ω pull-down to Ground. Place resistors close to pin.
$\overline{\text{CE}}$	B4	I	Chip Enable Input. When $\overline{\text{CE}}$ is High, the device is put into low-power standby mode, the address counter is reset, and the DATA and CLKOUT outputs are placed in a high impedance state.
D5	B5	—	Do Not Connect. Leave unconnected.
GND	B6	G	Ground

(1) P = Power
G = Ground
I = Input
O = Output

Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
BUSY	C1	—	Do Not Connect. Leave unconnected.
CLKOUT	C2	—	Do Not Connect. Leave unconnected.
DNC	C3	—	Do Not Connect. Leave unconnected.
DNC	C4	—	Do Not Connect. Leave unconnected.
D4	C5	—	Do Not Connect. Leave unconnected.
V _{CCO}	C6	P	Positive 3.3-V and 1.8-V supply voltage connected to the output voltage drivers and internal buffers.
($\overline{\text{CF}}$)	D1	I	Configuration pin. The ($\overline{\text{CF}}$) pin must be pulled High using an external 4.7-kΩ pull-up to V_{CCO}. Selects serial mode configuration.
($\overline{\text{CEO}}$)	D2	—	Do Not Connect. Leave unconnected.
DNC	D3	—	Do Not Connect. Leave unconnected.
DNC	D4	—	Do Not Connect. Leave unconnected.
D3	D5	—	Do Not Connect. Leave unconnected.
V _{CCO}	D6	P	Positive 3.3-V and 1.8-V supply voltage connected to the output voltage drivers and internal buffers.
V _{CCINT}	E1	P	Positive 1.8-V supply voltage for internal logic.
TMS	E2	I	JTAG Mode Select Input. TMS has an internal 50-k Ω resistive pull-up to V _{CCJ} .
DNC	E3	—	Do Not Connect. Leave unconnected.
DNC	E4	—	Do Not Connect. Leave unconnected.
D2	E5	—	Do Not Connect. Leave unconnected.
TDO	E6	O	JTAG Serial Data Output. TDO has an internal 50-k Ω resistive pull-up to V _{CCJ} .
GND	F1	G	Ground
DNC	F2	—	Do Not Connect. Leave unconnected.
DNC	F3	—	Do Not Connect. Leave unconnected.
DNC	F4	—	Do Not Connect. Leave unconnected.
GND	F5	G	Ground
GND	F6	G	Ground
TDI	G1	I	JTAG Serial Data Input. TDI has an internal 50k- Ω resistive pull-up to V _{CCJ} .
DNC	G2	—	Do Not Connect. Leave unconnected.
REV_SEL0	G3	I	Revision Select [1:0] Inputs. When the ($\overline{\text{EN_EXT_SEL}}$) is Low, the Revision Select pins are used to select the design revision to be enabled. The Revision Select [1:0] inputs have an internal 50-k Ω resistive pull-up to V _{CCO} . The (REV_SEL0) pin must be pulled Low using an external 10-kΩ pull-down to Ground. The (REV_SEL1) pin must be connected to Ground.
REV_SEL1	G4	I	
V _{CCO}	G5	P	Positive 3.3-V and 1.8-V supply voltage connected to the output voltage drivers and internal buffers.
V _{CCINT}	G6	P	Positive 1.8-V supply voltage for internal logic.
GND	H1	G	Ground
VCCJ	H2	P	Positive 3.3-V JTAG I/O supply voltage connected to the TDO output voltage driver and TCK, TMS and TDI input buffers.
TCK	H3	I	JTAG Clock Input. This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.
($\overline{\text{EN_EXT_SEL}}$)	H4	I	External Selection Input. ($\overline{\text{EN_EXT_SEL}}$) has an internal 50-k Ω resistive pull- up to V _{CCO} . The ($\overline{\text{EN_EXT_SEL}}$) pin must be connected to Ground.
D1	H5	—	Do Not Connect. Leave unconnected.
D0	H6	O	DATA output pin to provide data for configuring the DLPC910 in serial mode.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (see ⁽¹⁾ ⁽²⁾)

			MIN	MAX	UNIT
V _{CCINT}	Internal supply voltage	Relative to ground	–0.5	2.7	V
V _{CCO}	I/O supply voltage	Relative to ground	–0.5	4.0	V
V _{IN}	Input voltage with respect to ground	V _{CCO} < 2.5 V	–0.5	3.6	V
		V _{CCO} ≥ 2.5 V	–0.5	3.6	V
V _{TS}	Voltage applied to high-impedance output	V _{CCO} < 2.5 V	–0.5	3.6	V
		V _{CCO} ≥ 2.5 V	–0.5	3.6	V
T _J	Junction temperature			125	°C
T _{stg}	Storage temperature, ambient		–40	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Maximum DC undershoot below GND must be limited to either 0.5 V or 10 mA. During transitions, the device pins can undershoot to –2 V or overshoot to 7 V, provided this overshoot or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD) ⁽¹⁾	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽²⁾ ⁽³⁾	2000	V

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
- (2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (3) JEDEC Standard JESD22-A114A (C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω).

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _{CCINT}	Internal voltage supply		1.65	1.8	2.0	V
V _{CCO}	Supply voltage for output drivers	3.3-V operation	3.0	3.3	3.6	V
V _{IL}	Low-level input voltage	3.3-V operation	0	–	0.8	V
V _{IH}	High-level input voltage	3.3-V operation	2.0	–	3.6	V
V _O	Output voltage		0	–	V _{CCO}	V
t _{IN}	Input signal transition time (measured between 10% V _{CCO} and 90% V _{CCO})		–	–	500	ns
T _A	Operating ambient temperature		–40	–	85	°C

6.4 Thermal Information

Refer to the XCF16P product specifications at www.xilinx.com.

6.5 Electrical Characteristics

Refer to the XCF16P product specifications at www.xilinx.com.

6.6 Supply Voltage Requirements for Power-On Reset and Power-Down

(see ⁽¹⁾)

		MIN	MAX	UNIT
t_{VCC}	V_{CCINT} rise time from 0 V to nominal voltage ⁽²⁾	0.2	50	ms
V_{CCPOR}	POR threshold for V_{CCINT} supply	0.5	–	V
t_{OER}	$\overline{OE/RESET}$ release delay following POR ⁽³⁾	0.5	30	ms
V_{CCPD}	Power-down threshold for V_{CCINT} supply	–	0.5	V
t_{RST}	Time required to trigger a device reset when the V_{CCINT} supply drops below the maximum V_{CCPD} threshold	10	–	ms

- (1) V_{CCINT} , V_{CCO} , and V_{CCJ} supplies can be applied in any order.
- (2) At power up, the device requires the V_{CCINT} power supply to monotonically rise to the nominal operating voltage within the specified T_{VCC} rise time. If the power supply cannot meet this requirement, then the device might not perform power-on-reset properly. See Figure 6, in the Xilinx XCF16P (v2.18) Product Specification for more information.
- (3) If the V_{CCINT} and V_{CCO} supplies do not reach their respective recommended operating conditions before the $\overline{OE/RESET}$ pin is released, then the configuration data from the PROM is not available at the recommended threshold levels. The configuration sequence must be delayed until both V_{CCINT} and V_{CCO} have reached their recommended operating conditions.

6.7 Timing Requirements

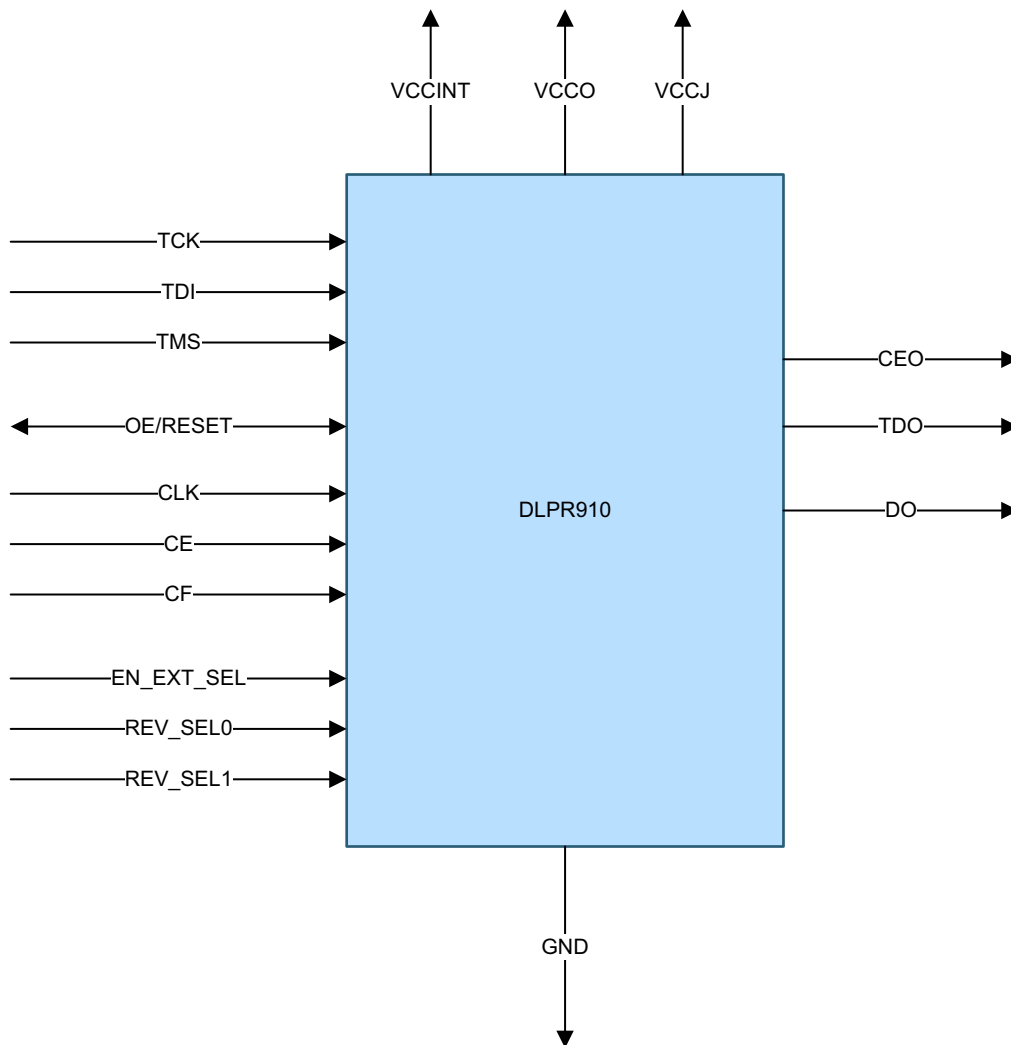
Refer to the XCF16P product specifications at www.xilinx.com.

7 Detailed Description

7.1 Overview

The configuration bit stream stored in the DLPR910 supports reliable operation of the DLPC910 with the DLP9000X DMD or the DLP6500 family of DMDs. The DLPC910 digital controller loads this configuration bit stream from the DLPR910.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Data Interface

7.3.1.1 Data Outputs

The DLPR910 is configured for serial mode operation, where D0 is the data output pin. D0 output pin provides a serial connection to the DLPC910, where the configuration is read out by the DLPC910.

7.3.1.2 Configuration Clock Input

The configuration CLK is connected to the DLPC910 in master mode, where the DLPC910 provides the clock pulses to read the configuration from the DLPR910.

Feature Description (continued)

7.3.1.3 Output Enable and Reset

When the OE/ $\overline{\text{RESET}}$ input is held low, the address counter is reset and the Data and CLKOUT outputs are placed in high-impedance state. **OE/ $\overline{\text{RESET}}$ must be pulled High using an external 4.7-k Ω pull-up to V_{CC0}.**

7.3.1.4 Chip Enable

The $\overline{\text{CE}}$ input is asserted by the DLPC910 to enable the Data and CLKOUT outputs. When $\overline{\text{CE}}$ is held high, the DLPR910 address counter is reset, and the Data and CLKOUT outputs are placed in high-impedance states.

7.3.1.5 Configuration Pulse

The DLPR910 is configured in serial mode when the Configuration Pulse $\overline{\text{CF}}$ is held high and $\overline{\text{CE}}$ and OE are enabled. New data is available a short time after each rising clock edge.

7.3.1.6 Revision Selection

REV_SEL_0, REV_SEL_1, and $\overline{\text{EN_EXT_SEL}}$ signals are used for selecting which revision to be the default. Setting all three signals to GND will default to revision 0 for simple DLPR910 setup.

7.4 Device Functional Modes

To successfully program the DLPC910 upon power-up, the DLPR910 must be configured and connected to the DLPC910 as shown in [Figure 2](#).

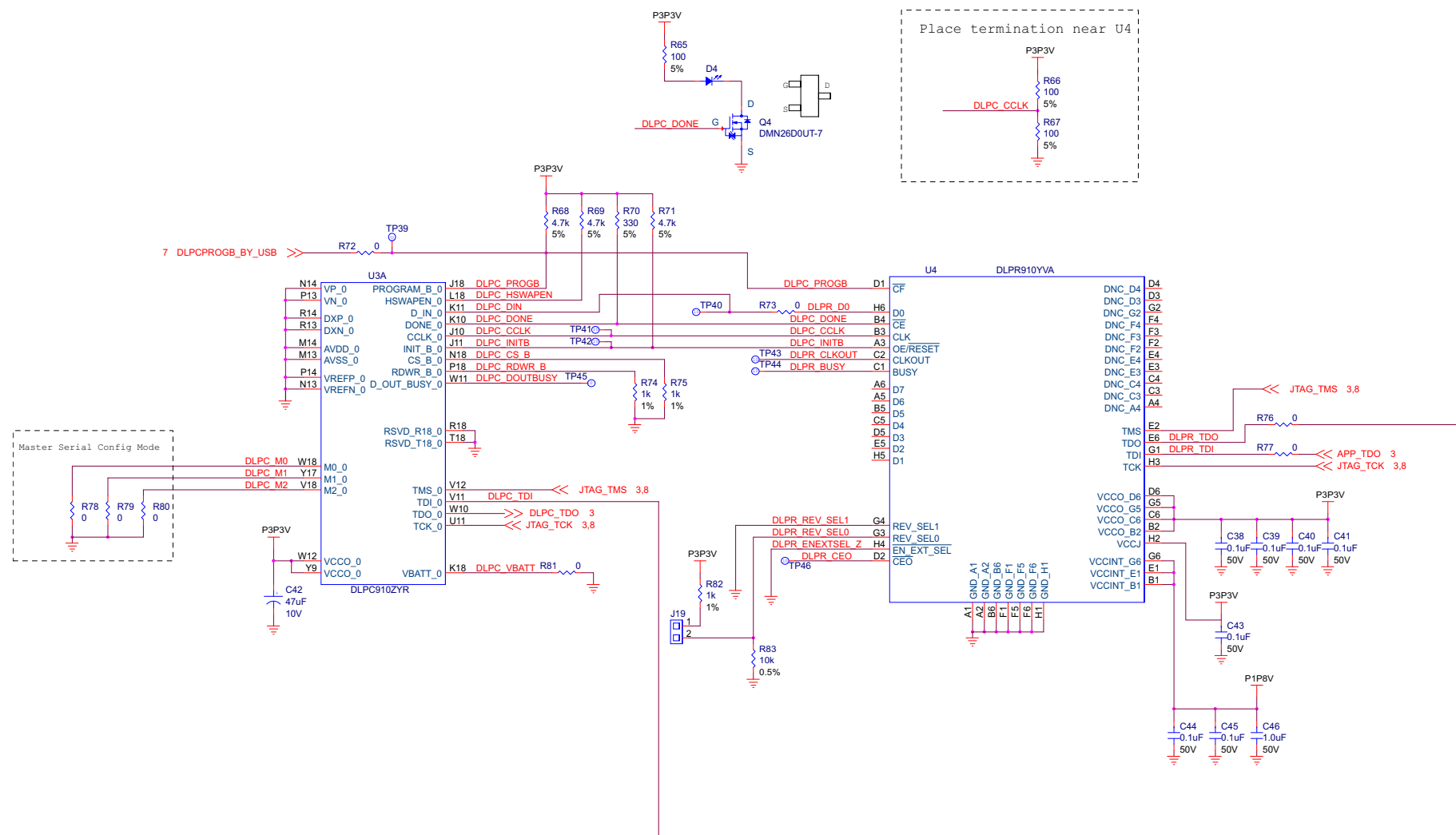


Figure 2. DLPC910 and DLPR910 Connection Schematic

NOTE

Typical Application (continued)

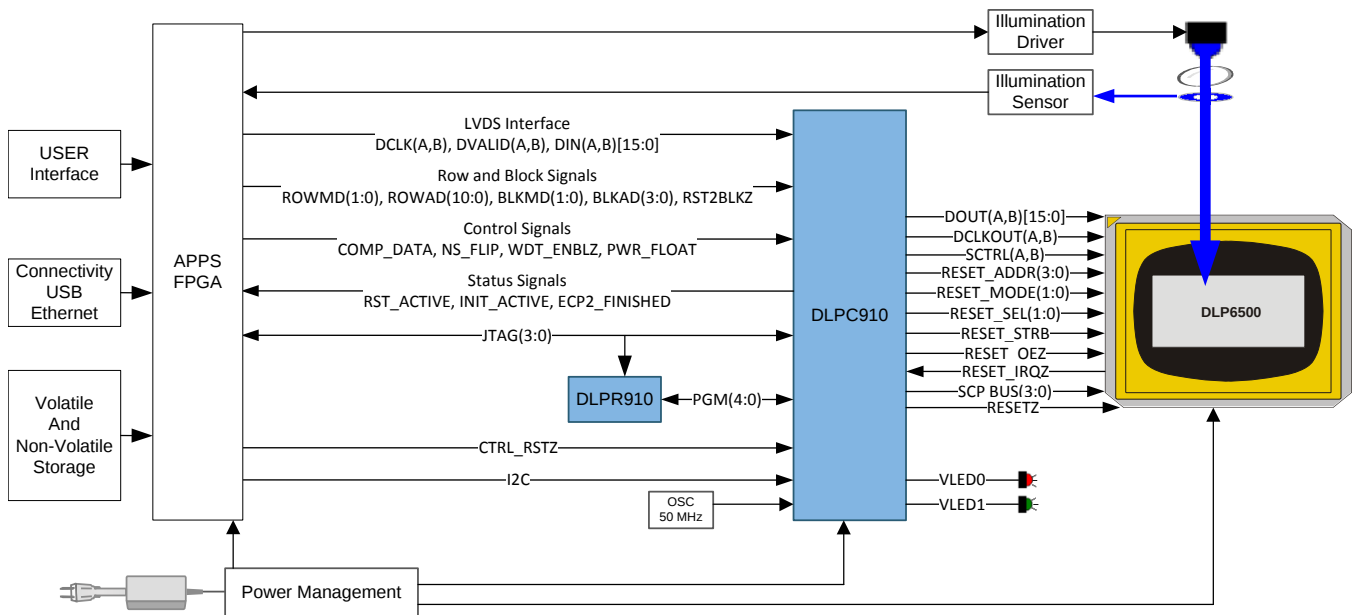


Figure 4. Typical High Speed DLP6500 Application Schematic

8.2.1 Design Requirements

The DLPR910 is part of a multi-chipset solution, and it is required to be coupled with the DLPC910 for reliable operation of the DLP9000X DMD or the DLP6500 family of DMDs. For more information, refer to the DLPC910 datasheet listed in [Related Documentation](#).

9 Power Supply Recommendations

The DLPR910 uses two power supply rails as shown in [Table 1](#).

Table 1. DLPR910 Power Supply Rails

SUPPLY	POWER PINS	COMMENTS
1.8 V	V _{CCINT1} , V _{CCINT2} , and V _{CCINT3}	All V _{CCINT} pins must be connected with a 0.1-μF decoupling capacitor to GND.
3.3 V	V _{CCO1} , V _{CCO2} , V _{CCO3} , V _{CCO4} , and V _{CCJ}	All V _{CCO} and V _{CCJ} pins must be connected with a 0.1-μF decoupling capacitor to GND.

10 Layout

10.1 Layout Guidelines

The DLPR910 is part of a multi-chipset solution, and it is required to be coupled with the DLPC910 for reliable operation of the DLP9000X DMD or the DLP6500 family of DMDs. Refer to the DLPC910 datasheet listed in [Related Documentation](#) for a layout example for this multi-chipset solution.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Compatibility

TI PART NUMBER	PRIOR TO REVISION "B" DMDs ⁽¹⁾	REVISION "B" DMDs OR LATER ⁽¹⁾
DLPR910YVA	Compatible	Not Compatible
DLPR910AYVA	Compatible	Compatible

(1) Refer to each individual DMD datasheet under Device and Documentation Support to determine location and revision of the DMD.

11.1.2 Device Nomenclature

Table 2. Part Number Description

TI PART NUMBER	DESCRIPTION	REFERENCE NUMBER
DLPR910AYVA	DLPR910 Configuration PROM	2514595-0002

11.1.3 Device Markings

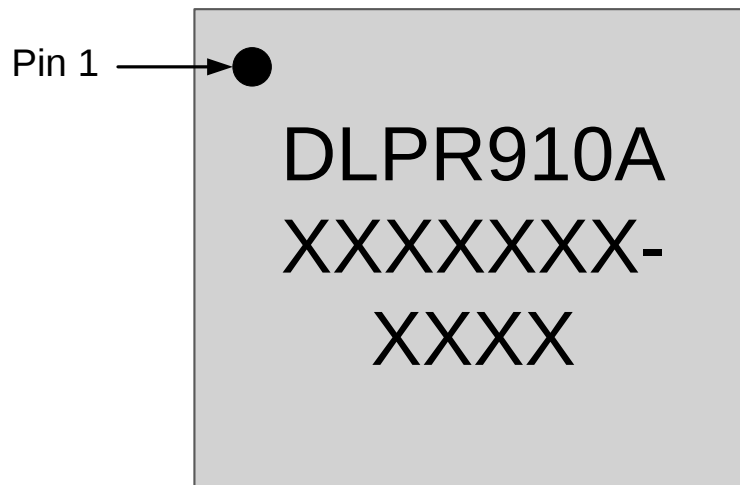


Figure 5. DLPR910 Device Markings

Where XXXXXXXX-XXXX is the reference number located in [Table 2](#).

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- DLPC910ZYR datasheet ([DLPS064](#))
- DLP9000(X) datasheet ([DLPS036](#))
- DLP6500 Type A datasheet ([DLPS040](#))
- DLP6500 S600 datasheet ([DLPS053](#))
- XCF16P data sheet (www.xilinx.com)

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

DLP is a registered trademark of Texas Instruments.

Xilinx is a registered trademark of Xilinx, Inc.

All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPR910AYVA	ACTIVE	DSBGA	YVA	48	1	TBD	Call TI	Call TI			Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

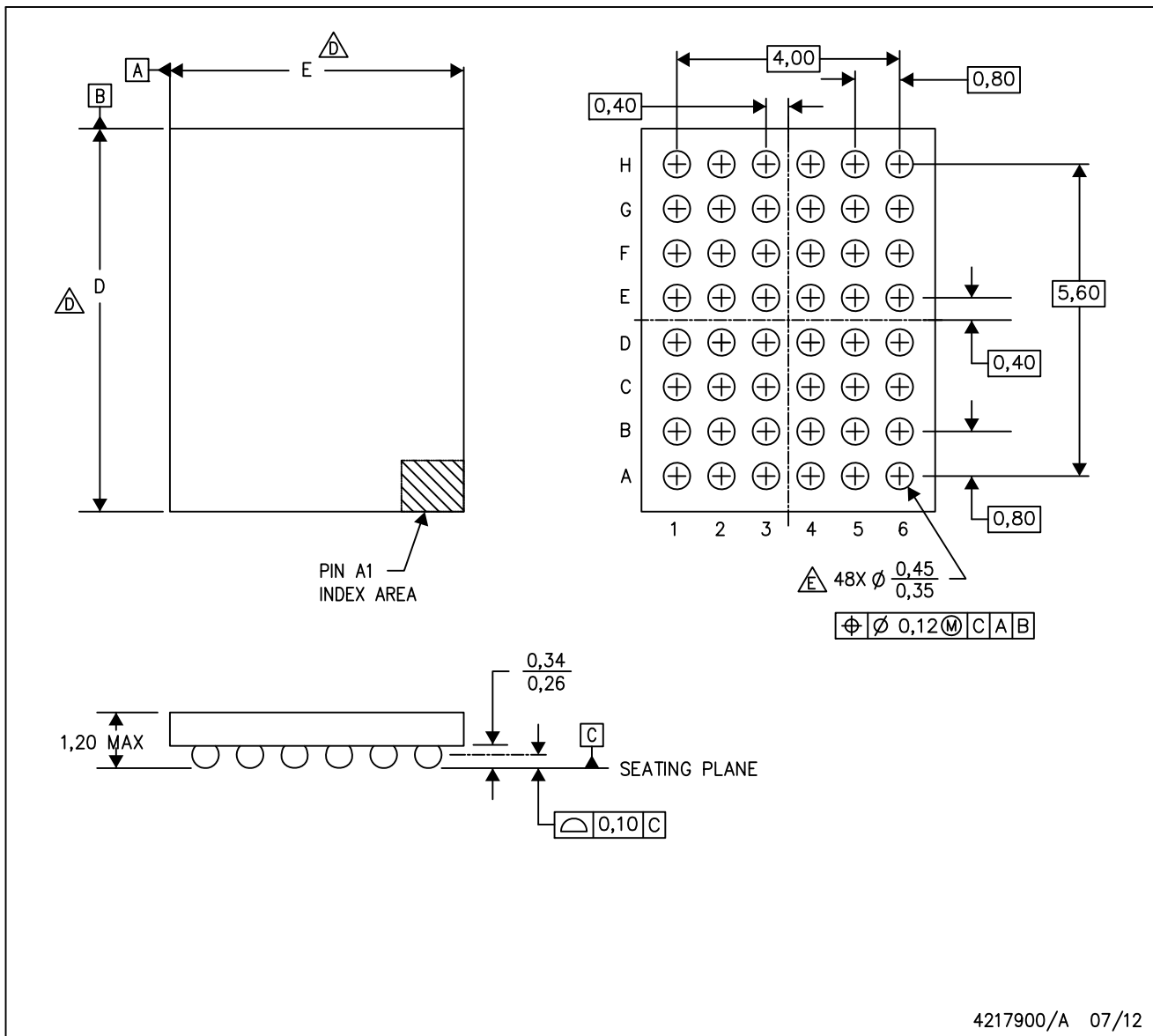
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

YVA (R-XBGA-N48)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 -  The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
 - E. Reference Product Data Sheet for array population. 6 x 8 matrix pattern is shown for illustration only.
 - F. This package contains Pb-free balls.

NanoFree is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.