



SCCS056A - August 1994 - Revised October 2001

# CY74FCT16500T CY74FCT162500T

## 18-Bit Registered Transceivers

### Features

- FCT-C speed at 4.6 ns
- $I_{off}$  supports partial-power- mode operation
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- $V_{CC} = 5\text{V} \pm 10\%$

#### CY74FCT16500T Features:

- 64 mA sink current, 32 mA source current
- Typical  $V_{OLP}$  (ground bounce) <1.0V at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$

#### CY74FCT162500T Features:

- Balanced 24 mA output drivers
- Reduced system switching noise
- Typical  $V_{OLP}$  (ground bounce) <0.6V at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$

### Functional Description

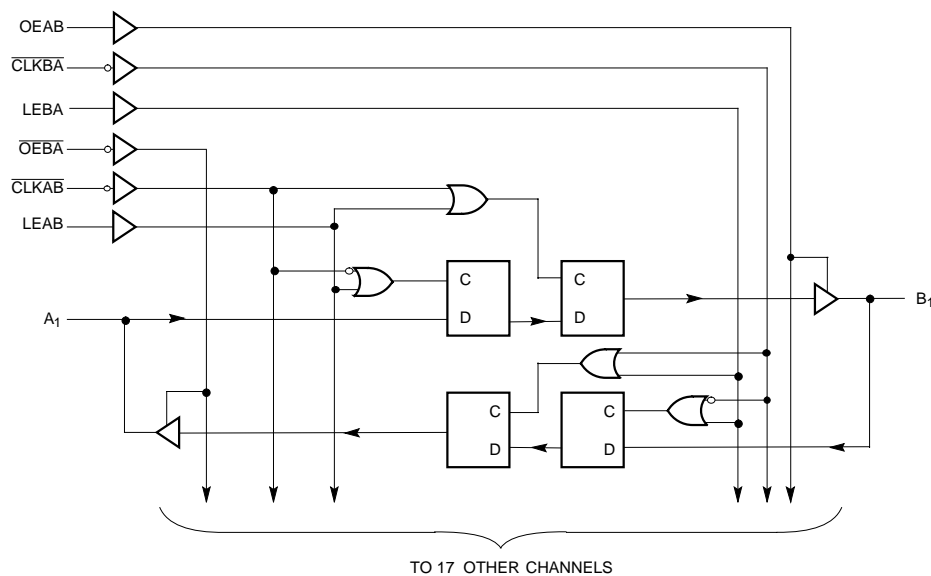
These 18-bit universal bus transceivers can be operated in transparent, latched, or clock modes by combining D-type latches and D-type flip-flops. Data flow in each direction is controlled by output-enable ( $\overline{\text{OEAB}}$  and  $\overline{\text{OEBA}}$ ), latch enable ( $\overline{\text{LEAB}}$  and  $\overline{\text{LEBA}}$ ), and clock inputs ( $\overline{\text{CLKAB}}$  and  $\overline{\text{CLKBA}}$ ) inputs. For A-to-B data flow, the device operates in transparent mode when  $\overline{\text{LEAB}}$  is HIGH. When  $\overline{\text{LEAB}}$  is LOW, the A data is latched if  $\overline{\text{CLKAB}}$  is held at a HIGH or LOW logic level. If  $\overline{\text{LEAB}}$  is LOW, the A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of  $\overline{\text{CLKAB}}$ .  $\overline{\text{OEAB}}$  performs the output enable function on the B port. Data flow from B-to-A is similar to that of A-to-B and is controlled by  $\overline{\text{OEBA}}$ ,  $\overline{\text{LEBA}}$ , and  $\overline{\text{CLKBA}}$ .

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

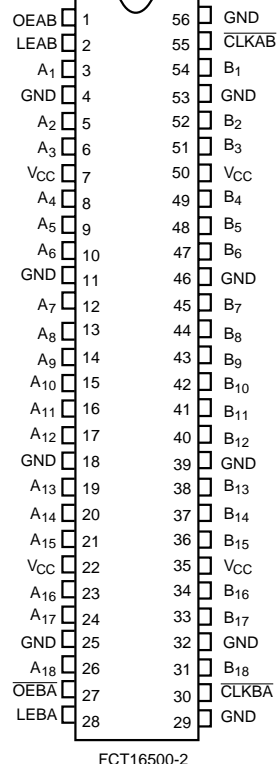
The CY74FCT16500T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162500T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162500T is ideal for driving transmission lines.

### Logic Block Diagram



### SSOP/TSSOP Top View



## Pin Summary

Name	Description
OEAB	A-to-B Output Enable Input
OEBA	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input (Active LOW)
CLKBA	B-to-A Clock Input (Active LOW)
A	A-to-B Data Inputs or B-to-A Three-State Outputs
B	B-to-A Data Inputs or A-to-B Three-State Outputs

## Function Table<sup>[1, 2]</sup>

Inputs				Outputs
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↯	L	L
H	L	↯	H	H
H	L	H	X	B <sup>[3]</sup>
H	L	L	X	B <sup>[4]</sup>

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. <sup>[7]</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage		2.0			V
V <sub>IL</sub>	Input LOW Voltage				0.8	V
V <sub>H</sub>	Input Hysteresis <sup>[8]</sup>			100		mV
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> =-18 mA		-0.7	-1.2	V
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>I</sub> =V <sub>CC</sub>			±1	μA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> =Max., V <sub>I</sub> =GND.			±1	μA
I <sub>OZH</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.7V			±1	μA
I <sub>OZL</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.5V			±1	μA
I <sub>OS</sub>	Short Circuit Current <sup>[9]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =GND	-80	-140	-200	mA
I <sub>O</sub>	Output Drive Current <sup>[9]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.5V	-50		-180	mA
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> =0V, V <sub>OUT</sub> ≤4.5V <sup>[10]</sup>			±1	μA

### Notes:

- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = HIGH Impedance. ↯ = HIGH-to-LOW Transition.
- A-to-B data flow is shown, B-to-A data flow is similar but uses OEBA, LEBA, and CLKBA.
- Output level before the indicated steady-state input conditions were established.
- Output level before the indicated steady-state input conditions were established, provided that CLKAB was LOW before LEAB went LOW.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.
- Typical values are at V<sub>CC</sub>=5.0V, T<sub>A</sub>=+25°C ambient.
- This parameter is specified but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
- Tested at +25°C.

## Maximum Ratings<sup>[5, 6]</sup>

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l -55°C to +125°C

Ambient Temperature with  
Power Applied..... Com'l -55°C to +125°C

DC Input Voltage .....-0.5V to +7.0V

DC Output Voltage .....-0.5V to +7.0V

DC Output Current  
(Maximum Sink Current/Pin) .....-60 to +120 mA

Power Dissipation ..... 1.0W

Static Discharge Voltage.....>2001V  
(per MIL-STD-883, Method 3015)

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40°C to +85°C	5V ± 10%

**Output Drive Characteristics for CY74FCT16500T**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[7]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-3 mA	2.5	3.5		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-15 mA	2.4	3.5		
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-32 mA	2.0	3.0		
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =64 mA		0.2	0.55	V

**Output Drive Characteristics for CY74FCT162500T**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[7]</sup>	Max.	Unit
I <sub>ODL</sub>	Output LOW Current <sup>[9]</sup>	V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V	60	115	150	mA
I <sub>ODH</sub>	Output HIGH Current <sup>[9]</sup>	V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V	-60	-115	-150	mA
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-24 mA	2.4	3.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =24 mA		0.3	0.55	V

**Capacitance<sup>[8]</sup> (T<sub>A</sub> = +25°C, f = 1.0 MHz)**

Parameter	Description	Test Conditions	Typ. <sup>[7]</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6.0	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5.5	8.0	pF

**Power Supply Characteristics**

Parameter	Description	Test Conditions	Typ. <sup>[7]</sup>	Max.	Unit
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> =Max. V <sub>IN</sub> ≤0.2V, V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	5	500	μA
ΔI <sub>CC</sub>	Quiescent Power Supply Current (TTL inputs HIGH)	V <sub>CC</sub> =Max. V <sub>IN</sub> =3.4V <sup>[11]</sup>	0.5	1.5	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>[12]</sup>	V <sub>CC</sub> =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OEAB=OEBA=V <sub>CC</sub> or GND V <sub>IN</sub> =V <sub>CC</sub> or V <sub>IN</sub> =GND	75	120	μA/MHz
I <sub>C</sub>	Total Power Supply Current <sup>[13]</sup>	V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz (CLKAB), f <sub>1</sub> =5 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, OEAB=OEBA=V <sub>CC</sub> LEAB=GND V <sub>IN</sub> =V <sub>CC</sub> or V <sub>IN</sub> =GND	0.8	1.7	mA
		V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	1.3	3.2	mA
		V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz, f <sub>1</sub> =2.5 MHz, 50% Duty Cycle, Outputs Open, Eighteen Bits Toggling, OEAB=OEBA=V <sub>CC</sub> LEAB=GND V <sub>IN</sub> =V <sub>CC</sub> or V <sub>IN</sub> =GND	3.8	6.5 <sup>[14]</sup>	mA
		V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	8.5	20.8 <sup>[14]</sup>	mA

**Notes:**

11. Per TTL driven input (V<sub>IN</sub>=3.4V); all other inputs at V<sub>CC</sub> or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
13.  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input (V<sub>IN</sub>=3.4V)  
 $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at D<sub>H</sub>  
 $I_{CCD}$  = Dynamic Current caused by an input transition pair (HLH or LHL)  
 $f_0$  = Clock frequency for registered devices, otherwise zero  
 $f_1$  = Input signal frequency  
 $N_1$  = Number of inputs changing at f<sub>1</sub>  
 All currents are in milliamps and all frequencies are in megahertz.
14. Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are specified but not tested.

**Switching Characteristics** Over the Operating Range<sup>[15]</sup>

Parameter	Description	CY74FCT162500AT		CY74FCT16500CT/ CY74FCT162500CT		Unit	Fig. No. <sup>[16]</sup>
		Min.	Max.	Min.	Max.		
$f_{MAX}$	CLKAB or CLKBA frequency		150		150	MHz	
$t_{PLH}$ $t_{PHL}$	Propagation Delay A to B or B to A	1.5	5.1	1.5	4.6	ns	1, 3
$t_{PLH}$ $t_{PHL}$	Propagation Delay LEBA to A, LEAB to B	1.5	5.6	1.5	5.3	ns	1, 5
$t_{PLH}$ $t_{PHL}$	Propagation Delay CLKBA to A, CLKAB to B	1.5	5.6	1.5	5.3	ns	1, 5
$t_{PZH}$ $t_{PZL}$	Output Enable Time OEBA to A, OEAB to B	1.5	6.0	1.5	5.4	ns	1, 7, 8
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time OEBA to A, OEAB to B	1.5	5.6	1.5	5.2	ns	1, 7, 8
$t_{SU}$	Set-Up Time, HIGH or LOW A to CLKAB, B to CLKBA	3.0		3.0		ns	9
$t_H$	Hold Time, HIGH or LOW A to CLKAB, B to CLKBA	0		0		ns	9
$t_{SU}$	Set-Up Time, HIGH or LOW A to LEAB, B to LEBA	Clock HIGH	3.0		3.0	ns	4
		Clock LOW	1.5		1.5	ns	4
$t_H$	Hold Time, HIGH or LOW A to LEAB, B to LEBA	1.5		1.5		ns	4
$t_W$	LEAB or LEBA Pulse Width HIGH	3.0		2.5		ns	5
$t_W$	CLKAB or CLKBA Pulse Width HIGH or LOW	3.0		3.0		ns	5
$t_{SK(O)}$	Output Skew <sup>[17]</sup>		0.5		0.5	ns	

**Ordering Information CY74FCT16500T**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	CY74FCT16500CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16500CTPVC/PVCT	O56	56-Lead (300-Mil) SSOP	

**Ordering Information CY74FCT162500T**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.6	CY74FCT162500CTPVC	O56	56-Lead (300-Mil) SSOP	Industrial
	74FCT162500CTPVCT	O56	56-Lead (300-Mil) SSOP	
5.1	CT74FCT162500ATPVC	O56	56-Lead (300-Mil) SSOP	Industrial
	74FCT162500ATPVCT	O56	56-Lead (300-Mil) SSOP	

**Notes:**

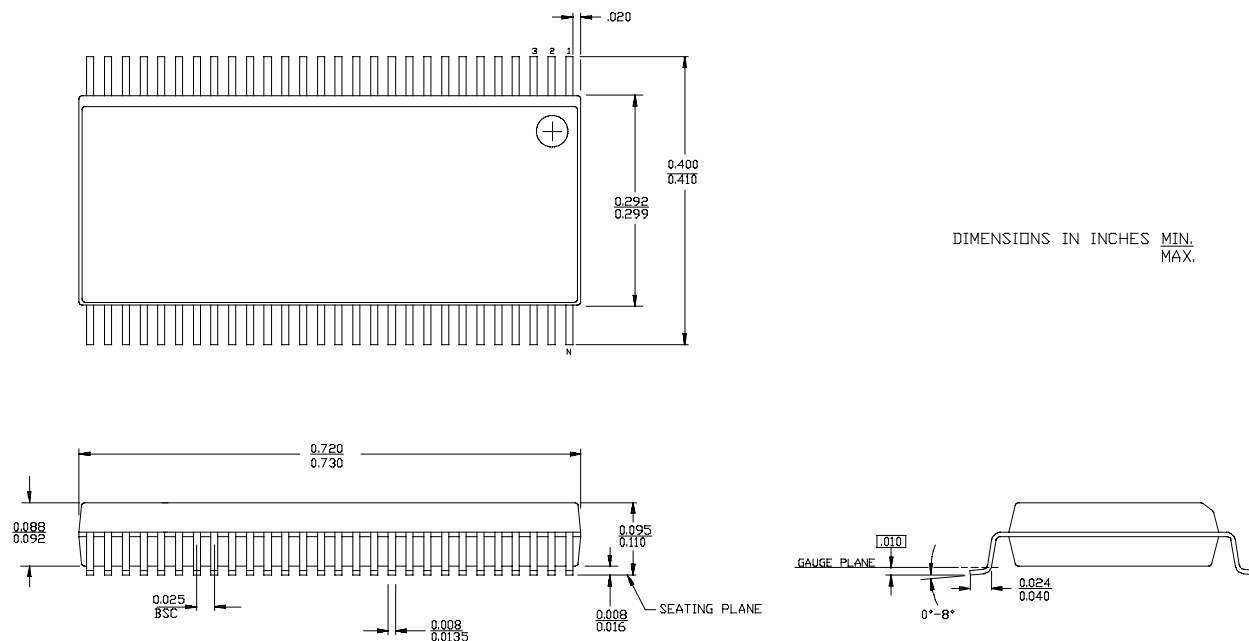
15. Minimum limits are specified but not tested on Propagation Delays.

16. See "Parameter Measurement Information" in the General Information section.

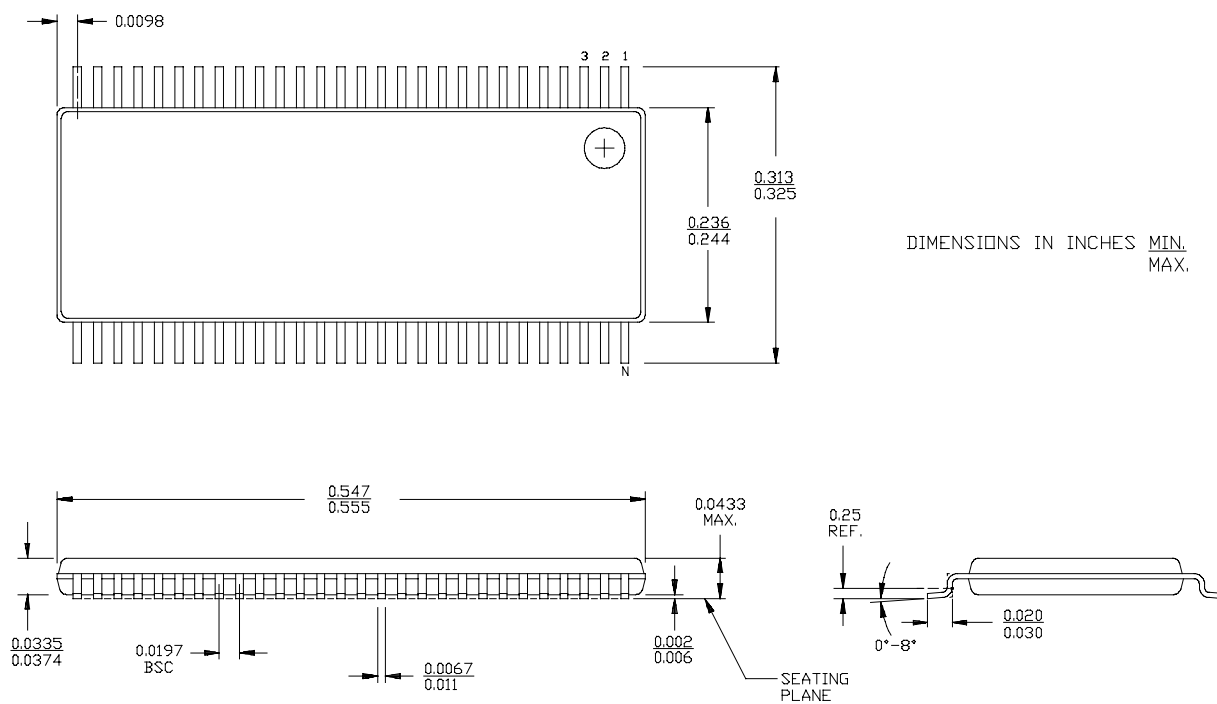
17. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

**Package Diagrams**

**56-Lead Shrunk Small Outline Package O56**



**56-Lead Thin Shrunk Small Outline Package Z56**



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY74FCT16500CTPVCT	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16500C	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

### REEL DIMENSIONS



### TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### TAPE AND REEL INFORMATION

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT16500CTPVCT	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT16500CTPVCT	SSOP	DL	56	1000	367.0	367.0	55.0

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed  $0.006$  (0,15).
  - D. Falls within JEDEC MO-118

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