

CDCI6214 Ultra-Low Power Clock Generator

With PCIe Gen4 Support, Four Programmable Outputs and EEPROM

1 Features

- One Configurable High Performance, Low-Power PLL With 4 Programmable Outputs
- RMS Jitter Performance
 - Supports PCIe Gen1 / Gen2 / Gen3 / Gen4 (typ. 386 fs)
- Typical Power Consumption: 150 mW at 1.8 V⁽²⁾
- Universal Clock Input
 - Differential AC-Coupled or LVCMOS: 1 MHz to 250 MHz
 - Crystal: 8 MHz to 50 MHz
- Flexible Output Frequencies
 - 44.1 kHz to 350 MHz
 - Glitch-Less Output Divider Switching
 - Spread Spectrum Clocking (SSC) for PCIe
- Four Individually Configurable Outputs
 - LVCMOS, LVDS or HCSL
 - Differential AC-Coupled With Programmable Swing (LVDS-, CML-, LVPECL-Compatible)
- Fully Integrated PLL, Configurable Loop Bandwidth: 100 kHz to 3 MHz
- Single or Mixed Supply Operation for Level Translation: 1.8 V, 2.5 V and 3.3 V
- Configurable GPIOs
 - Status Signals
 - Up to 4 Individual Output Enables
 - Output Divider Synchronization
- Flexible Configuration Options
 - I²C-Compatible Interface: Up to 400 kHz
 - Integrated EEPROM With Two Pages and External Select Pin
- Industrial Temperature Range: –40°C to 85°C
- Small Footprint: 24-Pin VQFN (4 mm × 4 mm)

2 Applications

- PCIe Gen 1/2/3/4 clocking
- 1G / 10G Ethernet Switches, NIC, Accelerators
- Test & Measurement , Handheld Equipment
- Multi-Function Printers
- Broadcast Infrastructure
- Servers

3 Description

The CDCI6214 device is an ultra-low power clock generator. The device selects between two independent reference inputs to a phase-locked loop and generates up to four different frequencies on configurable differential output channels and also a copy of the reference clock on a LVCMOS output channel.

Each of the four output channels has a configurable integer / fractional output divider and a dedicated integer divider. Together with the output muxes, this allows up to five different frequencies. Clock distribution dividers are reset in a deterministic way for clean clock gating and glitch-less update capability. Flexible power-down options allow to optimize the device for lowest power consumption in active and standby operation. Typically four 156.25 MHz LVDS outputs consume 150 mW at 1.8V. Typical RMS jitter of 386 fs for 100 MHz HCSL output enhances system margin for PCIe applications.

The CDCI6214 is configured using internal registers that are accessed by an I²C-compatible serial interface and internal EEPROM.

The CDCI6214 enables high-performance clock trees from a single reference at ultra-low power with a small footprint. The factory- and user-programmable EEPROM make the CDCI6214 ideal as easy-to-use, instant-on clocking solution with low power consumption.

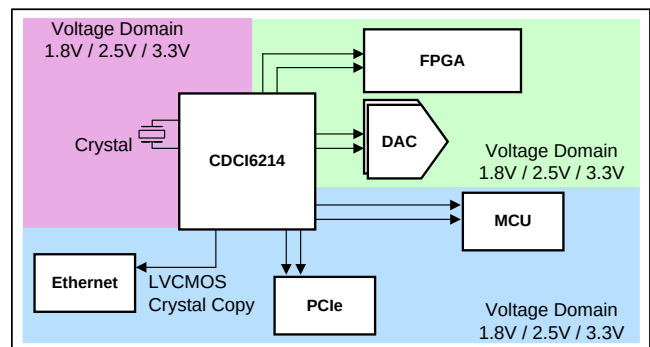
Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CDCI6214	VQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Four LVDS outputs, 156.25 MHz with crystal reference.

Application Example CDCI6214



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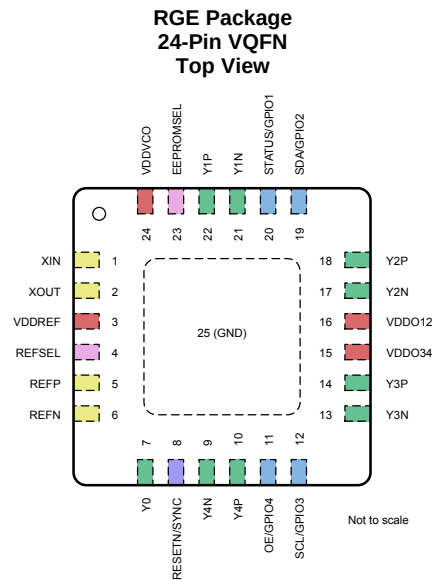
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2017) to Revision A	Page
• Changed device status from Advanced Info to Production Data	1
• Changed REFSEL pin description to reflx REFMUX control.	24

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
XIN	1	I	Reference / Crystal Input
XOUT	2	IO	Reference / Crystal Driver Output
VDDREF	3	P	Power Supply Pin for Input Path, Digital and EEPROM
REFSEL	4	I	Manual Reference Selection MUX for PLL, $R_{PU} = 50\text{ k}\Omega$, $R_{PD} = 50\text{ k}\Omega$
REFP	5	I	Differential Positive Reference
REFN	6	I	Differential Negative Reference
Y0	7	O	Output 0 Pin
RESETP/SYNC	8	I	Chip Reset. Alternatively, Output Divider Sync, $R_{PU} = 50\text{ k}\Omega$ ⁽¹⁾
Y4N	9	O	Output 4 Negative Pin
Y4P	10	O	Output 4 Positive Pin
OE/GPIO4	11	IO	Global output enable (default) or programmable GPIO, $R_{PU} = 50\text{ k}\Omega$ ⁽¹⁾
SCL/GPIO3	12	IO	Serial interface clock (default) or programmable GPIO
Y3N	13	O	Output 3 Negative Pin
Y3P	14	O	Output 3 Positive Pin
VDDO34	15	P	Power Supply for Outputs 3 and 4
VDDO12	16	P	Power Supply for Outputs 1 and 2
Y2N	17	O	Output 2 Negative Pin
Y2P	18	O	Output 2 Positive Pin
SDA/GPIO2	19	IO	Serial interface data (default) or programmable GPIO
STATUS/GPIO1	20	IO	Status (default) or programmable GPIO, $R_{PU} = 50\text{ k}\Omega$ ⁽¹⁾
Y1N	21	O	Output 1 Negative Pin
Y1P	22	O	Output 1 Positive Pin
EEPROMSEL	23	I	EEPROM Page Mode Select, $R_{PU} = 50\text{ k}\Omega$, $R_{PD} = 50\text{ k}\Omega$ ⁽¹⁾
VDDVCO	24	P	Power Supply Pin for VCO / PLL
GND	25	G	Ground, Thermal Pad

(1) R_{PU} is an internal pull-up resistor. R_{PD} is an internal pull-down resistor.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
VDDREF, VDDVCO, VDDO12, VDDO34	Supply Voltage	-0.3	3.6	V
XIN, XOUT, REFP, REFN	Input Voltage	-0.3	VDDREF + 0.3	V
STATUS/GPIO1, SDA/GPIO2, SCL/GPIO3, OE/GPIO4, REFSEL, EEPROMSEL, RESETN/SYNC	Input Voltage	-0.3	VDDREF + 0.3	V
Y0, Y1P, Y1N, Y2P, Y2N, Y3P, Y3N, Y4P, Y4N	Output Voltage	-0.3	VDDO _x + 0.3	V
STATUS/GPIO1, SDA/GPIO2, SCL/GPIO3, OE/GPIO4	Output Voltage	-0.3	VDDREF + 0.3	V
T _J	Junction Temperature		125	°C
T _{stg}	Storage temperature		150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDVCO	Core supply voltage	1.71		3.465	V
VDDO1	Output supply voltage	1.71		3.465	V
VDDO2	Output supply voltage	1.71		3.465	V
VDDO3	Output supply voltage	1.71		3.465	V
VDDO4	Output supply voltage	1.71		3.465	V
T _A	Ambient temperature	-40		85	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		CDCI6214	UNIT
		RGE (VQFN)	
		24 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	39.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	29.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	16.9	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	2.6	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ _{JB}	Junction-to-board characterization parameter	16.8	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 EEPROM Characteristics

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
n _{EEcyc}	EEPROM programming cycles	each word	10	10,000	cycles
t _{EEret}	EEPROM data retention		10		years

6.6 Reference Input, Single Ended and Differential Mode Characteristics (REFP, REFN, XIN, XOUT)

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{IN_Ref}	Reference frequency	1		250	MHz
V _{IH}	Input high voltage	LVC MOS input buffer	0.8 · VDDREF		V
V _{IL}	Input low voltage	LVC MOS input buffer		0.2 · VDDREF	V
V _{IN_DIFF}	Differential input voltage swing, peak-to-peak	VDDREF=2.5V or 3.3V, AC-coupled differential input buffer	0.5	1.6	V
V _{IN_DIFF}	Differential input voltage swing, peak-to-peak	VDDREF=1.8V, AC-coupled differential input buffer	0.5	1.0	V
dV _{IN} /dT	Input slew rate	20% - 80%	3		V/ns
IDC	Input duty cycle		40	60	%
C _{IN_XIN}	Input capacitance	No xtal active, on-chip load disabled, at 25°C	7		pF
C _{IN_XOUT}	Input capacitance	No xtal active, on-chip load disabled, at 25°C	5		pF
C _{IN_REF}	Input capacitance	at 25°C	5		pF

6.7 Reference Input, Crystal Mode Characteristics (XIN, XOUT)

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{IN_Xtal}	Crystal frequency	Fundamental mode	8	50	MHz
Z _{ESR}	Crystal equivalent series resistance	A supported crystal is within	30	100	Ω
C _L	Crystal load capacitance	using on-chip load capacitance a supported crystal is within	5	8	pF
P _{XTAL}	Crystal tolerated drive power	A supported crystal tolerates up to	100		μW
C _{XIN_LOAD}	On-Chip load capacitance	Programmable in typ. 200 fF steps at room temp	3	9.1	pF
DNL _{XIN_LO AD}	Differential non-linearity	at room temp	200		fF

6.8 General Purpose Input and Output Characteristics (GPIO[4:1], SYNC/RESETN)

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IH}	Input high voltage	0.8 · VDDREF			V
V _{IL}	Input low voltage			0.2 · VDDREF	V
I _{IH}	Input high level current	V _{IH} = VDDREF	-0.02		μA
I _{IH}	Input high level current	V _{IH} = VDDREF, Pin 12, 19	0.004		μA
I _{IL}	Input low level current	V _{IL} = GND	-50		μA
I _{IL}	Input low level current	V _{IL} = GND, Pin 12, 19	-0.004		μA
dV _{IN} /dT	Input slew rate	20% - 80%	0.5		V/ns
C _{IN_GPIO}	Input Capacitance			10	pF

General Purpose Input and Output Characteristics (GPIO[4:1], SYNC/RESETN) (continued)

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OH}	Output high voltage	only capacitive load	0.8 · VDDREF		V
V _{OL}	Output low voltage	only capacitive load		0.2 · VDDREF	V
dV _{OUT} /dT	Output slew rate	20% - 80%, at 10pF	0.3		V/ns
R _{PU}	Pull-up resistance	Pin 11, 20	77		kΩ

6.9 Triple Level Input Characteristics (EEPROMSEL, REFSEL)

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IH}	Input high voltage	0.8 · VDDREF			V
V _{IM}	Input mid voltage	0.41 · VDDREF	0.5 · VDDREF	0.58 · VDDREF	V
V _{IL}	Input low voltage			0.2 · VDDREF	V
I _{IH}	Input high level current	V _{IH} = VDDREF	40		μA
I _{IM}	Input mid level current	V _{IH} = VDDREF/2	-1		μA
I _{IL}	Input low level current	V _{IL} = GND	-40		μA
t _{RIN}	input slew rate	10% - 90%	50		ns
C _{IN_TRI}				10	pF
R _{PDPU}			64		kΩ

6.10 Reference Mux Characteristics⁽¹⁾

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
L _{REF_MUX}	Reference mux isolation	XIN = Crystal 25 MHz, REF = 27 MHz	89		dBc
L _{REF_MUX}	Reference mux isolation	XIN = Crystal 25 MHz, REF = 24.576 MHz	78		dBc

(1) Mux isolation is defined as the attenuation relative to the carrier base harmonic as a positive dBc number.

6.11 Phase Locked Loop Characteristics

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{PFD}	Phase Detector Frequency	1		100	MHz
f _{VCO}	Voltage Controlled Oscillator Frequency	2400		2800	MHz
f _{BW}	Configurable closed-loop PLL Bandwidth	REF = 25 MHz	100	3000	kHz
f _{CLKDIST}	Clock Distribution Frequency	400		700	MHz
K _{VCO}	Voltage Controlled Oscillator Gain	f _{VCO} = 2.4 GHz	62		MHz/V
K _{VCO}	Voltage Controlled Oscillator Gain	f _{VCO} = 2.5 GHz	62		MHz/V
K _{VCO}	Voltage Controlled Oscillator Gain	f _{VCO} = 2.8 GHz	92		MHz/V
ΔT _{CL}	Allowable Temperature Drift for Continuous Lock	dT/dt ≤ 20 K / min		125	°C

6.12 Closed Loop Output Jitter Characteristics

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{RJ_CL} RMS Phase Jitter	int. Range from 10 kHz to 20 MHz , XIN = Crystal 25 MHz, Yx = 156.25 MHz LVDS		500	750	fs
t _{RJ_CL} RMS Phase Jitter	int. Range from 10 kHz to 20 MHz , XIN = Crystal 25 MHz, Yx = 100 MHz HCSL		386	800	fs
t _{RJ_CL} RMS Phase Jitter	PCIe Gen 3/4 Common Clock transfer functions applied, XIN = Crystal 25 MHz, Yx = 100 MHz HCSL			500	fs
t _{RJ_CL} RMS Phase Jitter	int. Range from 10 kHz to 20 MHz , XIN = Crystal 25 MHz, VCO = 2500 MHz, Fractional Divider , Y1 =122.88 MHz LVDS		2		ps

6.13 PCIe Spread Spectrum Generator

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C, f_{VCO}=2.4

GHz, ch[4:1]_iod_mux = 2, ch[4:1]_iod

=3, ch[4:1]_ssc_counter=4, ch[4:1]_ssc_fmod=1, ch[4:1]_ssc_type=1, ch[4:1]_ssc_spread=0

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{SSC} SSC deviation			31.25		kHz
t _{SSC_FREQ_DEVIATION} SSC deviation			-0.5		%

6.14 Output Mux Characteristics⁽¹⁾

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
L _{OUT_MUX} Output mux isolation	REF=27 MHz, XIN = 25 MHz, VCO = 2500 MHz, PSFB=4, Y_ODD = 312.5 MHz, Y_EVEN = 208.3 MHz, LVPECL		65		dBc
L _{OUT_MUX} Output mux isolation	REF=27 MHz, XIN = 25 MHz, VCO = 2500 MHz, PSFB=4, Y_ODD = 312.5 MHz, Y_EVEN = 250 MHz, LVPECL		63		dBc
L _{OUT_MUX} Output mux isolation	REF=27 MHz, XIN = 25 MHz, VCO = 2500 MHz, PSFB=4, Y_ODD = 312.5 MHz, Y_EVEN = 89.3 MHz, LVPECL		72		dBc
L _{OUT_MUX} Output mux isolation	REF=27 MHz, XIN = 25 MHz, VCO = 2500 MHz, PSFB=4, IODs = 312.5 MHz, Yx=BYPASS (XIN), LVPECL		64		dBc
L _{OUT_MUX} Output mux isolation	REF=27 MHz, XIN = 25 MHz, VCO = 2500 MHz, PSFB=4, Y_ODD = 100 MHz, Y_EVEN = 266.6 MHz, LVPECL		57		dBc

⁽¹⁾ Mux isolation is defined as the attenuation relative to the carrier base harmonic as a positive dBc number.

6.15 LVCMOS Output Characteristics

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{O_LVCMOS} Output frequency	VDDO_x=2.5V or 3.3V, normal drive	0.1		350	MHz
f _{O_LVCMOS} Output frequency	VDDO_x=1.8V, normal drive	0.1		250	MHz
V _{OH_LVCMOS} Output high voltage	Normal mode, only capacitive load	0.8 · VDDREF			V

LVC MOS Output Characteristics (continued)

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OL_LVC MOS}$ Output low voltage	Normal mode, only capacitive load			0.2 · VDDREF	V
$V_{OH_LVC MOS}$ Output high voltage	slow mode, only capacitive load	0.7 · VDDREF			V
$V_{OL_LVC MOS}$ Output low voltage	slow mode, only capacitive load			0.3 · VDDREF	V
$R_{ON_LVC MOS}$ Output impedance	Normal mode		28		Ω
$R_{ON_LVC MOS}$ Output impedance	Weak mode		80		Ω
$L_{LVC MOS_100M}$ Phase noise floor, single side band	$f_{CARRIER}=100MHz$, $f_{OFFSET}=10MHz$		-148		dBc/Hz

6.16 HCSL Output Characteristics

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{O_HCSL} Output frequency		0.1		350	MHz
V_{CM_HCSL} Output common mode		0.2	0.34	0.55	V
V_{OD} Differential output voltage	$f_{O_HCSL}=100\text{ MHz}$	0.4		1.0	V
V_{SS} Differential output voltage, peak to peak	$f_{O_HCSL}=100\text{ MHz}$	0.8		2.0	Vpp
V_{CROSS} Absolute crossing point	$R_p=49.9\text{ }\Omega\pm5\%$, $f_{O_HCSL}=100\text{ MHz}$	250		550	mV
ΔV_{CROSS} Relative crossing point variation	w.r.t to average crossing point, $f_{O_HCSL}=100\text{ MHz}$		100		mV
dV/dt	Slew rate for rising and falling edge	differential, at $V_{CROSS} \pm 150\text{ mV}$, $f_{O_HCSL}=100\text{ MHz}$ (1)		4	V/ns
$\Delta dV/dt$	Slew rate matching	single ended, at $V_{CROSS} \pm 75\text{ mV}$, $f_{O_HCSL}=100\text{ MHz}$ (1)		20	%
ODC	Output duty cycle	Not in PLL bypass mode	45	55	%
R_p	Parallel termination	$R_p=49.9\text{ }\Omega\pm5\%$ required	45	55	Ω
L_{HCSL_100M} Phase noise floor, single side band	$f_{CARRIER}=100\text{ MHz}$, $f_{OFFSET}=10\text{ MHz}$		-152		dBc/Hz

(1) PCIe test load slew rate

6.17 LVDS DC-Coupled Output Characteristics

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{O_PRG_AC}$ Output frequency		0.1		350	MHz
V_{CM} Output common mode	VDDO_X = 2.5V, 3.3V, chx_lvds_cmtrim_inc=2	1.125	1.2	1.375	V
V_{CM} Output common mode	VDDO_X = 1.8V, chx_lvds_cmtrim_inc=2	0.8	0.9	1.0	V
V_{OD} Differential output voltage	LVDS	0.25	0.3	0.45	V
t_{RF} Output rise/fall times	LVDS (20% to 80%)		675		ps
ODC	Output duty cycle	Not in PLL bypass mode	45	55	%
$L_{LVDS_DC_100M}$ Phase noise floor, single side band	$f_{CARRIER}=100MHz$, $f_{OFFSET}=10MHz$		-152		dBc/Hz

6.18 Programmable Differential AC-Coupled Output Characteristics

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C and AC-coupled outputs

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{O_PRG_AC} Output frequency		0.1		350	MHz
V _{OD} Differential output voltage	LVDS-like		0.45		V
V _{OD} Differential output voltage	CML-like		0.8		V
V _{OD} Differential output voltage	LVPECL-like		0.9		V
t _{RF} Output rise/fall times	LVDS-like (20% to 80%)		675		ps
t _{RF} Output rise/fall times	CML-like (20% to 80%)		520		ps
t _{RF} Output rise/fall times	LVPECL-like (20% to 80%)		500		ps
ODC Output duty cycle	Not in PLL bypass mode	45		55	%
L _{DIFF_AC_10} OM Phase noise floor, single side band	f _{CARRIER} =100MHz, f _{OFFSET} =10MHz		-152		dBc/Hz

6.19 Output Skew and Delay Characteristics

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{SK_HCSL} Skew between HCSL	Y[4:1] = HCSL, f _{OY[4:1]} =100 MHz		140	50	ps
t _{SK_DIFFAC} Skew between progr. differential AC	Y[4:1] = programmable output swing, f _{OY[4:1]} =100 MHz		150		ps
t _{SK_LVCMOS} Skew between LVCMOS	Y[4:1] = LVCMOS, f _{OY[4:1]} =100 MHz		100		ps
t _{SK_LVCMOS_BYP} Skew between LVCMOS to Bypass	Y[4:0] = LVCMOS, f _{OY[4:0]} =100 MHz		3		ns
t _{PD_ZDM} Propagation Delay	REF=67 MHz, VCO = 2680 MHz, PSFB=4, PSA _{Y_ODD} =4, PSB _{Y_EVEN} =4, IOD _{Y_ODD} =10, IOD _{Y_EVEN} =10, Y _{P_ODD} =Y _{N_ODD} =IOD, in ext. ZDM, LVCMOS	-600		600	ps

6.20 Output Synchronization Characteristics

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{SU_SYNC} Setup time SYNC pulse	with respect to PLL reference rising edge at 100 MHz with R=1	3			ns
t _{H_SYNC} Hold time SYNC pulse	with respect to PLL reference rising edge at 100 MHz with R=1			3	ns
t _{PWH_SYNC} High pulse width for SYNC	with R=1, at least 2 PFD periods + 24 feedback pre-scaler periods	60			ns
t _{PWL_SYNC} Low pulse width for SYNC	with R=1, at least 1 PFD period	6			ns
t _{EN} Individual output enable time ⁽¹⁾	tri-state to first rising edge, f _{Y[4:1]} < 200 MHz		4		nCK
t _{DIS} Individual output disable time ⁽¹⁾	last falling edge to tri-state, f _{Y[4:1]} < 200 MHz		4		nCK

(1) Output clock cycles of respective output channel. Global output enable handled by digital logic, additional propagation will be added.

6.21 Timing Characteristics

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and T_A = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{INIT} Initialization time	initialization time from POR to device releasing PLL outputs.			5	ms
t _{VDD} Power supply ramp	timing requirement for any VDD pin while RESETN=LOW	50		2000	μs

6.22 I²C-Compatible Serial Interface Characteristics (SDA/GPIO2, SCL/GPIO3)

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IH}	Input Voltage, Logic High	0.7 · VDDREF			V
V _{IL}	Input Voltage, Logic Low			0.3 · VDDREF	V
V _{HYS}	Input Schmitt Trigger Hysteresis	VDDREF=3.3V, f _{SCL} =400kHz	156		mV
V _{HYS}	Input Schmitt Trigger Hysteresis	VDDREF=2.5V, f _{SCL} =400kHz	118		mV
V _{HYS}	Input Schmitt Trigger Hysteresis	VDDREF=1.8V, f _{SCL} =400kHz	85		mV
I _{IH}	Input Leakage Current	VDDREF=0.17V..3.12V	-10	10	μA
V _{OL}	Low Level Output Voltage	at 3mA sink current, VDDREF=3.3V-5%		0.4	V
V _{OL}	Low Level Output Voltage	at 3mA sink current, VDDREF=2.5V-5%		0.4	V
V _{OL}	Low Level Output Voltage	at 2mA sink current, VDDREF=1.8V-5%		0.342	V
I _{OL}	Low Level Output Current	V _{OL} =0.4V	3		mA
C _{IN}	Input Capacitance			10	pF

6.23 Timing Requirements, I²C-Compatible Serial Interface (SDA/GPIO2, SCL/GPIO3)

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PW_G}	Pulse Width of Suppressed Glitches			50	ns
f _{SCL}	SCL Clock Frequency	Standard	100		kHz
f _{SCL}	SCL Clock Frequency	Fast-mode	400		kHz
t _{SU_STA}	Setup Time Start Condition	SCL=V _{IH} before SDA=V _{IL}	0.6		μs
t _{H_STA}	Hold Time Start Condition	SCL=V _{IL} after SCL=V _{IL} After this time, the first clock edge is generated.	0.6		μs
t _{SU_SDA}	Setup Time Data	SDA valid after SCL=V _{IL} , f _{SCL} =100kHz	250		ns
t _{SU_SDA}	Setup Time Data	SDA valid after SCL=V _{IL} , f _{SCL} =400kHz	100		ns
t _{H_SDA}	Hold Time Data ⁽¹⁾	SDA valid before SCL=V _{IH}	0 ⁽²⁾		⁽³⁾ μs
t _{PWH_SCL}	Pulse Width High, SCL	f _{SCL} =100kHz	4.0		μs
t _{PWH_SCL}	Pulse Width High, SCL	f _{SCL} =400kHz	0.6		μs
t _{PWL_SCL}	Pulse Width Low, SCL	f _{SCL} =100kHz	4.7		μs
t _{PWL_SCL}	Pulse Width Low, SCL	f _{SCL} =400kHz	1.3		μs
t _{OF}	Output Fall Time	C _{OUT} =10..400pF		250	ns

- (1) t_{H_SDA} is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge. use own words
- (2) A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH(min)} of the SCL signal) to bridge the undefined region of the falling edge of SCL. use own words
- (3) The maximum t_{H_SDA} could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode, but must be less than the maximum of t_{VD_SDA} by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{PWL_SCL}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock. use own words

6.24 Power Supply Characteristics

VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{DD_REF}	Reference input current	DBL=on	4		mA
I _{DD_XIN}	Crystal input current	Crystal with P _{max} =200μW	2		mA

Power Supply Characteristics (continued)

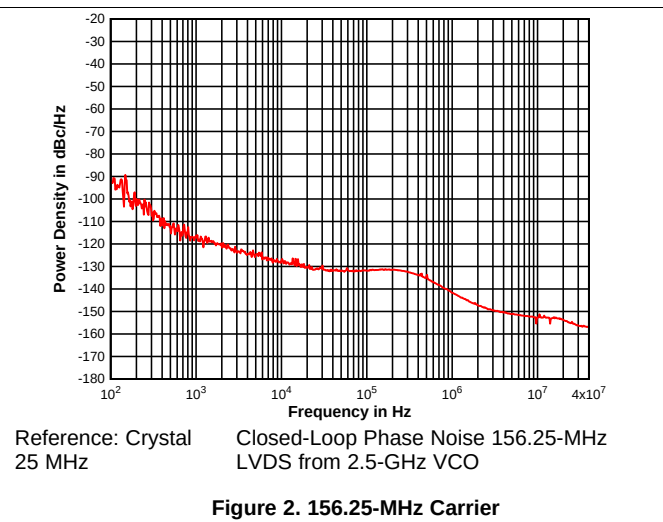
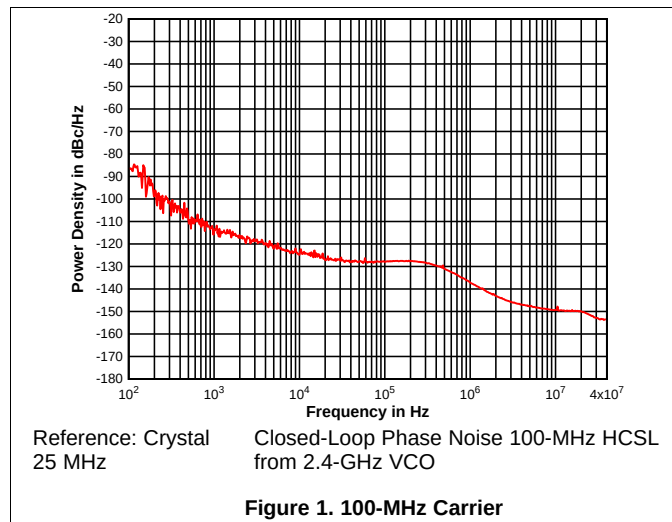
VDDVCO, VDDO12, VDDO34, VDDREF = 1.8V ±5%, 2.5V ±5%, 3.3V ±5% and TA = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{DD_VCO}	VCO and PLL current	f _{VCO} =2500MHz, PSFB=PSA=4 and PSB=off	13		mA
I _{DD_OUT}	Output channel current	activated output channel, 1x LVDS 156.25 MHz	10		mA
I _{DD_IOD}	Output integer divider current		2		mA
I _{DD_FOD}	Output fractional divider current		20		mA
I _{DD_PDN}	Power down current	using reset pin / bits	3		mA
I _{DD_TYP}	Typical current	4x 156.25 MHz LVDS case using crystal input and doubler	83		mA
I _{DD_TYP}	Typical current	2x IODs LVDS/LVCMOS, 1x FOD LVDS	72		mA
L _{PSNR}	Power supply noise rejection ⁽¹⁾	Yx=100MHz LVDS, on one of VDDx injected sine wave 50 mV at f _{INJ} =10kHz,	-56		dBc
L _{PSNR}	Power supply noise rejection ⁽¹⁾	Yx=100MHz LVDS, on one of VDDx injected sine wave 50 mV at f _{INJ} =100kHz	-46		dBc
L _{PSNR}	Power supply noise rejection ⁽¹⁾	Yx=100MHz LVDS, on one of VDDx injected sine wave 50 mV at f _{INJ} =1MHz	-49		dBc
L _{PSNR}	Power supply noise rejection ⁽¹⁾	Yx=100MHz LVDS, on one of VDDx injected sine wave 50 mV at f _{INJ} =10MHz	-69		dBc
L _{PSNR}	Power supply noise rejection ⁽¹⁾	Yx=100MHz LVDS, on one of VDDx injected sine wave 50 mV at f _{INJ} =20MHz	-74		dBc
L _{PSNR}	Power supply noise rejection ⁽¹⁾	Yx=100MHz LVDS, on one of VDDx injected sine wave 50 mV at f _{INJ} =40MHz	-73		dBc

(1) dBc with respect to output carrier frequency.

6.25 Typical Characteristics

VDDx = 1.8 V at room temperature



7 Parameter Measurement Information

7.1 Parameters

7.1.1 Reference Inputs

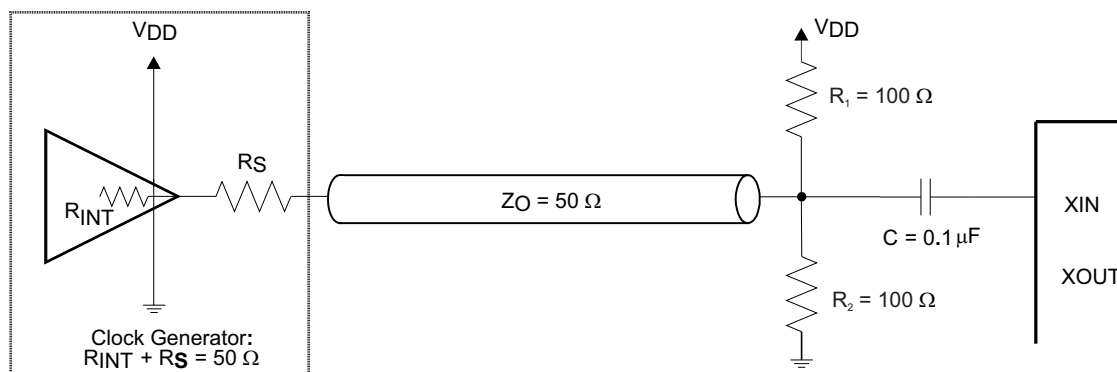
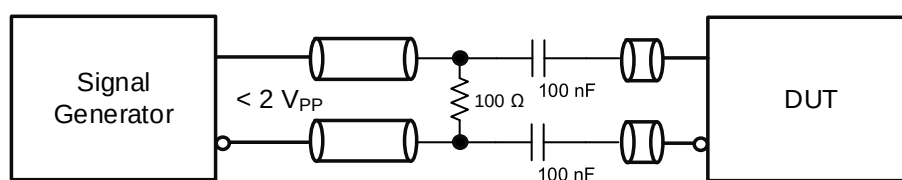


Figure 3. Single-Ended LVCMOS Crystal Input



(1) Applied signal has to stay within V_{IN_DIFF} limits.

Figure 4. Differential AC-Coupled Input

7.1.2 GPIOs

7.1.3 Outputs

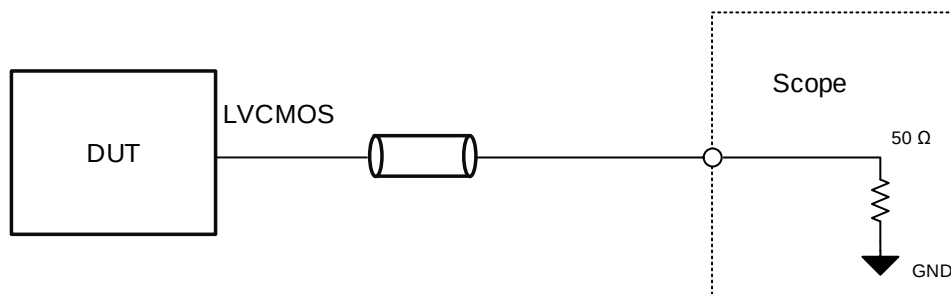


Figure 5. LVCMOS Output

Parameters (continued)

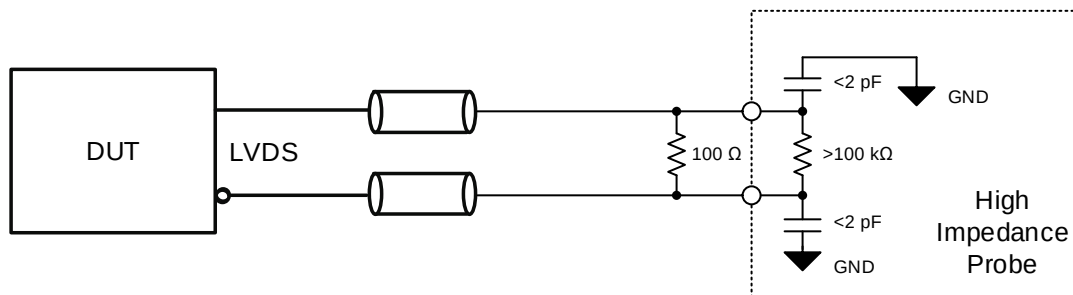


Figure 6. LVDS Output, DC-Coupled

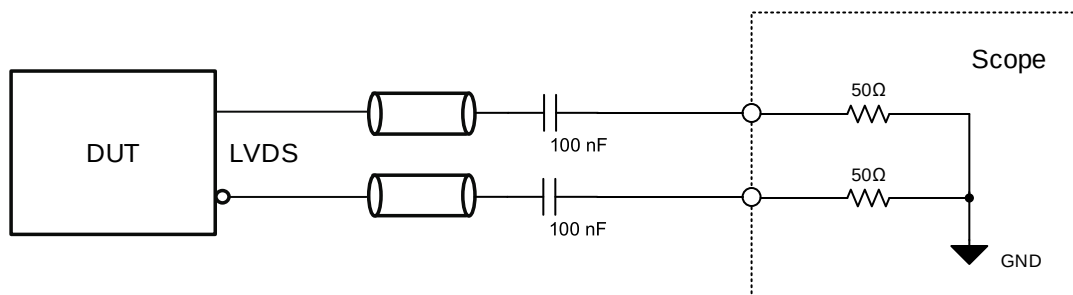


Figure 7. LVDS Output AC-Coupled

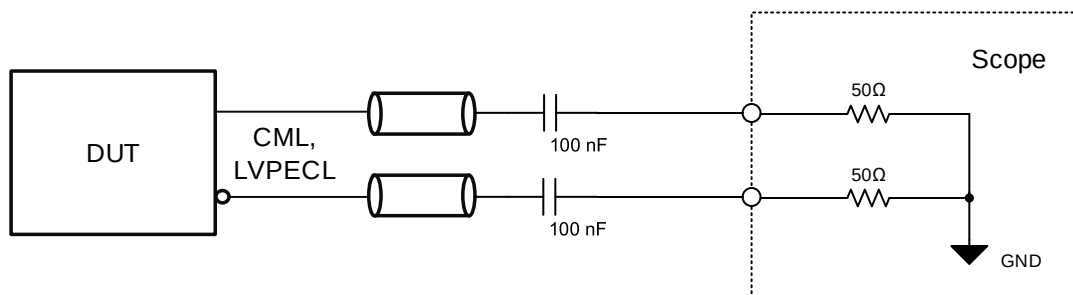


Figure 8. Differential AC-Coupled (CML, LVPECL)

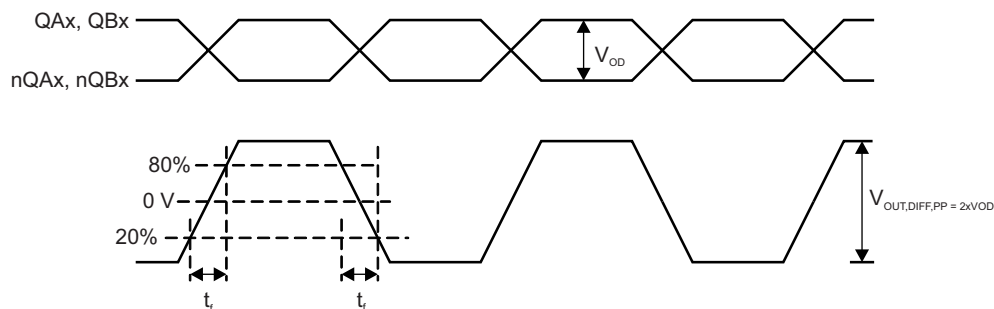
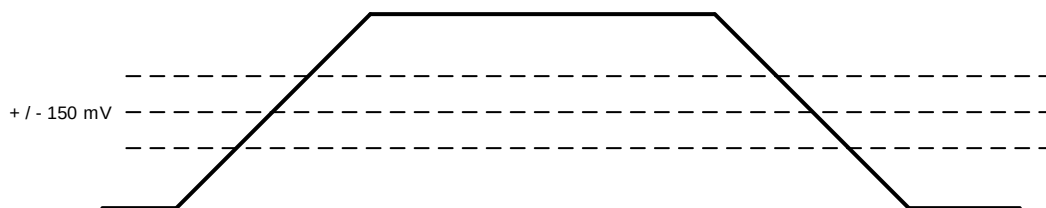


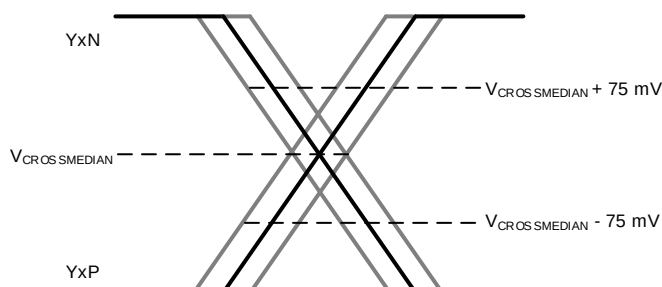
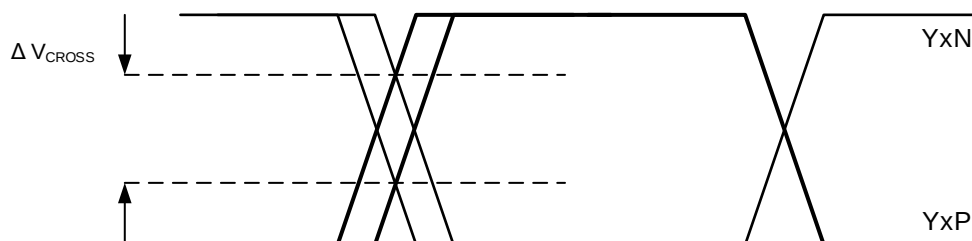
Figure 9. Differential Output Voltage and Rise/Fall Time

Parameters (continued)

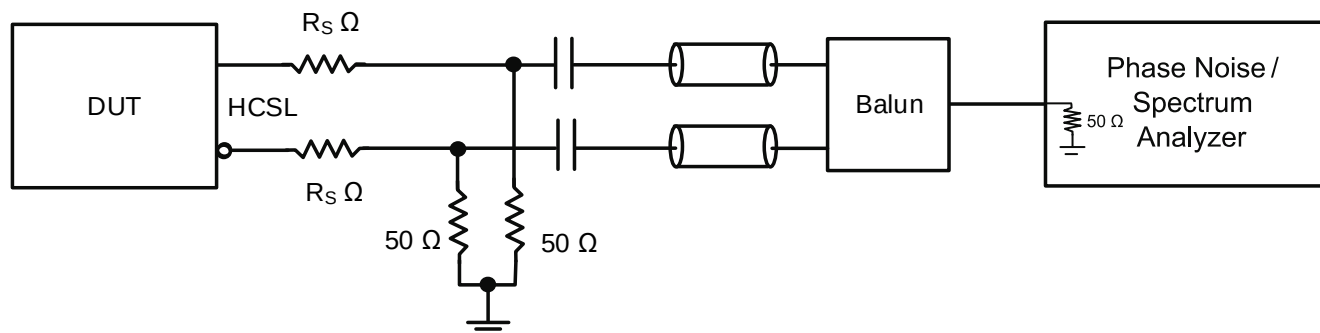
Differential Waveform HCSL



- (1) Differential waveform created using math function in scope subtracting positive from negative output pin waveform: $Y_{xP} - Y_{xN}$.
- (2) Slew rate measured using absolute ± 150 mV on the differential waveform. This correlates to the cross-point of the single ended positive and negative waveform.

Figure 10. HCSL, Differential Rise and Fall Time

Figure 11. HCSL, Slew Rate Variation


- (1) Measurement conducted using the single ended waveforms. Total variation of the crossing point of rising Y_{xP} and falling Y_{xN} edges.

Figure 12. HCSL, Delta Crossing Voltage

Figure 13. HCSL, Phase Noise Measurement

Parameters (continued)

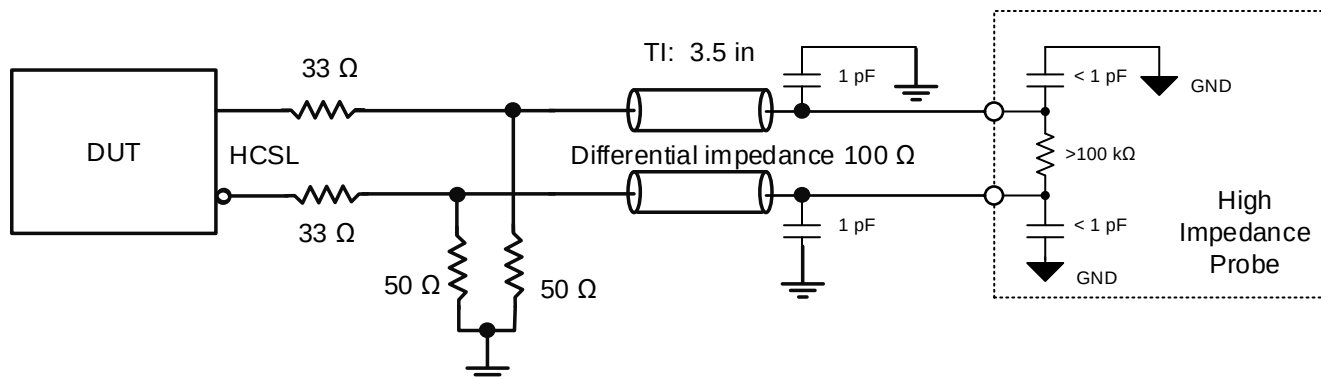


Figure 14. HCSL PCIe Test Load Setup

7.1.4 Serial Interface

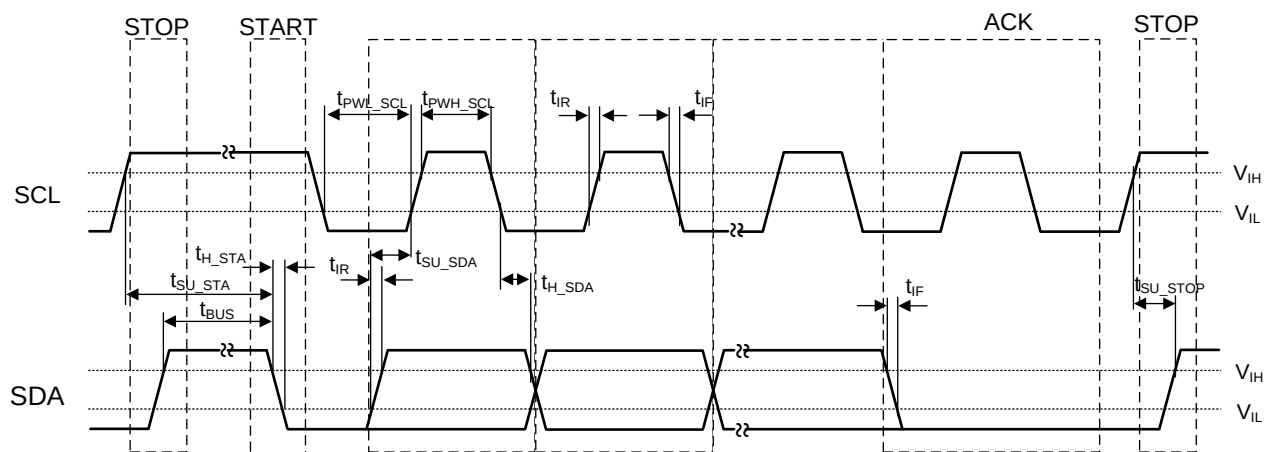


Figure 15. I²C Timing

7.1.5 Power Supply

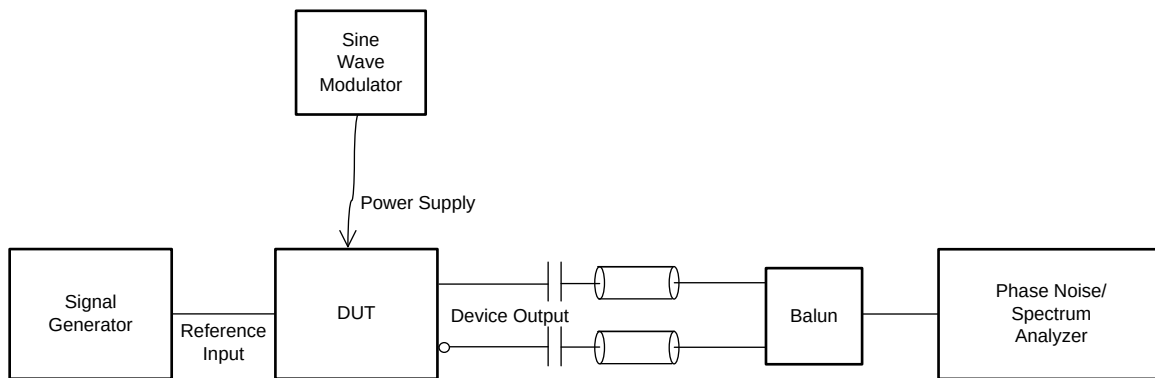


Figure 16. PSNR Setup

8.3 Feature Description

The following sections describe the individual blocks of the CDCI6214 ultra-low power clock generator.

8.3.1 Reference Block

A reference clock to the PLL is fed to pins 1 (XIN) and 2 (XOUT) or to pins 5 (REFP) and 6 (REFN). There are multiple input stages available to adapt to many clock references. The bit-fields that control the reference input type selection are [xin_inbuf_ctrl](#) and [ref_inbuf_ctrl](#).

The reference mux selects the reference for the PLL and the PLL-bypass path. For debug purposes [ip_byp_mux](#) allows to connect the reference divider or doubler output to the clock distribution.

The buffers for the PLL-bypass path can be individually enabled and disabled using [ip_byp_en_ch\[4:1\]](#) and [ip_byp_en_y0](#).

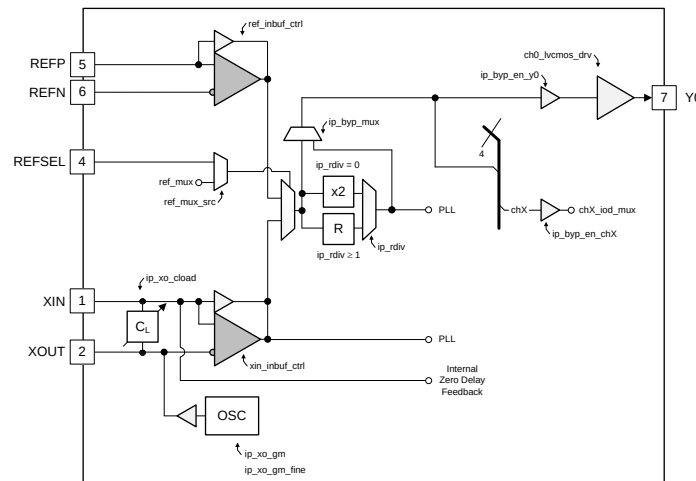


Figure 18. Reference Block

8.3.1.1 Input Stages

8.3.1.1.1 Crystal Oscillator

The XIN and XOUT pins provide a crystal oscillator stage to drive a fundamental mode crystal in the range of 8 MHz to 50 MHz. The crystal input stage integrates a tunable load capacitor array up to 9 pF using [ip_xo_cload](#). The drive capability of the oscillator is adjusted using [ip_xo_gm](#).

8.3.1.1.2 LVCMOS

The LVCMOS input buffer threshold voltage follows VDDREF. This helps to use the device as a level shifter as the outputs have separate supplies.

8.3.1.1.3 Differential AC-Coupled

The differential input stage has an internal bias generator and should only be used with AC-coupled reference inputs.

8.3.1.2 Reference Mux

Either XIN or REF can be selected as reference to the PLL and clock distribution path. The reference mux is controlled using the REFSEL pin with [ref_mux_src](#) = 0 or the [ref_mux](#) bit-field with [ref_mux_src](#) = 1.

8.3.1.3 Reference Divider

A reference divider can be used to divide higher input frequencies to the permitted PFD range. It supports division values of 1 to 255 using [ip_rdiv](#).

Feature Description (continued)

8.3.1.3.1 Doubler

The reference path contains a doubler circuit. It is used to double the input frequency and can be used to achieve the highest PFD update frequency of 100 MHz using a 50-MHz crystal. The doubler activates using [ip_rdiv](#) = 0.

8.3.1.4 Bypass-Mux

The input reference or the input to the PFD can be routed to the bypass path using [ip_byp_mux](#).

8.3.1.5 Zero Delay, Internal and External Path

In zero delay mode the REF input clock is used as reference clock at the PFD. The XIN clock can be used to feed an external source as feedback clock to the PFD. The external feedback path is recommended for zero delay operation. Moreover there is an additional internal feedback path which is sourced by output channel 2.

Table 1. Zero Delay Operation⁽¹⁾

Operation	Reference					Feedback							
	REFSEL	ref_mux	ref_mux_src	ip_rdiv	ref_inbuf_ctrl	xin_inbuf_ctrl	zdm_mode	zdm_cloc_ksel	zdm_auto	pll_psfb	pll_psa	pll_ndiv	ch2_iod_div ⁽²⁾
Normal PLL, XIN Reference	L	x	0	1	x	0	0	x	x	x	x	x	x
Normal PLL, REF Reference	L	x	0	1	x	x	0	x	x	x	x	x	x
Normal PLL, REF Reference	x	1	1	1	x	x	0	x	x	x	x	x	x
Zero Delay, Internal Feedback	x	1	1	1	A	A	1	0	1	B	B	C	C
Zero Delay, External Feedback	x	1	1	1	A	A	1	1	1	B	B	C	C

(1) 'x' allows any possible bit-field value. An entry of 'A', 'B' or 'C' indicates the same bit-field value.

(2) For internal feedback channel 2 is required. For external feedback the output clock connected to XIN / XOUT is recommended to have same settings as default PLL feedback path.

8.3.2 Phase-Locked Loop

The CDCI6214 contains a fully integrated phase-locked loop circuit. The error between a reference phase and an internal feedback phase is compared at the phase-frequency-detector. The comparison result is fed to a charge pump that is connected to an integrated loop filter. The control voltage resulting from the loop filter tunes an internal voltage-controlled oscillator (VCO). The frequency of the VCO is fed through a pre-scaler feedback divider (PSFB) and another feedback divider back to the PFD.

The PLL closed-loop bandwidth is configurable using registers [PLL0](#), [PLL1](#), and [PLL2](#).

- Integer PLL
- PFD operates 1 MHz to 100 MHz
- Live Lock-Detector provides PLL lock status on status pin and bit [lock_det](#) (there is an additional sticky bit [unlock_s](#))
- Integrated selectable loop filter components
- For 25-MHz PFD bandwidths between 100 kHz and 3000 kHz can be achieved to optimize PLL to input reference
- Voltage-Controlled Oscillator (VCO) tuning range of 2400 to 2800 MHz
- VCO is compatible to 0.5% spread spectrum (SSC) references at 100 MHz.

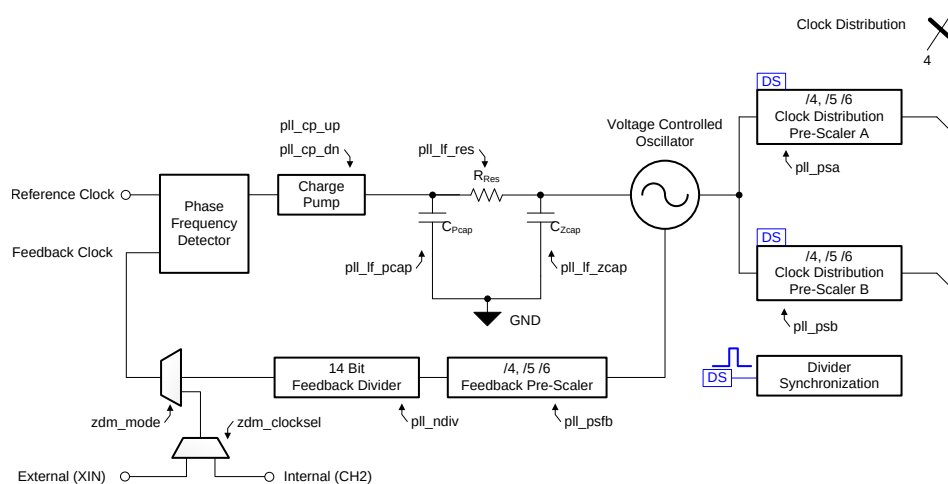


Figure 19. Phase-Locked Loop Circuit

Table 2. Common Clock Generator Loop Filter Settings⁽¹⁾

f _{VCO} in MHz	f _{PFD} in MHz	BW in MHz	Phase Margin in °	Damping Factor	I _{CP} in mA	C _{Pcap} IN pF	R _{Res} IN kΩ	C _{Zcap} IN pF
					pll_cp_up ⁽²⁾	pll_lf_pcap	pll_lf_res	pll_lf_zcap
2400	25	0.51	67	0.9	2.0	17.5	2.5	450
2400	50	0.97	67	1.3	2.0	17.5	2.5	450
2400	100	1.41	68	1.2	2.4	17.5	1.5	450
2457.6	61.44	1.04	67	1.4	1.8	17.5	2.5	450
2500	25	0.49	67	0.9	2.0	17.5	2.5	450
2500	50	0.93	68	1.3	2.0	17.5	2.5	450
2680	67	0.38	67	1.3	0.2	19.5	5.5	480
2688	48	0.93	68	1.3	1.5	17.5	2.5	480
2688	96	0.36	67	1.0	0.2	19.5	3.5	480
2800	50	1.00	68	1.0	2.6	17.5	1.5	450
2800	100	1.00	68	1.0	1.3	17.5	1.5	450

(1) All values typical design targets.

(2) Program same value to pll_cp_dn.

8.3.3 Clock Distribution

The VCO connects to two individually configurable pre-scaler dividers sourcing the on-chip clock distribution.

The clock distribution consists of four output channels. Each output channel contains a divider with integer and fractional division as well as spread-spectrum and synchronization capabilities.

A mux after each divider allows to feed the generated frequency to the adjacent output buffers. Thus for single frequency clock generation only a single output divider needs to be active.

The output buffers are compatible to various signaling standards: LVDS, CML-like, LVPECL-like, LVCMOS and HCSL using [ch1_outbuf_ctrl](#).

- HCSL must be directly connected to a load termination to ground. A series resistance can be used to adapt to the trace impedance.
- LVDS requires a differential termination connected between the positive and negative output buffer pins. The termination can be connected directly or using AC-coupling.
- CML and LVPECL are only supported in an AC-coupled configuration. The receiver and the termination may only be connected through AC-coupling capacitors to the device pins.
- LVCMOS outputs are designed for capacitive loads only. A series resistance should be used to adapt the driver impedance to the trace impedance. For a typical 50-Ω trace, a resistor between 22 Ω to 33 Ω should be

used. The polarity of the positive and negative pins can be adjusted separately.

The output buffers support a wide frequency range of up to 350 MHz. Higher output frequencies up to 700 MHz are functional, but are not covered by electrical specifications.

8.3.3.1 Output Channel

Figure 20. Clock Distribution Pre-Scaler Dividers⁽¹⁾

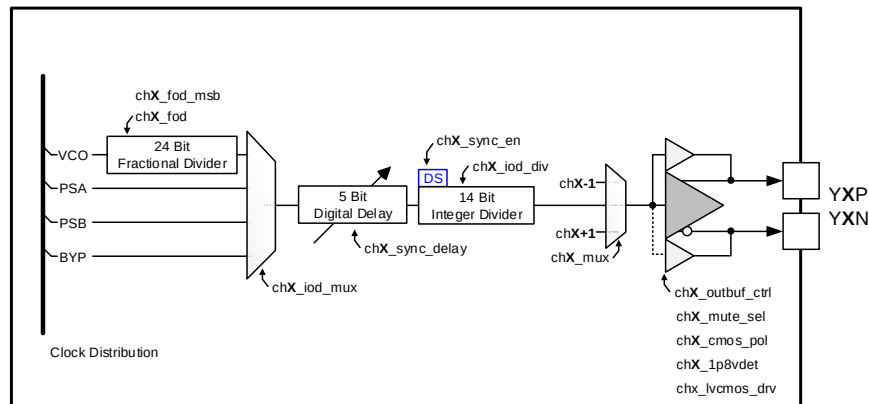


Figure 21. Clock Distribution, Output Channel

INSTANCES	DIVISION VALUES
PSA	4, 5, 6
PSB	4, 5, 6

(1) A known phase relationship for divider synchronization with mixed division values is ensured by architecture.

Table 3. Output Buffer Signal Standards

OUTPUT	LVC MOS	HCSL ⁽¹⁾	LVDS	AC-CML ⁽²⁾	AC-LVPECL ⁽²⁾
Y0	X				
Y1		X	X	X	X
Y2	X	X	X	X	X
Y3	X	X	X	X	X
Y4		x	X	x	X

(1) For highest performance it is recommended to use HCSL on output Y1 or Y4.

(2) The common mode shall be provided externally through an external bias source, like a voltage divider or pull-up resistor. The output buffer will provide sufficient swing.

Table 4. Output Channel Signal Selection

NO.	INPUT SOURCE	Y1 (N=1)	Y2 (N=2)	Y3 (N=3)	Y4 (N=4)
0	Channel N-1		X	X	X
1	IOD N	X	X	X	X
2	Channel N+1	X	X	X	

Table 5. Integer Divider Input Selection

NO.	SOURCE
0	Pre-scaler A
1	Pre-scaler B
2	Fractional Divider
3	Bypass

Table 6. Output Channel Divider Types and Delay

ABBREVIATION	TYPE	DIVIDER		DELAY
		MIN	MAX	PRE-SCALER, CYCLES
IOD	Integer	1	16383	32 ⁽¹⁾
FOD	Fractional ⁽²⁾	2 / 3	4 / 3	32 ⁽³⁾

(1) Cycles of the selected pre-scaler PSA or PSB.

(2) with respect to fractional divider input frequency $f_{FOD_IN} = f_{VCO} / 8$.

(3) Cycles of $f_{VCO}/8$.

8.3.3.2 Fractional Divider

8.3.3.2.1 Synthesis Mode

A 24-Bit resolution fractional divider synthesizes any frequency between $f_{VCO}/12 \leq f_{FOD} \leq f_{VCO}/6$. The synthesized frequency f_{FOD} is available on the respective integer divider source mux [ch\[4:1\]_iod_mux](#) for further division when required.

Please use the TICS Pro software to generate the fractional divider settings for [ch\[4:1\]_fod_msb](#) and [ch\[4:1\]_fod](#).

In general the following bits should be considered to activate one of the fractional dividers.

- [pdn_pll_fodclk](#) = 0
- [pdn_ch\[4:1\]](#) = 0
- [pdn_ch\[4:1\]_fod](#) = 0
- [ch\[4:1\]_iod_mux](#) = 2

For spread spectrum operation the part shall be configured in "bypass-mode" which is basically a $f_{VCO} / 8$ integer mode. For bypass mode the settings shall be [ch\[4:1\]_fod_msb](#) = 32768 and [ch\[4:1\]_fod](#) = 0.

8.3.3.2.2 Spread Spectrum Clocking

The device offers a spread spectrum clocking option in each output channel. The following requirements have to be met for the spread spectrum option to operate:

$$f_{Y[4:1]} = f_{VCO} / (8 \cdot \text{ch}[4:1]_{\text{iod_div}})$$

where

- $2400 \leq f_{VCO} \leq 2800$
- $1 \leq \text{ch}[4:1]_{\text{iod_div}} \leq 48$
- $10 \text{ MHz} \leq f_{Y[4:1]} \leq 350 \text{ MHz}$

$$f_{\text{ssc_mod_chX}} = f_{YX} / (2 \cdot \text{chX_ssc_counter} \cdot \text{lookup}(\text{chX_ssc_fmod}))$$

where

- $\text{chX_ssc_counter_src} = 0$

8.3.3.2.2.1 Modulation Frequency

The modulation frequency of a spread spectrum clock is derived from the output frequency $f_{Y[4:1]}$.

Example: $Y1 = 100 \text{ MHz}$ with 31.25-kHz SSC modulation frequency.

$$f_{VCO} = 2400 \text{ MHz} \quad (3)$$

$$f_{Y1} = 100 \text{ MHz} \quad (4)$$

$$f_{\text{ssc_mod_ch1}} = 31.25 \text{ kHz}$$

where

- $\text{ip_rdiv} = 1$
- $\text{pll_ndiv} = 24$
- $\text{pll_psfb} = 4$
- $\text{pdn_pll_fodclk} = 0$
- $\text{pdn_ch1_fod} = 0$
- $\text{ch1_iod_mux} = 2$
- $\text{ch1_iod_div} = 3$

- ch1_ssc_counter_src = 0
 - ch1_ssc_counter = 4
 - ch1_ssc_fmod = 1 → lookup value is 400
- (5)

8.3.3.2.2 Frequency Deviation or Spectrum Spread

The energy of the harmonics from the rectangular clock signal can be spread over a certain frequency range. This frequency deviation leads to lowered average amplitude of the harmonics. This can help to mitigate electromagnetic interference (EMI) challenges in a system when the receiver supports this mode of operation. The modulation shape is triangular.

ch[4:1]_ssc_type selects center- or down-spread. For center-spread the configuration bit-field ch[4:1]_ssc_spread shall be interpreted as $f_{nom} \pm f_{spread}$. For down-spread options as $f_{nom} - f_{spread}$.

Table 7. Spread Spectrum

ch[4:1]_ssc_spread	Down-Spread	Center-Spread
	$f_{nom} + f_{spread}$	$f_{nom} \pm f_{spread}$
0	0.5%	0.25%
1	1.0%	0.5%
2	2.0%	1.0%
3	5.0%	2.5%

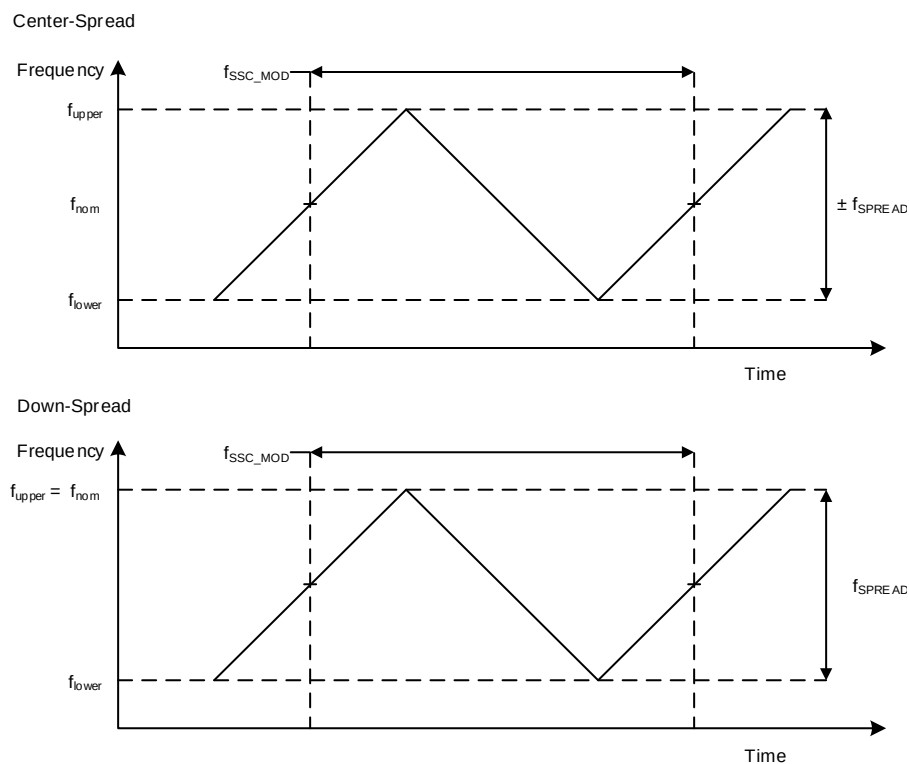


Figure 22. Spread Spectrum Clock

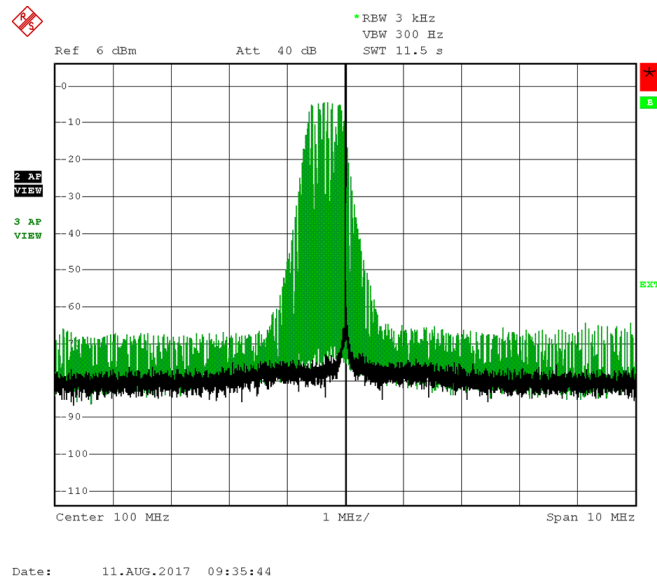


Figure 23. 100 MHz With 0.5% Spread Spectrum (Trace 3) and Without (Trace 2)

8.3.3.2.3 Recommended Usage

The spread spectrum settings in the registers are transferred to the analog block with a write of `ch[4:1]_ssc_en = 0`, followed by a write of `ch[4:1]_ssc_en = 1`.

8.3.3.3 Divider Glitch-Less Update

The bit fields `ch1_glitchless_en` can be used to enable glitch-less output divider update. This feature ensures that the high pulse of a clock period is not cut off by the output divider update process. It ensures that setup and hold time of a receiver is not violated. The low pulse in the *transition* from earlier period to the new period is extended accordingly.

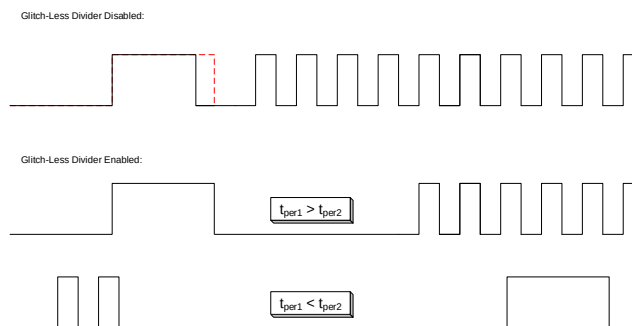


Figure 24. Glitch-Less Divider Update

8.3.4 Control Pins

The ultra-low power clock generator is controlled by multiple LVCMOS input pins.

EEPROMSEL acts as EEPROM page select. The CDCI6214 clock generator contains two pages of configuration settings. The level of this pin is sampled after device power-up. A low level selects page zero. A high level selects page one. The EEPROMSEL pin is a tri-level input pin. This third voltage level is automatically applied by an internal voltage divider. The mid-level is used to select an internal default where the serial interface is enabled.

RESETN/SYNC (pin 8), SCL (pin 12), and SDA (pin 19) have a secondary functionality and can act as general-purpose inputs and outputs (GPIO). This means that either the serial interface or the GPIO functionality can be active.

RESETN/SYNC resets the internal circuitry and is used in the initial power-up sequence. The pin can be reconfigured to act as synchronization input. The differential outputs are kept in mute while SYNC is low. When SYNC is high, outputs are active. Moreover status signals can be driven by this pin.

SCL can act as general-purpose input.

SDA can act as general-purpose input and output.

REFSEL is used to select between the input references to the PLL. A low level selects the crystal reference on XIN. A high level selects the differential input reference on REFP, REFN.

Table 8. Control and GPIO List

PIN			RECONFIGURABLE?	INPUT		OUTPUT	TERMINATION	
NO.	NAME	GPIO		2-LOGIC-LEVELS	3-LOGIC-LEVELS	2-LEVEL	PULLDOWN	PULLUP
23	EEPROMSEL	-	–	–	yes	–	50 kΩ	50 kΩ
20	STATUS	GPIO1	yes	yes	–	yes	–	50 kΩ
19	SDA	GPIO2	yes	yes	–	yes	–	–
12	SCL	GPIO3	yes	yes	–	–	–	–
11	OE	GPIO4	yes	yes	–	yes	–	50 kΩ
8	RESETN	GPIO0	yes	yes	–	yes	–	50 kΩ
4	REFSEL	-	–	–	yes	–	50 kΩ	50 kΩ

Table 9. GPIO - Input Signal List⁽¹⁾

SIGNAL NO.	ABBREVIATION	DESCRIPTION
0	FREQ_INC	Frequency increment; increments the IOD / FOD. ⁽²⁾
1	FREQ_DEC	Frequency decrement; decrements the IOD / FOD. ⁽²⁾
2	OE (global)	Enables or disables all differential outputs Y[4:1] (bypass not affected). ⁽³⁾
3	SSC_EN	Enables or disables SSC.
4	OE_Y1	Enables or disables Y1. ⁽³⁾
5	OE_Y2	Enables or disables Y2. ⁽³⁾
6	OE_Y3	Enables or disables Y3. ⁽³⁾
7	OE_Y4	Enables or disables Y4. ⁽³⁾

(1) Signals from this list are available on pin 11 (OE / GPIO4) and pin 20 (STATUS / GPIO1), see [GENERIC1](#).

(2) Selected using bit mask in [GENERIC3](#).

(3) Disable / Mute behaviour configured individually using ch_mute_sel bit in [GENERIC0](#) table.

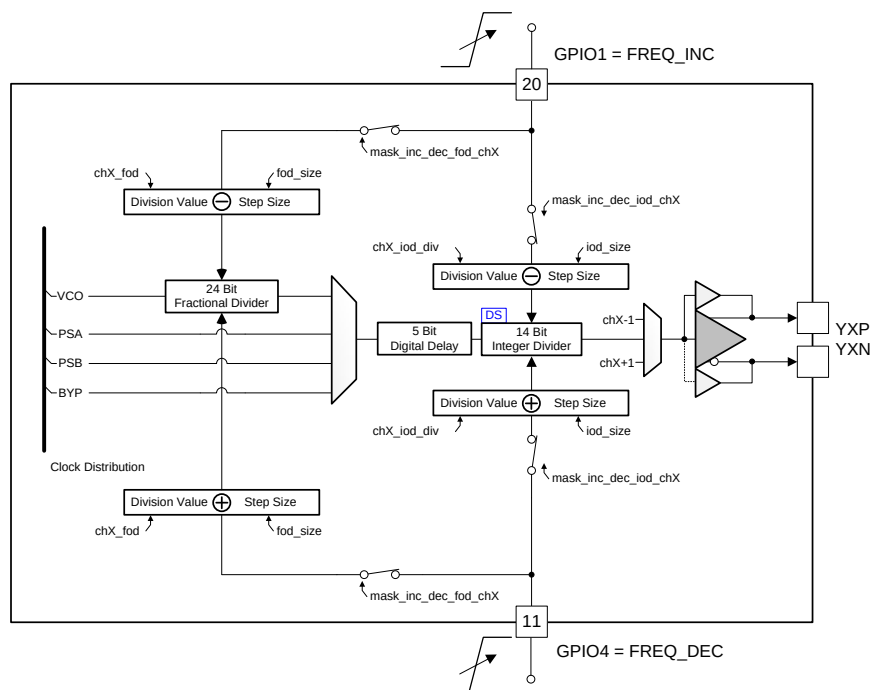
Table 10. GPIO - Output Signal List⁽¹⁾

SIGNAL NO.	ABBREVIATION	DESCRIPTION
0	PLL_LOCK	0 = PLL out of lock; 1 = indicates PLL in lock
1	XTAL_OSC	0 = crystal failure; 1 = crystal oscillates
2	CAL_DONE	0 = PLL (VCO) calibration ongoing; 1 = calibration done
3	CONF_DONE	0 = device logic busy; 1 = device operational
4	SYNC_DONE	0 = output sync ongoing, muted; 1 = outputs released operational
5	EEPROM_BUSY	0 = EEPROM idle; 1 = EEPROM access ongoing
6	EEPROM_Y12	0 = EEPROM pin sees low level; 1 = EEPROM pin sees high level
7	EEPROM_M12	0 = EEPROM pin sees low or high level; 1 = EEPROM pin sees mid level
8	I2C_LSB	Indicates I ² C slave address LSB config from loaded EEPROM
9	CLK_FSM	Clock, State machine
10	CLK_PFD_REF	Clock, PFD, reference
11	CLK_PFD_FB	Clock, PFD, feedback
12	BUF_SYNC	buffered SYNC pin

(1) Signals from this list are available on pin 8 (RESETN/SYNC or GPIO0), pin 11 (OE / GPIO4) and pin 20 (STATUS / GPIO1).

SIGNAL NO.	ABBREVIATION	DESCRIPTION
13	BUF_SCL	buffered SCL pin
14	BUF_SDA	buffered received SDA pin

This functionality allows to select integer or fractional output dividers in the clock distribution. A bit mask (`mask_inc_dec_fod_iod_ch[4:1]`) allows to select a divider to be incremented or decremented in a predefined, configurable step size. Every rising edge on the `FREQ_INC` signal increases the output frequency, thus decreases the division value. Every rising edge on the `FREQ_DEC` signal decreases the output frequency, thus increases the division value. There are two ways to trigger the increment or decrement: 1) appropriate configuration of the GPIOs and sending pulses using a micro-controller 2) using the shadow bits of the GPIOs via the serial interface, see `fod_iod_reg_mode`, `fod_iod_inc`, and `fod_iod_dec`.



8.3.4.2 Global and Individual Output Enable: OE and OE_Y[4:1]

The output enable functionality allows to enable or disable all or a specific output buffer. The bypass copy on Y0 is excluded from the global output enable signal. When an output is disabled, it drives a configurable mute-state, [ch\[4:1\]_mute_sel](#). When the serial interface is deactivated one can use all individual output enable signals at the same time, see [mode](#). The individual output enable signal controls the respective output channel integer divider to gate the clock. Therefore each integer divider needs to be active. When multiple outputs are sourced from the same integer divider, the respective OE signal will enable/disable the output(s). ⁽¹⁾

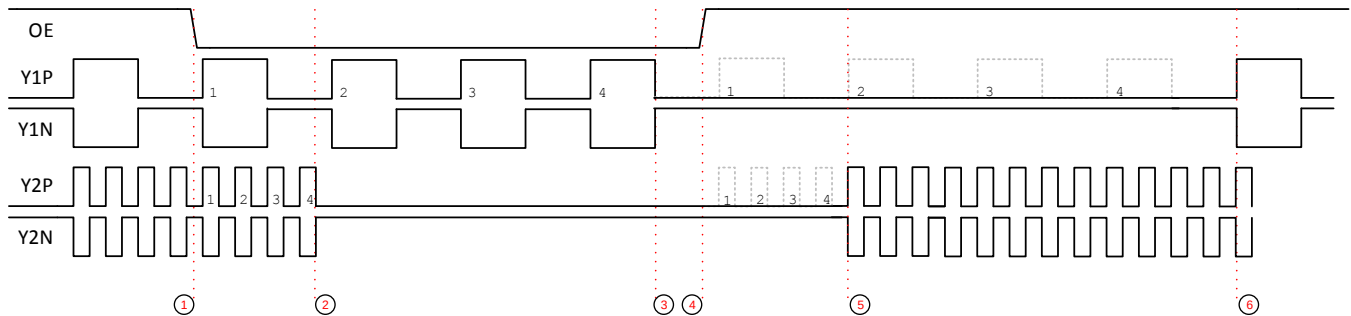
When multiple output enable signals are configured on multiple-GPIO pins, then the global output enable OE has higher priority than the individual output enable OE[4:1]. An individual output enable OE[4:1] may only be configured on a single pin.

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The individual output enable signal enables and disables the respective output in a deterministic way. Therefore the high and low level of the signal is qualified by counting four cycles of the respective output clock. The following steps can be seen in [Figure 26](#):

1. The OE falling edge which disables the outputs.
2. Transition from *logic high to logic low* / *logic low to logic high* for Y2 after four rising edges.
3. Transition from *logic high to logic low* / *logic low to logic high* for Y1 after four rising edges.
4. The OE rising edge which enables the outputs.
5. Output Y2 starts toggling after four rising edges.
6. Output Y1 starts toggling after four rising edges.

MUTE_SEL= Logic Low



MUTE_SEL= Logic High

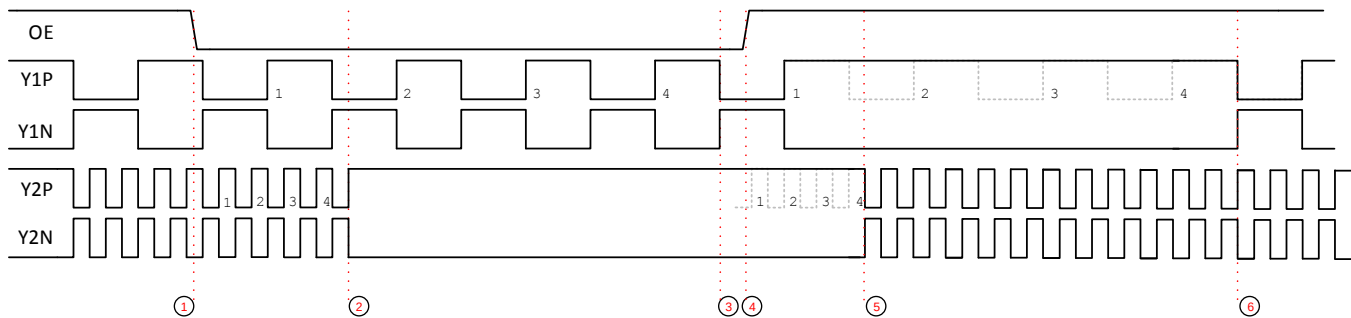


Figure 26. Individual Output Enable and Disable

NOTE

The deterministic behaviour of the individual output enable is designed for an output frequency up to 200 MHz.

8.3.5 Operation Modes

The device can operate in different modes.

Following operating modes can be set and the GPIOs configured. An operating mode change only becomes effective when it is loaded from the EEPROM after a power cycle.

Table 11. Modes of Operation

DESCRIPTION	MODE	REFSEL	EEPROMSEL	GPIO4	GPIO3	GPIO2	GPIO1
I ² C + GPIOs	Fallback	M	M	I/O	SCL	SDA	I/O
I ² C + GPIOs	0	LH	LH	I/O	SCL	SDA	I/O
OE	1	LH	LH	OE4	OE3	OE2	OE1

8.3.6 Divider Synchronization - SYNC

The output dividers can be reset in a deterministic way. This can be achieved using the [sync](#) bit or the pin 8 configured for SYNC function using [gpio0_input_sel](#) and [gpio0_dir_sel](#). The level of the pin is qualified internally using the reference frequency at the PFD. A low level will mute the outputs. A high level will synchronously release all output dividers to operation, so that all outputs share a common rising edge, see [Figure 27](#). The first rising edge can be individually delayed in steps of the respective pre-scaler period, up to 32 cycles using [ch1_sync_delay](#). This allows to compensate external delays like routing mismatch, cables or inherent delays introduced by logic gates in an FPGA design. Each channel can be included or excluded from the SYNC process using [ch1_sync_en](#). ^{(1) (2)}

For a deterministic behaviour over power-cycles seen from input to output the reference divider must be set to 1. It should not divide the reference clock nor should the reference doubler be used.

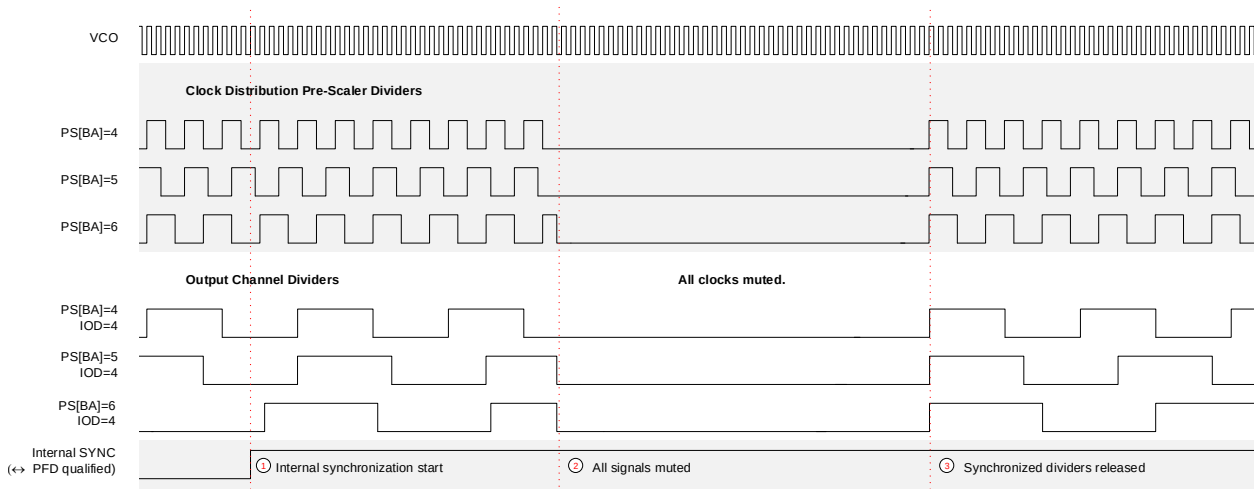


Figure 27. Divider Synchronization

- (1) [ch\[4:1\]_sync_en](#) may only be activated with an active clock source selected in [ch1_iod_mux](#) bit in the [CH1_CTRL2](#) table.
- (2) The LVCMOS bypass output Y0 is not part of the SYNC process, neither are the dividers of the PLL.

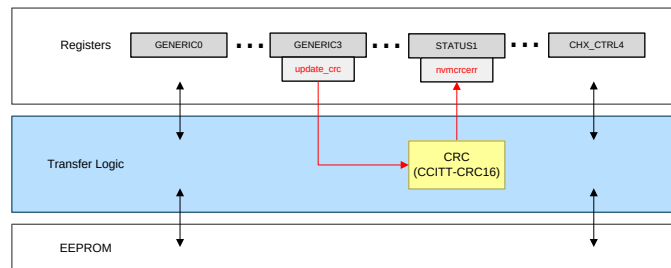
Table 12. Digital Delay Step Size

VCO FREQUENCY IN MHz	PRE-SCALER STEP IN ns		
	/4	/5	/6
2400	1.67	2.08	2.50
2457.6	1.63	2.03	2.44
2500	1.60	2.00	2.40
2800	1.43	1.79	2.14

8.3.7 EEPROM - Cyclic Redundancy Check

The device contains a cyclic redundancy check (CRC) function for reads from the EEPROM to the device registers. At start-up the EEPROM will be read internally and a CRC value calculated. One of the EEPROM words contains an earlier stored CRC value. The [stored](#) and the [actual](#) CRC value are compared and the result transferred to STATUS1 register. The CRC calculation can be triggered again by writing a '1' to the [update_crc](#) bit. A mismatch between stored and calculated CRC value is informational only and non-blocking to the device operation. Just reading back the CRC status bit and the live CRC value can speed up in-system EEPROM programming and avoid reading back each word of the EEPROM for known configurations.

The polynomial used is CCITT-CRC16: $x^{16} + x^{12} + x^5 + 1$.

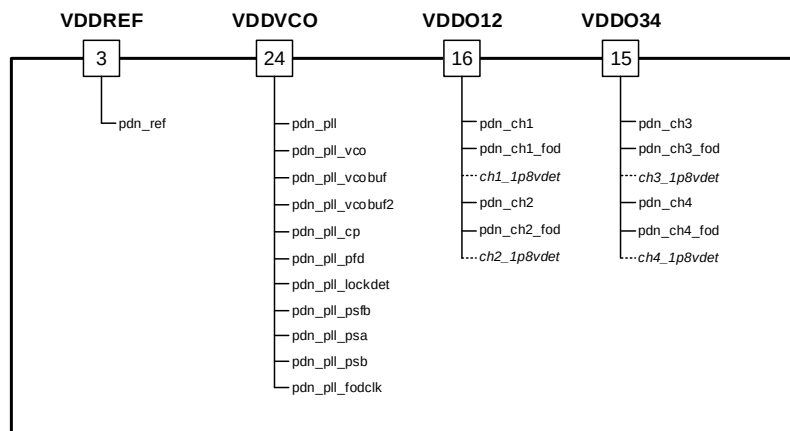

Figure 28. EEPROM CRC

8.3.8 Power Supplies

The CDCI6214 provides multiple power supply pins. Each of the power supplies supports 1.8 V, 2.5 V, or 3.3 V. Internal low-dropout regulators (LDO) source the internal blocks and allow each pin to be supplied with its individual supply voltage. The VDDREF pin supplies the control pins and the serial interface. Therefore, any pullup resistors shall be connected to the same domain as VDDREF. By default the LDOs are configured for 1.8-V $\pm 5\%$ operation.

8.3.8.1 Power Management

The device is very flexible with respect to internal power management. Each block offers a power-down bit and can be disabled to save power when the block is not required. The available bits are illustrated in Figure 29. The bypass output Y0 is connected to the `pdn_ch4` bit. Each output channel has a bit which should be adapted to the applied supply voltage, `ch[4:1]_1p8vdet`.


Figure 29. Power Management

8.4 Device Functional Modes

8.4.1 Pin Mode

In pin mode, the pins 12 and 19 are input pins which act as *individual output enable* pins. Together with pin 11 and 20, this allows for one output enable pin per output channel.

8.4.2 Serial Interface Mode

In serial interface mode, pins 12 and 19 are configured as an I²C interface.

Device Functional Modes (continued)

8.4.2.1 Fall-Back Mode

As the programming interface can be intentionally deactivated using the EEPROM, an accidental disabling of the I²C blocks further access to the device. The serial interface can be forced using the fall-back mode. To enter this mode, the user leaves pin 4 and pin 23 floating while the supply voltage is applied to VDDREF. In this mode, pin 11 is preconfigured as an input and pin 20 is configured as an output.

8.5 Programming

The CDCI6214 ultra-low power clock generator provides an I²C-compatible serial interface for register and EEPROM access. The device is compatible to standard-mode I²C at 100 kHz and the fast-mode I²C at 400-kHz clock frequency.

Table 13. I²C-Compatible Serial Interface, Slave Address Byte

7	6	5	4	3	2	1	0
Slave Address A[6:0] ⁽¹⁾							R/W# Bit ⁽²⁾

(1) The slave address consists of two sections. The hardwired MSBs A[6:2] and the software-selectable LSBs A[1:0].

(2) The R/W# bit indicates a read (1) or a write (0) transfer.

Table 14 shows the slave address decoding with respect to EEPROMSEL pin. This enables the user to avoid in-system conflicts with different configurations, as the selected EEPROM page can be reflected in the slave address least significant bit A0. Moreover a device being powered up in the silicon default, can always be expected under the default address of 0xE9 for reads (or 0xE8 for writes).

Table 14. I²C-Compatible Serial Interface, Programmable Slave Address

A6	A5	A4	A3	A2	A1	A0	EEPROMSEL	DESCRIPTION
1	1	1	0	1	0	0	MID	Device Default
					1	I2C_A0 ⁽¹⁾	LOW	EEPROM, Page 0
					1	I2C_A0 ⁽²⁾	HIGH	EEPROM, Page 1

(1) Configuration Bit in EEPROM Page 0, default value of 0.

(2) Configuration Bit in EEPROM Page 1, default value of 1.

The serial interface uses the following protocol as shown in [Figure 30](#). The slave address is followed by a word-wide register offset and a word-wide register value.

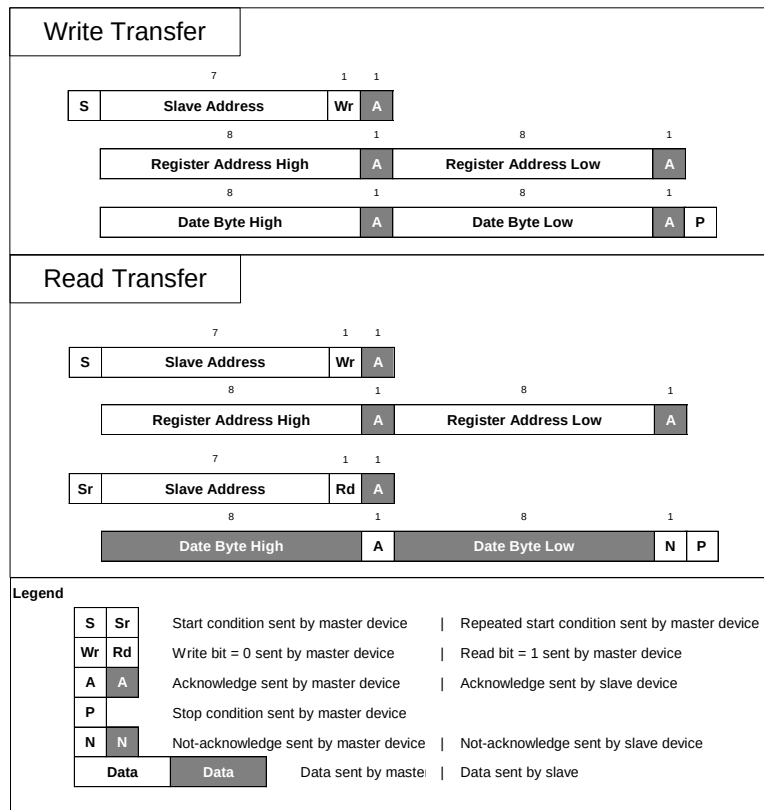


Figure 30. I²C-Compatible Serial Interface, Supported Protocol

8.5.1 Recommended Programming Procedure

TI recommends programming the registers of the device in the following way:

1. Ensure that [ee_lock](#) is set when overwriting the EEPROM.
2. Configure the voltage domain bits appropriately [ch\[4:1\]_1p8vdet](#).
3. Program register addresses in descending order from 0x44 to 0x00 including all register addresses with reserved values.

8.5.2 EEPROM Access

NOTE

The EEPROM word write access time is typically 8 ms. The EEPROM_BUSY signal indicates when the EEPROM is busy and can be observed as a status signal on a GPIO pin to optimally time the writes (for example, in [gpio4_output_sel](#)).

There are two methods to write into the internal EEPROM:

1. Register Commit
2. EEPROM Direct Access

Use the following steps to bring the device into a known state and be able to conduct the programming:

1. Power down all device supplies
2. Apply RESETN=LOW.
3. Apply REFSEL=MID (leave tri-stated).
4. Apply EEPROMSEL=MID (leave tri-stated).

5. Apply 1.8 V to all device supplies. When device operation is not required, only apply 1.8 V to VDDREF.
 6. Apply RESETN=HIGH.
 7. Use the I²C interface to configure the device using slave address 0x74. See [Table 14](#) for more details.
- In the *Register Commit* flow all bits from the device registers are copied into the EEPROM. The recommended flow is:

1. Pre-configure the device as desired, except the serial interface using [mode](#).
2. Write 1 to [recal](#) to calibrate the VCO in this operation mode.
3. Select the EEPROM page, to copy the register settings into, using [regcommit_page](#).
4. Unlock the EEPROM for write access with [ee_lock](#) = 0x5
5. Start the commit operation by writing a 1 to [regcommit](#)
6. Force a CRC update by writing a 1 to [update_crc](#).
7. Read back the calculated CRC in [nvmlcrc](#).
8. Store the read CRC value in the EEPROM by writing 0x3F to [nvmm_wr_addr](#) and then the CRC value to [nvmm_wr_data](#).

In the *EEPROM Direct Access* flow the EEPROM words are directly accessed using the address and the data bit-fields. The recommended flow is:

1. Prepare an EEPROM image consisting of 64 words.
2. Unlock the EEPROM for write access with [ee_lock](#) = 0x5
3. Write the initial address offset to the address bit-field. Write a 0x00 to [nvmm_wr_addr](#).
4. Loop through the EEPROM image from address 0 to 63 by writing each word from the image to [nvmm_wr_data](#). The EEPROM word address is automatically incremented by every write access to [nvmm_wr_data](#).



Figure 31. EEPROM Direct Access Using I²C

8.5.3 Device Defaults

The CDCI6214 contains the following defaults:

Table 15. CDCI6214 Register Defaults

ADDRESS	DEFAULT	EEPROM PAGE 0	EEPROM PAGE 1
0x46	0x00460000	0x00460000	0x00460000
0x45	0x00450000	0x00450000	0x00450000
0x44	0x00440000	0x00440000	0x00440000
0x43	0x00430020	0x00430020	0x00430020

Table 15. CDCI6214 Register Defaults (continued)

ADDRESS	DEFAULT	EEPROM PAGE 0	EEPROM PAGE 1
0x42	0x00420000	0x00420200	0x00420200
0x41	0x00410F34	0x00410F34	0x00410F34
0x40	0x0040000D	0x0040000D	0x0040000D
0x3F	0x003F0210	0x003F4210	0x003F4210
0x3E	0x003E4210	0x003E4218	0x003E4218
0x3D	0x003D1000	0x003D1500	0x003D1500
0x3C	0x003C0010	0x003C0018	0x003C0018
0x3B	0x003B0009	0x003B0061	0x003B0061
0x3A	0x003A0008	0x003A0008	0x003A0008
0x39	0x00390A65	0x00398851	0x00398851
0x38	0x00380405	0x00380409	0x00380008
0x37	0x00370004	0x00370006	0x00370000
0x36	0x00360000	0x00360000	0x00360000
0x35	0x00358000	0x00358000	0x00358000
0x34	0x00340008	0x00340008	0x00340008
0x33	0x00330A65	0x00338861	0x00338861
0x32	0x00320405	0x00320429	0x00320431
0x31	0x00310004	0x00310006	0x00310006
0x30	0x00300000	0x00300000	0x00300000
0x2F	0x002F8000	0x002F8000	0x002F8000
0x2E	0x002E0008	0x002E0008	0x002E0008
0x2D	0x002D0A65	0x002D0851	0x002D0851
0x2C	0x002C0405	0x002C0409	0x002C0010
0x2B	0x002B0004	0x002B0006	0x002B0000
0x2A	0x002A0000	0x002A0000	0x002A0000
0x29	0x00298000	0x00298000	0x00298000
0x28	0x00280008	0x00280008	0x00280008
0x27	0x00270A65	0x00270851	0x00270851
0x26	0x00260405	0x00260409	0x00260409
0x25	0x00250004	0x00250006	0x00250006
0x24	0x00240000	0x00240000	0x00240000
0x23	0x00238000	0x00238000	0x00238000
0x22	0x00220050	0x00220050	0x00220050
0x21	0x00210007	0x00210007	0x00210007
0x20	0x00200000	0x00200000	0x00200000
0x1F	0x001F1E72	0x001F1E72	0x001F1E72
0x1E	0x001E5140	0x001E5140	0x001E5140
0x1D	0x001D400A	0x001D000C	0x001D000C
0x1C	0x001C0000	0x001C0000	0x001C0000
0x1B	0x001B0000	0x001B0000	0x001B0000
0x1A	0x001A0718	0x001A0A1C	0x001A0A1C
0x19	0x00190000	0x00190406	0x00192406
0x18	0x00180601	0x00180601	0x00180601
0x17	0x00170000	0x00170595	0x00170595
0x16	0x00160000	0x00160000	0x00160000
0x15	0x00150000	0x00150000	0x00150000
0x14	0x00140000	0x00140001	0x00140001
0x13	0x00130000	0x00130000	0x00130000
0x12	0x00120000	0x0012FFFF	0x0012FFFF
0x11	0x001126C4	0x001126C4	0x001126C4
0x10	0x0010921F	0x0010921F	0x0010921F

Table 15. CDCI6214 Register Defaults (continued)

ADDRESS	DEFAULT	EEPROM PAGE 0	EEPROM PAGE 1
0xF	0x000FA037	0x000FA037	0x000FA037
0xE	0x000E0000	0x000E0000	0x000E0000
0xD	0x000D0000	0x000D0000	0x000D0000
0xC	0x000C0000	0x000C0000	0x000C0000
0xB	0x000B0000	0x000B0000	0x000B0000
0xA	0x000A0000	0x000AC964	0x000AC964
0x9	0x00090000	0x0009C964	0x0009C964
0x8	0x00080000	0x00080001	0x00080001
0x7	0x00070000	0x00070C0D	0x00070C0D
0x6	0x00060000	0x0006159F	0x000619CA
0x5	0x00050028	0x00050028	0x00050028
0x4	0x00040055	0x00040055	0x000400DD
0x3	0x00030000	0x00030000	0x00030800
0x2	0x00020053	0x00020053	0x00020053
0x1	0x00016882	0x00016865	0x00016864
0x0	0x00000000	0x00000001	0x00000000

Table 16. Default EEPROM Image

ADDRESS	Section	Word Value
0x0	Base	0xEE00
0x1		0x490F
0x2		0x0362
0x3		0x0E00
0x4		0x1400
0x5		0xC104
0x6		0x0C00
0x7		0x5000
0x8		0x0861
0x9		0x8421
0xA		0x0006
0xB		0x0000

Table 16. Default EEPROM Image (continued)

ADDRESS	Section	Word Value
0xC	Page 0	0x6501
0xD		0x5368
0xE		0xAA80
0xF		0x4382
0x10		0x0001
0x11		0x0030
0x12		0x4500
0x13		0x79C9
0x14		0x8000
0x15		0x0C00
0x16		0x1200
0x17		0x2904
0x18		0x0002
0x19		0x3002
0x1A		0x4800
0x1B		0xA410
0x1C		0x0008
0x1D		0xC008
0x1E		0x2000
0x1F		0x1045
0x20		0x0033
0x21		0x0020
0x22		0x8003
0x23		0x4104
0x24		0x39CA
0x25		0x0000

Table 16. Default EEPROM Image (continued)

ADDRESS	Section	Word Value
0x26	Page 1	0x6400
0x27		0x5368
0x28		0xEE80
0x29		0x4382
0x2A		0x0001
0x2B		0x0030
0x2C		0x4500
0x2D		0x79C9
0x2E		0x8000
0x2F		0x0C00
0x30		0x1200
0x31		0x2904
0x32		0x0002
0x33		0x0002
0x34		0x8000
0x35		0xA400
0x36		0x0008
0x37		0xC008
0x38		0x2000
0x39		0x1046
0x3A		0x0033
0x3B		0x0020
0x3C		0x0000
0x3D		0x4004
0x3E		0x39CA
0x3F		0xC964

CDCI6214

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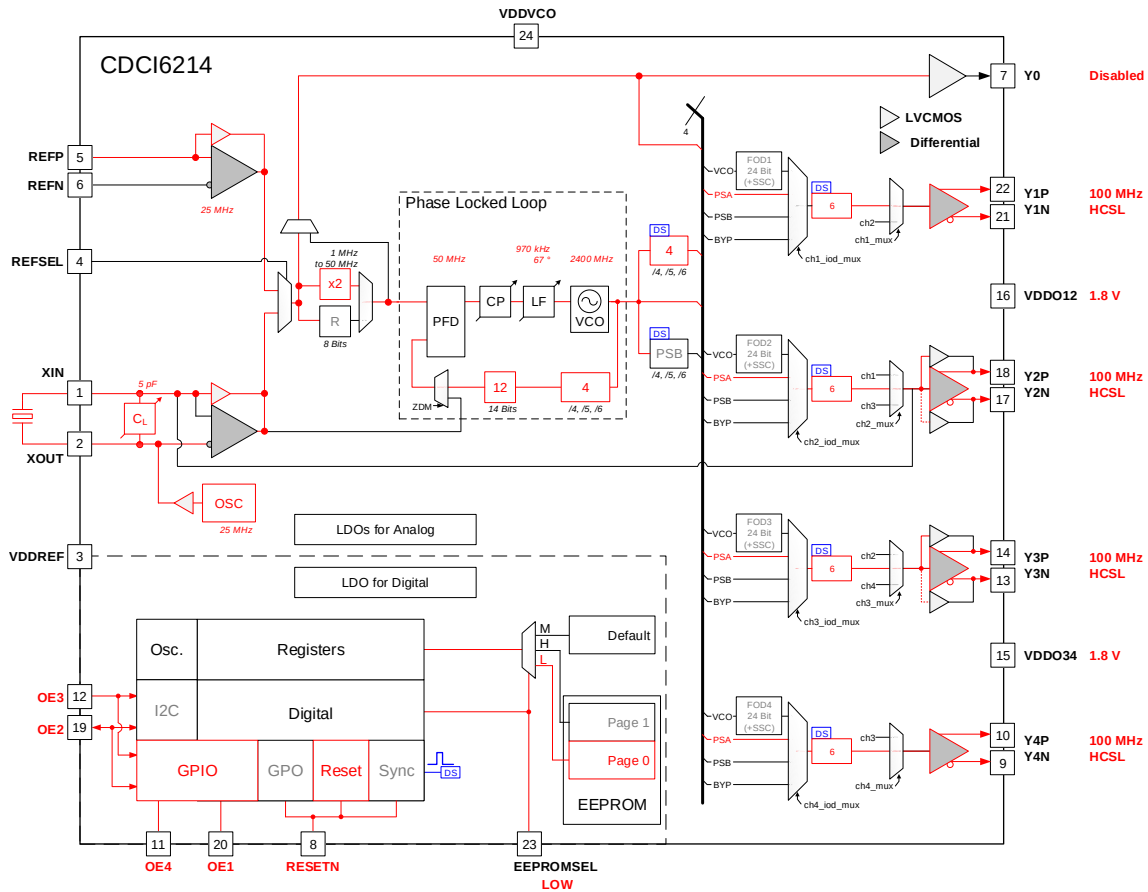


Figure 32. CDCI6214 - Pre-Configured EEPROM Page 0

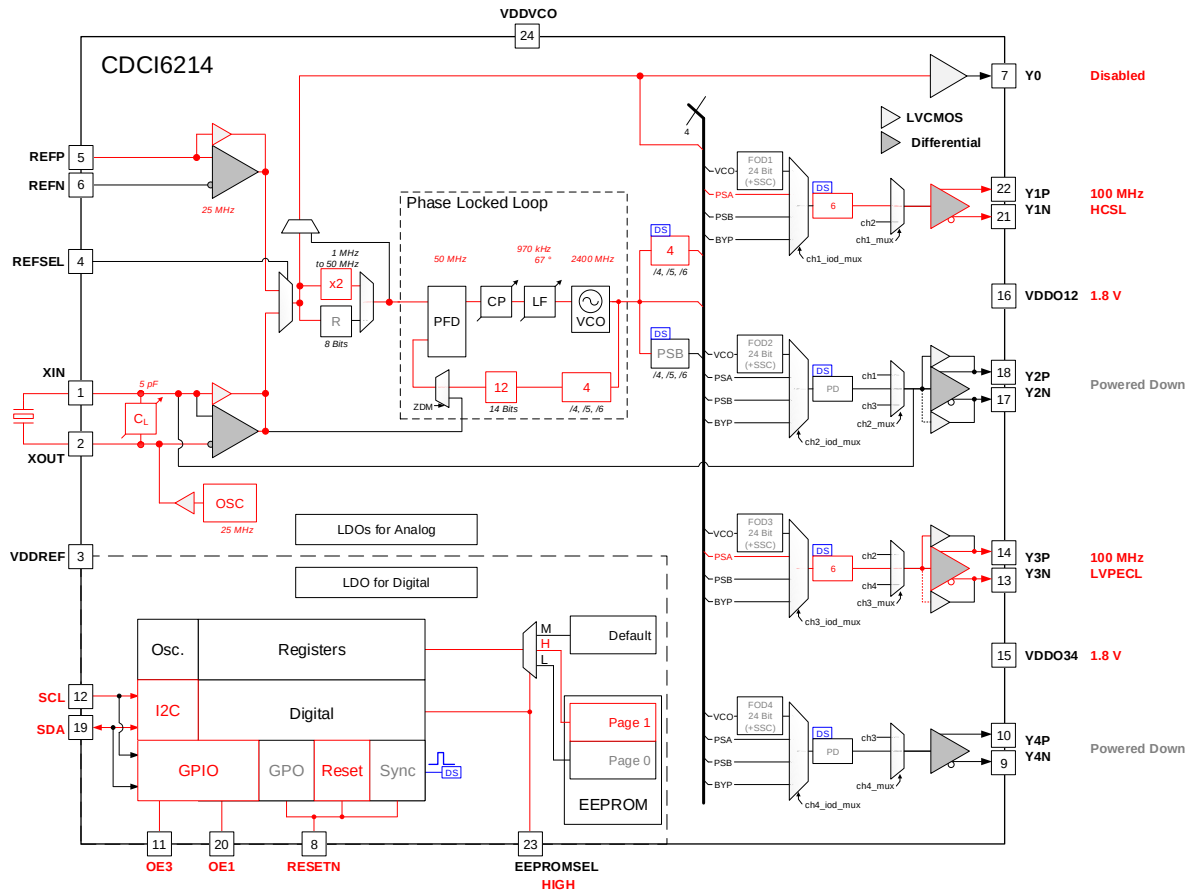


Figure 33. CDCI6214 - Pre-Configured EEPROM Page 1

8.6 Register Maps

8.6.1 CDCl6214 Registers

[Table 17](#) lists the memory-mapped registers for the CDCl6214.

NOTE

All register offset addresses not listed in [Table 17](#) should be considered as reserved locations and the register contents should not be modified.

NOTE

All bit-field combinations not listed in the description column should be considered as reserved combinations and should only be programmed using the given values.

Table 17. CDCl6214 Registers

ADDRESS	ACRONYM	REGISTER NAME	SECTION
0h	GENERIC0	Generic setting, device operation mode, synchronization, control pins, reset, and power down.	Go
1h	GENERIC1	Generic settings, GPIO input signal selection.	Go
2h	GENERIC2	Generic settings, GPIO output signal selection.	Go
3h	GENERIC3	Generic settings, EEPROM and frequency increment / decrement.	Go
4h	POWER0	Power-down bits, output channels.	Go
5h	POWER1	Power-down bits, phase-locked-loop.	Go
6h	STATUS0	Status information, calibration bus.	Go
7h	STATUS1	Status information, PLL lock and EEPROM.	Go
8h	STATUS2	Status information, miscellaneous	Go
9h	STATUS3	Status information, live CRC of EEPROM	Go
Ah	EEPROM0	EEPROM, stored CRC of EEPROM	Go
Bh	EEPROM1	EEPROM, direct access read address	Go
Ch	EEPROM2	EEPROM, direct access read data	Go
Dh	EEPROM3	EEPROM, direct access write address	Go
Eh	EEPROM4	EEPROM, direct access write data	Go
Fh	STARTUP0	Start-up configuration, EEPROM lock, auto-calibration, and I2C glitch filter	Go
10h	STARTUP1	Start-up configuration, digital state machine counters	Go
11h	STARTUP2	Start-up configuration, digital state machine counters	Go
18h	REV0	Revision ID	Go
1Ah	INPUT0	Input reference, buffer configuration, and crystal oscillator controls.	Go
1Bh	INPUT1	Input reference, reference divider, and bypass buffers.	Go
1Ch	INPUT_DBG0	Input reference debug, status pin buffers.	Go
1Dh	PLL0	PLL, feedback dividers.	Go
1Eh	PLL1	PLL, charge pump current and clock distribution pre-scaler dividers.	Go
1Fh	PLL2	PLL, loop filter configuration	Go
21h	PLL4	PLL, lock detector and PFD delay	Go
23h	CH1_CTRL0	Output channel 1, fractional divider.	Go
24h	CH1_CTRL1	Output channel 1, fractional divider.	Go
25h	CH1_CTRL2	Output channel 1, integer divider and mux control.	Go
26h	CH1_CTRL3	Output channel 1, synchronization, digital delay, output buffer, mux and mute controls.	Go
27h	CH1_CTRL4	Output channel 1, divider glitch-less enable and spread spectrum controls.	Go
28h	CH1_CTRL5	Output channel 1 , fractional divider calibration.	Go

Table 17. CDCl6214 Registers (continued)

ADDRESS	ACRONYM	REGISTER NAME	SECTION
29h	CH2_CTRL0	Output channel 2, fractional divider.	Go
2Ah	CH2_CTRL1	Output channel 2, fractional divider.	Go
2Bh	CH2_CTRL2	Output channel 2, integer divider and mux control.	Go
2Ch	CH2_CTRL3	Output channel 2, synchronization, digital delay, output buffer, mux and mute controls.	Go
2Dh	CH2_CTRL4	Output channel 2, divider glitch-less enable and spread spectrum controls.	Go
2Eh	CH2_CTRL5	Output channel 2, fractional divider calibration.	Go
2Fh	CH3_CTRL0	Output channel 3, fractional divider.	Go
30h	CH3_CTRL1	Output channel 3, fractional divider.	Go
31h	CH3_CTRL2	Output channel 3, integer divider and mux control.	Go
32h	CH3_CTRL3	Output channel 3, synchronization, digital delay, output buffer, mux and mute controls.	Go
33h	CH3_CTRL4	Output channel 3, divider glitch-less enable and spread spectrum controls.	Go
34h	CH3_CTRL5	Output channel 3, fractional divider calibration.	Go
35h	CH4_CTRL0	Output channel 4, fractional divider.	Go
36h	CH4_CTRL1	Output channel 4, fractional divider.	Go
37h	CH4_CTRL2	Output channel 4, integer divider and mux control.	Go
38h	CH4_CTRL3	Output channel 4, synchronization, digital delay, output buffer, mux and mute controls.	Go
39h	CH4_CTRL4	Output channel 4, divider glitch-less enable and spread spectrum controls.	Go
3Ah	CH4_CTRL5	Output channel 4, fractional divider calibration.	Go
3Bh	CHX_CTRL0	Output channels, generic clock distribution and bypass output controls.	Go
3Ch	CHX_CTRL1	Output channels, common fractional divider controls.	Go
3Dh	CHX_CTRL2	Output channels, common fractional divider controls.	Go
3Eh	CHX_CTRL3	Output channels, common fractional divider controls.	Go
3Fh	CHX_CTRL4	Output channels, common fractional divider controls.	Go

Complex bit access types are encoded to fit into small table cells. [Table 18](#) shows the codes that are used for access types in this section.

Table 18. CDCl6214 Access Type Codes

ACCESS TYPE	CODE	DESCRIPTION
READ TYPE		
R	R	Read
RC	C R	to Clear Read
WRITE TYPE		
W	W	Write
WEX	W	Write
WMC	W	Write
WPD	W	Write
WSC	W	Write
WST	W	Write
RESET OR DEFAULT VALUE		
-n		Value after reset or the default value

8.6.1.1 GENERIC0 Register (Address = 0h) [reset = 0h]

GENERIC0 is shown in [Figure 34](#) and described in [Table 19](#).

Return to [Summary Table](#).

Figure 34. GENERIC0 Register

15	14	13	12	11	10	9	8
i2c_a0	gpio0_input_sel	gpio4_dir_sel	gpio1_dir_sel	gpio0_dir_sel	zdm_clocksel	zdm_muxsel	zdm_mode
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED	pll_rst_lockdet	sync	recal	resetsn_soft	swrst	powerdown	mode
R/W-0h	R/W-0h	R/WSC-0h	R/WSC-0h	R/W-0h	R/WSC-0h	R/WPD-0h	R/W-0h

Table 19. GENERIC0 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15	i2c_a0	R/W	0h	When regcommit is used to program an EEPROM page, using regcommit_page , this defines the LSB of the I ² C slave address. When a configuration is loaded into the registers from an EEPROM page, this represents the saved LSB bit.
14	gpio0_input_sel	R/W	0h	Input signal select for GPIO0, Pin 8. 0h = RESETN 1h = SYNC
13	gpio4_dir_sel	R/W	0h	GPIO4 direction select. 0h = Input 1h = Output
12	gpio1_dir_sel	R/W	0h	GPIO1 direction select. 0h = Input 1h = Output
11	gpio0_dir_sel	R/W	0h	Direction select for Pin 8. 0h = Input 1h = Output
10	zdm_clocksel	R/W	0h	Selects the internal or external clock for calibration, in the ZDM mode. In non-ZDM mode, always internal clock will be selected and this register doesn't have any meaning. SM signal. Refer Digital Review Document 0h = Internal Feedback 1h = External Feedback
9	zdm_muxsel	R/W	0h	Mux select for ZDM or non-ZDM loop. 0h = 0 1h = 1
8	zdm_mode	R/W	0h	Zero Delay Mode 0h = ZDM Off 1h = ZDM On
7	RESERVED	R/W	0h	Reserved.
6	pll_rst_lockdet	R/W	0h	Reset (active high) to PLL lock detect circuit.
5	sync	R/WSC	0h	Generates sync pulse (for output decoder). This is a self clearing register bit and writing '1' will create the SYNC pulse.
4	recal	R/WSC	0h	Self clearing bit. Writing '1' will do the re-calibration. For example - after the configuration followed by calibration if '1' is written to this register the calibration engine will start with the current capcode and cross code.

Table 19. GENERIC0 Register Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
3	resetsn_soft	R/W	0h	Configure the pin RESETN/SYNC as a soft reset. 0h = Hard Reset (reset state machines and registers) 1h = Soft Reset (state machines only, register content stays as is)
2	swrst	R/WSC	0h	Soft reset bit. This is a self clearing bit. Writing a '0' has no effect and writing a '1' creates a reset pulse which resets the digital logic except the programmable registers. Also- this soft reset has similar effect on digital logic as hard reset (RESETN/SYNC). Soft reset will restart the configuraton and calibration.
1	powerdown	R/WD	0h	Analog Power Down. 0h = Active 1h = Power down
0	mode	R/W	0h	Mode of Operation. 0h = Serial Interface, I2C 1h = Pin Mode, Output Enable

8.6.1.2 GENERIC1 Register (Address = 1h) [reset = 6A32h]

GENERIC1 is shown in [Figure 35](#) and described in [Table 20](#).

Return to [Summary Table](#).

Figure 35. GENERIC1 Register

15	14	13	12	11	10	9	8
fod_size						ref_mux_src	ref_mux
R/W-1Ah						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
gpio4_input_sel				gpio1_input_sel			
R/W-3h				R/W-2h			

Table 20. GENERIC1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-10	fod_size	R/W	1Ah	This sets the FOD increment/decrement size step. Refer FOD Calculation document to calculate FOD Step Size (which is dependent upon Output Frequency). Step Size of 26 would set step at 0.1ppm/step for 19.2-MHz output.
9	ref_mux_src	R/W	0h	Reference mux control signal source. 0h = Pin 1h = ref_mux bit-field
8	ref_mux	R/W	0h	Reference mux bit override. 0h = XIN 1h = REF
7-4	gpio4_input_sel	R/W	3h	GPIO4 output signal select. <i>Do not choose the same signal on gpio1_input_sel.</i> 0h = FREQ_INC 1h = FREQ_DEC 2h = OE 3h = SSC_EN 4h = OE1 5h = OE2 6h = OE3 7h = OE4
3-0	gpio1_input_sel	R/W	2h	GPIO1 output signal select. <i>Do not choose the same signal on gpio4_input_sel.</i> 0h = FREQ_INC 1h = FREQ_DEC 2h = OE 3h = SSC_EN 4h = OE1 5h = OE2 6h = OE3 7h = OE4

8.6.1.3 GENERIC2 Register (Address = 2h) [reset = 53h]

GENERIC2 is shown in [Figure 36](#) and described in [Table 21](#).

Return to [Summary Table](#).

Figure 36. GENERIC2 Register

15	14	13	12	11	10	9	8
RESERVED	iod_size	RESERVED				gpio0_output_sel	
R/W-0h	R/W-0h	R/W-0h				R/W-0h	
7	6	5	4	3	2	1	0
		gpio4_output_sel				gpio1_output_sel	
		R/W-5h				R/W-3h	

Table 21. GENERIC2 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15	RESERVED	R/W	0h	Reserved.
14	iod_size	R/W	0h	Increment size for IOD (0 h = step size 1 ; 1h = Step size 100) 0h = 1 1h = 10
13-12	RESERVED	R/W	0h	Reserved.
11-8	gpio0_output_sel	R/W	0h	GPIO0, Pin 8, output select , 0h = PLL_LOCK 1h = XTAL_OSC 2h = CAL_DONE 3h = CONF_DONE 4h = SYNC_DONE 5h = EEPROM_BUSY 6h = EEPROM_Y12 7h = EEPROM_M12 8h = I2C_LSB 9h = CLK_FSM Ah = CLK_PFD_REF Bh = CLK_PFD_FB Ch = BUF_SYNC Dh = BUF_SCL Eh = BUF_SDA

Table 21. GENERIC2 Register Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-4	gpio4_output_sel	R/W	5h	GPIO4 , output select , 0h = PLL_LOCK 1h = XTAL_OSC 2h = CAL_DONE 3h = CONF_DONE 4h = SYNC_DONE 5h = EEPROM_BUSY 6h = EEPROM_Y12 7h = EEPROM_M12 8h = I2C_LSB 9h = CLK_FSM Ah = CLK_PFD_REF Bh = CLK_PFD_FB Ch = BUF_SYNC Dh = BUF_SCL Eh = BUF_SDA
3-0	gpio1_output_sel	R/W	3h	GPIO1 , output select , 0h = PLL_LOCK 1h = XTAL_OSC 2h = CAL_DONE 3h = CONF_DONE 4h = SYNC_DONE 5h = EEPROM_BUSY 6h = EEPROM_Y12 7h = EEPROM_M12 8h = I2C_LSB 9h = CLK_FSM Ah = CLK_PFD_REF Bh = CLK_PFD_FB Ch = BUF_SYNC Dh = BUF_SCL Eh = BUF_SDA

8.6.1.4 GENERIC3 Register (Address = 3h) [reset = 0h]

GENERIC3 is shown in [Figure 37](#) and described in [Table 22](#).

Return to [Summary Table](#).

Figure 37. GENERIC3 Register

15	14	13	12	11	10	9	8
disable_crc	update_crc	nvmcommit	regcommit	regcommit_page	mask_inc_dec_iod_ch4	mask_inc_dec_iod_ch3	mask_inc_dec_iod_ch2
R/W-0h	R/WMC-0h	R/WSC-0h	R/WSC-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
mask_inc_dec_iod_ch1	mask_inc_dec_fod_ch4	mask_inc_dec_fod_ch3	mask_inc_dec_fod_ch2	mask_inc_dec_fod_ch1	fod_iod_dec	fod_iod_inc	fod_iod_reg_mode
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/WSC-0h	R/WSC-0h	R/W-0h

Table 22. GENERIC3 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15	disable_crc	R/W	0h	Disable the CRC computation. However if Page is selected CRC will happen after PoR (power on reset from analog). For example- after the calibration if this bit is set to '1' and apply a soft reset (or reset through pin) the configuration will bypass the CRC computation.
14	update_crc	R/WMC	0h	This is a self clearing register bit. Writing a '1' will cause the re-computation of CRC. The computed CRC can be read from the live CRC (nvmlrc) register after the status bit nvmbusy = 0.
13	nvmcommit	R/WSC	0h	NVM Commit to Registers. The NVMCOMMIT bit is used to initiate a transfer of the on-chip EEPROM contents to internal registers. The transfer happens automatically after reset or when NVMCOMMIT is set to 1. The NVMCOMMIT bit is automatically cleared to 0. The I2C registers cannot be read while a NVM Commit operation is taking place. The NVMCOMMIT operation can only be carried out when the Always On Clock is active. The Always On Clock can be kept running after lock by setting the AONAFTERLOCK bit or by forcing the Always On Clock Enable using the CLKDBG1 register.
12	regcommit	R/WSC	0h	REG Commit to NVM SRAM Array. The REGCOMMIT bit is used to initiate a transfer from the on-chip registers back to the corresponding location in the NVM SRAM Array. The REGCOMMIT bit is automatically cleared to 0 when the transfer is complete. The particular page of SRAM used as the destination for the transfer is selected by the REGCOMMIT_PAGE register.
11	regcommit_page	R/W	0h	Decide which page of EEPROM to use for the Register/NVM commit operations. Note= this register is used only after the initial power-up configuration from EEPROM if any. Once power-up configuration is done with the page chosen by EEPROMSEL the value of this register will be used for subsequent configurations using Register/NVM commit operations. 0h = Page 0 1h = Page 1
10	mask_inc_dec_iod_ch4	R/W	0h	Bit mask for GPIO input function FREQ_INC, FREQ_DEC. Increase or decrease using step size defined by iod_size and fod_size respectively. 0h = IOD CH4 excluded 1h = IOD CH4 included
9	mask_inc_dec_iod_ch3	R/W	0h	Bit mask for GPIO input function FREQ_INC, FREQ_DEC. Increase or decrease using step size defined by iod_size and fod_size respectively. 0h = IOD CH3 excluded 1h = IOD CH3 included

Table 22. GENERIC3 Register Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
8	mask_inc_dec_iod_ch2	R/W	0h	Bit mask for GPIO input function FREQ_INC, FREQ_DEC. Increase or decrease using step size defined by iod_size and fod_size respectively. 0h = IOD CH2 excluded 1h = IOD CH2 included
7	mask_inc_dec_iod_ch1	R/W	0h	Bit mask for GPIO input function FREQ_INC, FREQ_DEC. Increase or decrease using step size defined by iod_size and fod_size respectively. 0h = IOD CH1 excluded 1h = IOD CH1 included
6	mask_inc_dec_fod_ch4	R/W	0h	Bit mask for GPIO input function FREQ_INC, FREQ_DEC. Increase or decrease using step size defined by iod_size and fod_size respectively. 0h = FOD CH4 excluded 1h = FOD CH4 included
5	mask_inc_dec_fod_ch3	R/W	0h	Bit mask for GPIO input function FREQ_INC, FREQ_DEC. Increase or decrease using step size defined by iod_size and fod_size respectively. 0h = FOD CH3 excluded 1h = FOD CH3 included
4	mask_inc_dec_fod_ch2	R/W	0h	Bit mask for GPIO input function FREQ_INC, FREQ_DEC. Increase or decrease using step size defined by iod_size and fod_size respectively. 0h = FOD CH2 excluded 1h = FOD CH2 included
3	mask_inc_dec_fod_ch1	R/W	0h	Bit mask for GPIO input function FREQ_INC, FREQ_DEC. Increase or decrease using step size defined by iod_size and fod_size respectively. 0h = FOD CH1 excluded 1h = FOD CH1 included
2	fod_iod_dec	R/WSC	0h	Register decrement for FOD/IOD, writing 1 decrements the FOD/IOD word by the fod_size/iod_size
1	fod_iod_inc	R/WSC	0h	Register increment for FOD/IOD, writing 1 increments the FOD/IOD word by the fod_size/iod_size
0	fod_iod_reg_mode	R/W	0h	Enable increment/decrement for FOD/IOD controlled by writing registers fod_iod_inc/fod_iod_dec rather than through pins 0h = Pin 1h = Reg

8.6.1.5 POWER0 Register (Address = 4h) [reset = 54h]

POWER0 is shown in [Figure 38](#) and described in [Table 23](#).

Return to [Summary Table](#).

Figure 38. POWER0 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
pdn_ch4	pdn_ch4_fod	pdn_ch3	pdn_ch3_fod	pdn_ch2	pdn_ch2_fod	pdn_ch1	pdn_ch1_fod
R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R/W-0h	R/W-0h

Table 23. POWER0 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-8	RESERVED	R/W	0h	Reserved.
7	pdn_ch4	R/W	0h	Powers Down CH4 LDO. 0h = Active 1h = Power down
6	pdn_ch4_fod	R/W	1h	Powers Down CH4 FOD. 0h = Active 1h = Power down
5	pdn_ch3	R/W	0h	Powers Down CH3 LDO. 0h = Active 1h = Power down
4	pdn_ch3_fod	R/W	1h	Powers Down CH3 FOD. 0h = Active 1h = Power down
3	pdn_ch2	R/W	0h	Powers Down CH2 LDO. 0h = Active 1h = Power down
2	pdn_ch2_fod	R/W	1h	Powers Down CH2 FOD. 0h = Active 1h = Power down
1	pdn_ch1	R/W	0h	Powers Down CH1 LDO. 0h = Active 1h = Power down
0	pdn_ch1_fod	R/W	0h	Powers Down CH1 FOD. 0h = Active 1h = Power down

8.6.1.6 POWER1 Register (Address = 5h) [reset = 30h]

POWER1 is shown in Figure 39 and described in Table 24.

Return to [Summary Table](#).

Figure 39. POWER1 Register

15	14	13	12	11	10	9	8
RESERVED					pdn_pll_vcobuf 2	pdn_pll_vco	pdn_pll_vcobuf
R/W-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
pdn_pll_cp	pdn_pll_lockdet	pdn_pll_psfbb	pdn_pll_psfba	pdn_pll_fodclk	pdn_pll_pfd	pdn_pll_psfb	pdn_ref
R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 24. POWER1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-11	RESERVED	R/W	0h	Reserved.
10	pdn_pll_vcobuf2	R/W	0h	Power down of VCO buffer LDO. 0h = Active 1h = Power down
9	pdn_pll_vco	R/W	0h	Power down of VCO LDO. 0h = Active 1h = Power down
8	pdn_pll_vcobuf	R/W	0h	Power down of VCO buffer. 0h = Active 1h = Power down
7	pdn_pll_cp	R/W	0h	Power down of charge pump LDO. 0h = Active 1h = Power down
6	pdn_pll_lockdet	R/W	0h	Power down of PLL lock detector. 0h = Active 1h = Power down
5	pdn_pll_psfbb	R/W	1h	Power down of PLL feedback pre-scaler. 0h = Active 1h = Power down
4	pdn_pll_psfba	R/W	1h	Active low enable of prescaler-a. Active (low) during PoR and '1' later. 1h = Power Down PFD. 0h = Otherwise. SM Signal. Refer Digital Review Document
3	pdn_pll_fodclk	R/W	0h	Active low enable for clock path output to all FODs. Active (low) during PoR and '1' later. 1h = Power Down PFD. 0h = Otherwise. SM Signal. Refer Digital Review Document
2	pdn_pll_pfd	R/W	0h	Active low enable of PFD. Inactive (high) till calibration and '0' afterwards. 1h = Power Down PFD. 0h = Otherwise. SM Signal. Refer Digital Review Document
1	pdn_pll_psfb	R/W	0h	Active low enable of prescaler. Active (low) during PoR and '1' later. 1h = Powers Down PS, 0h = Otherwise. SM Signal. Refer Digital Review Document
0	pdn_ref	R/W	0h	Powers Down Input Path LDO. Kill Switch. Do not use. 1h = PD, 0h = Otherwise.

8.6.1.7 STATUS0 Register (Address = 6h) [reset = 0h]

STATUS0 is shown in [Figure 40](#) and described in [Table 25](#).

Return to [Summary Table](#).

Figure 40. STATUS0 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
cal_status															
R-0h															

Table 25. STATUS0 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	cal_status	R	0h	Calibration word.

8.6.1.8 STATUS1 Register (Address = 7h) [reset = 0h]

STATUS1 is shown in [Figure 41](#) and described in [Table 26](#).

Return to [Summary Table](#).

Figure 41. STATUS1 Register

15	14	13	12	11	10	9	8
RESERVED				lock_det_a	pll_vco_cal_ready	nvm_rd_error	nvm_wr_error
R-0h				R-0h	R-0h	RC-0h	RC-0h
7	6	5	4	3	2	1	0
rd_error	wr_error	nvmrcerr	nvmbusy	cal_done	config_done	unlock_s	lock_det
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R/WEX-0h	R-0h

Table 26. STATUS1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-12	RESERVED	R	0h	Reserved.
11	lock_det_a	R	0h	Analog lock detect
10	pll_vco_cal_ready	R	0h	VCO Buffer LDO POR can be read through this register
9	nvm_rd_error	RC	0h	Occurs when any NVM operation is issued during Read Phase of the NVM. Read Phase of the NVM includeS CRC calculation or a simple read through RD NVM Addr/Data registers from any NVM location or a NVM commit operation
8	nvm_wr_error	RC	0h	Occurs when any NVM operation is issued during Write Phase of the NVM. Write Phase of the NVM includes a simple write into any NVM location through WR NVM Addr/Data registers or a Register Commit operation
7	rd_error	R	0h	Reading using the I2C interface with an address above the address of the last register gives this error.
6	wr_error	R	0h	Writing using the I2C interface with an address above the address of the last register gives this error.
5	nvmrcerr	R	0h	NVM CRC Error Indication. The NVMCRCERR bit is set to 1 if a CRC Error has been detected when reading back from on-chip EEPROM during device configuration. This bit will be cleared when [TBD]
4	nvmbusy	R	0h	NVM Program Busy Indication. The NVMBUSY bit is 1 during an on-chip EEPROM Erase/Program cycle. While NVMBUSY is 1 the on-chip EEPROM cannot be accessed. When the NVM operation is completed this bit will be cleared. NVM related operations are REGcommit NVMcommit CRC calculation or simple Read/Write through RD/WR NVM
3	cal_done	R	0h	1h = Calibration (Two rounds of Amplitude followed by calibration) is done.
2	config_done	R	0h	1 h = Configuration (CRC Check followed by transfer of EEPROM to registers) is done.
1	unlock_s	R/WEX	0h	Lock Detect Sticky Bit. This indicates the loss of lock of the PLL and this is cleared only by re-calibration or a hard reset through RESETN/SYNC pin 0h = locked 1h = unlocked
0	lock_det	R	0h	When the calibration is done frequency may or may not be locked. 1h = Frequency is locked. 0h = Otherwise 0h = unlocked 1h = locked

8.6.1.9 STATUS2 Register (Address = 8h) [reset = 0h]

STATUS2 is shown in [Figure 42](#) and described in [Table 27](#).

Return to [Summary Table](#).

Figure 42. STATUS2 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
misc_status															
R-0h															

Table 27. STATUS2 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	misc_status	R	0h	Miscellaneous status word.

8.6.1.10 STATUS3 Register (Address = 9h) [reset = 0h]

STATUS3 is shown in [Figure 43](#) and described in [Table 28](#).

Return to [Summary Table](#).

Figure 43. STATUS3 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
nvmlcrc															
R-0h															

Table 28. STATUS3 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	nvmlcrc	R	0h	The NVMLCRC register holds the Live CRC byte that has been calculated while reading on-chip EEPROM.

8.6.1.11 EEPROM0 Register (Address = Ah) [reset = 0h]

EEPROM0 is shown in [Figure 44](#) and described in [Table 29](#).

Return to [Summary Table](#).

Figure 44. EEPROM0 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
nvmscrc															
R-0h															

Table 29. EEPROM0 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	nvmscrc	R	0h	Stored CRC value. This value is used to compare with the computed CRC and to update the crc status bit

8.6.1.12 EEPROM1 Register (Address = Bh) [reset = 0h]

EEPROM1 is shown in [Figure 45](#) and described in [Table 30](#).

Return to [Summary Table](#).

Figure 45. EEPROM1 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED		nvm_rd_addr					
R/W-0h		R/W-0h					

Table 30. EEPROM1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-6	RESERVED	R/W	0h	Reserved.
5-0	nvm_rd_addr	R/W	0h	Writing an address into the NVM WR Address starts the read loop. This register will contain the data read from the EEPROM at the address provided by the NVM WR Address. The address is auto-incremented and subsequent read from the NVM RD Data register will give the data from the next EEPROM location.

8.6.1.13 EEPROM2 Register (Address = Ch) [reset = 0h]

EEPROM2 is shown in [Figure 46](#) and described in [Table 31](#).

Return to [Summary Table](#).

Figure 46. EEPROM2 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
nvm_rd_data															
R-0h															

Table 31. EEPROM2 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	nvm_rd_data	R	0h	Reading from this register will return the data present at the EEPROM from the immediate next address location than what was programmed in the NVM RD Address register since writing into NVM RD Address register already returned the data from EEPROM from the written address. Subsequent read from this register will cause the address to be auto-incremented and cause a read from the next EEPROM location.

8.6.1.14 EEPROM3 Register (Address = Dh) [reset = 0h]

EEPROM3 is shown in [Figure 47](#) and described in [Table 32](#).

Return to [Summary Table](#).

Figure 47. EEPROM3 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				nvm_wr_addr			
R/W-0h				R/W-0h			

Table 32. EEPROM3 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-6	RESERVED	R/W	0h	Reserved.
5-0	nvm_wr_addr	R/W	0h	Writing an address into the NVM WR Address starts the write loop. But Writing a data into the NVM WR Data register will program the EEPROM with that data at the address provided by writing into NVM WR Address initially.

8.6.1.15 EEPROM4 Register (Address = Eh) [reset = 0h]

EEPROM4 is shown in [Figure 48](#) and described in [Table 33](#).

Return to [Summary Table](#).

Figure 48. EEPROM4 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
nvm_wr_data															
R/W-0h															

Table 33. EEPROM4 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	nvm_wr_data	R/W	0h	Writing a data into this register will program the EEPROM with the written data at the address given by NVM WR Address. Subsequent write into this register will cause the address to be auto-incremented and cause a program at the next EEPROM location.

8.6.1.16 STARTUP0 Register (Address = Fh) [reset = 37h]

STARTUP0 is shown in [Figure 49](#) and described in [Table 34](#).

Return to [Summary Table](#).

Figure 49. STARTUP0 Register

15	14	13	12	11	10	9	8
ee_lock				RESERVED			zdm_auto
R/W-0h				R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
bypass_cal	bypass_config	cal_mute	shift_left		gpio3_gf_en	gpio2_gf_en	acal_en
R/W-0h	R/W-0h	R/W-1h	R/W-2h		R/W-1h	R/W-1h	R/W-1h

Table 34. STARTUP0 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-12	ee_lock	R/W	0h	Locks EEPROM for regcommit and EEPROM write operations. To unlock, write 5h, any other value to lock.
11-9	RESERVED	R/W	0h	Reserved.
8	zdm_auto	R/W	0h	Setting this bit 1 will allow state machine to control the value of pll_ndiv and pll_psfb internally in Normal/ZDM mode of calibration. If set 0 the user has to manually program the pll_ndiv and pll_psfb
7	bypass_cal	R/W	0h	Bypass the calibration. By default two rounds of calibrations (AC followed by FC) will be done. Setting this bit to 1 will bypass the calibration.
6	bypass_config	R/W	0h	Bypass the configuration. Note that on PoR this bit is zero and hence configuration will happen. However after the first configuration this bit can be set and apply the soft/pin reset so that configuration will be bypassed
5	cal_mute	R/W	1h	Mute the output during the calibration. 0h = Outputs stay active 1h = Outputs muted
4-3	shift_left	R/W	2h	Divide the ref clock (PFD clock) during calibration by 2 to the power of value 0h = 1 1h = 2 2h = 4 3h = 8
2	gpio3_gf_en	R/W	1h	Enable the glitch filter for SCL, GPIO3. 0h = Disabled 1h = Enabled
1	gpio2_gf_en	R/W	1h	Enable the glitch filter for SDA, GPIO2. 0h = Disabled 1h = Enabled
0	acal_en	R/W	1h	Enable automatic frequency calibration at power-up or EEPROM re-load. 0h = Disabled 1h = Enabled

8.6.1.17 STARTUP1 Register (Address = 10h) [reset = 921Fh]

STARTUP1 is shown in [Figure 50](#) and described in [Table 35](#).

Return to [Summary Table](#).

Figure 50. STARTUP1 Register

15	14	13	12	11	10	9	8
pll_lock_dly					ac_init_dly		
R/W-12h					R/W-10h		
7	6	5	4	3	2	1	0
ac_init_dly				cp_dly			
R/W-10h				R/W-1Fh			

Table 35. STARTUP1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-11	pll_lock_dly	R/W	12h	Wait time before lock detect goes high after the calibration. Expected value is ~1ms. The actual delay will be 256*T*(programmed value). Where T is the smclk period.
10-5	ac_init_dly	R/W	10h	Peak detector settlig time. i.e. pll_en_peakdet_vco going high to first cross code change. Expected value is 1.6us. The actual delay will be 4*T*(programmed value). Where T is the smclk period.
4-0	cp_dly	R/W	1Fh	Delay from vtune driver enable (pll_en_vtune_drv) going high to peak detector enable (pll_en_peakdet_vco) going high. Expected delay is 200us. The actual delay will be 64*T*(programmed value). Where T is the smclk period.

8.6.1.18 STARTUP2 Register (Address = 11h) [reset = 6C4h]

STARTUP2 is shown in [Figure 51](#) and described in [Table 36](#).

Return to [Summary Table](#).

Figure 51. STARTUP2 Register

15	14	13	12	11	10	9	8
RESERVED	switch_dly				err_cnt		
R/W-0h		R/W-0h				R/W-6h	
7	6	5	4	3	2	1	0
fc_setl_dly		ac_cmp_dly					
R/W-3h		R/W-4h					

Table 36. STARTUP2 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15	RESERVED	R/W	0h	Reserved.
14-11	switch_dly	R/W	0h	Indicates number of SM clocks to wait before SSM clock is turned off after all the active signals are low. Internally scaled up by 2 ⁶
10-8	err_cnt	R/W	6h	Indicates how long to wait for *b4* outputs before declaring lock detect. in PFD clocks 0h = 32 1h = 64 2h = 128 3h = 256
7-6	fc_setl_dly	R/W	3h	Delay between two cap codes in terms of REFCLK period. Expected value is 1 us. The actual delay will be 32*T*[programmed value]. Where T is the refclk period.
5-0	ac_cmp_dly	R/W	4h	Delay between successive cross code change. Expected value is 1us. The actual delay will be 4*T*[programmed value]. Where T is the smclk period.

8.6.1.19 REV0 Register (Address = 18h) [reset = 601h]

REV0 is shown in [Figure 52](#) and described in [Table 37](#).

Return to [Summary Table](#).

Figure 52. REV0 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-6h							
7	6	5	4	3	2	1	0
rev_reg							
R-1h							

Table 37. REV0 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-8	Reserved	R	06h	Reserved
7-0	rev_reg	R	1h	Revision ID register. 1h = CDCl6214

8.6.1.20 INPUT0 Register (Address = 1Ah) [reset = B14h]

INPUT0 is shown in [Figure 53](#) and described in [Table 38](#).

Return to [Summary Table](#).

Figure 53. INPUT0 Register

15	14	13	12	11	10	9	8
ref_inbuf_ctrl	RESERVED	RESERVED	ip_xo_cload				
R/W-0h	R/W-0h	R/W-0h	R/W-Bh				
7	6	5	4	3	2	1	0
ip_xo_gm_fine		ip_xo_gm				xin_inbuf_ctrl	
R/W-0h		R/W-5h				R/W-0h	

Table 38. INPUT0 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15	ref_inbuf_ctrl	R/W	0h	Reference input buffer select. 0h = LVCMOS 1h = AC-Differential
14	RESERVED	R/W	0h	RESERVED
13	RESERVED	R/W	0h	RESERVED

Table 38. INPUT0 Register Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
12-8	ip_xo_cload	R/W	Bh	Selects load cap for XO (up to 9 pF) in 5 bit binary selection). Step size is about 200 fF. 0h = 3.0 pF 1h = 3.2 pF 2h = 3.4 pF 3h = 3.6 pF 4h = 3.8 pF 5h = 4.0 pF 6h = 4.2 pF 7h = 4.4 pF 8h = 4.6 pF 9h = 4.8 pF Ah = 5.0 pF Bh = 5.2 pF Ch = 5.4 pF Dh = 5.6 pF Eh = 5.8 pF Fh = 6.0 pF 10h = 6.2 pF 11h = 6.4 pF 12h = 6.5 pF 13h = 6.7 pF 14h = 6.9 pF 15h = 7.1 pF 16h = 7.3 pF 17h = 7.5 pF 18h = 7.7 pF 19h = 7.9 pF 1Ah = 8.1 pF 1Bh = 8.3 pF 1Ch = 8.5 pF 1Dh = 8.7 pF 1Eh = 8.9 pF 1Fh = 9.0 pF
7-6	ip_xo_gm_fine	R/W	0h	Tune XO bias LSB current value from default to 1/3.

Table 38. INPUT0 Register Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
5-2	ip_xo_gm	R/W	5h	Tune bias current for XO. Gm programmability. Typical values: 0h = Disabled 1h = 14 μ A 2h = 29 μ A 3h = 44 μ A 4h = 59 μ A 5h = 148 μ A 6h = 295 μ A 7h = 443 μ A 8h = 591 μ A 9h = 884 μ A Ah = 1177 μ A Bh = 1468 μ A Ch = 1758 μ A
1-0	xin_inbuf_ctrl	R/W	0h	Input buffer select. 0h = XO 1h = CMOS 2h = DIFF

8.6.1.21 INPUT1 Register (Address = 1Bh) [reset = 0h]

INPUT1 is shown in [Figure 54](#) and described in [Table 39](#).

Return to [Summary Table](#).

Figure 54. INPUT1 Register

15	14	13	12	11	10	9	8
ip_en_pri_diff_buf	ip_byp_en_ch4	ip_byp_en_ch3	ip_byp_en_ch2	ip_byp_en_ch1	ip_byp_en_y0	ip_byp_mux	ip_rst_rdiv
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
ip_rdiv							
R/W-0h							

Table 39. INPUT1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15	ip_en_pri_diff_buf	R/W	0h	Refer State Machine Document. Refer State Machine Document
14	ip_byp_en_ch4	R/W	0h	Bypass path buffer enable for CH4. This is required to drive a bypass signal using ch4_iod_mux. 0h = disabled 1h = enabled
13	ip_byp_en_ch3	R/W	0h	Bypass path buffer enable for CH3. This is required to drive a bypass signal using ch3_iod_mux. 0h = disabled 1h = enabled
12	ip_byp_en_ch2	R/W	0h	Bypass path buffer enable for CH2. This is required to drive a bypass signal using ch2_iod_mux. 0h = disabled 1h = enabled
11	ip_byp_en_ch1	R/W	0h	Bypass path buffer enable for CH1. This is required to drive a bypass signal using ch1_iod_mux. 0h = disabled 1h = enabled
10	ip_byp_en_y0	R/W	0h	Enable input clock to come out on Y0 buffer.
9	ip_byp_mux	R/W	0h	Selects Y0 clock between "REF_CLK" and "PFD_CLK". 0h = REF 1h = PFD
8	ip_rst_rdiv	R/W	0h	Resets flops in ref divider. Active (high) during power on reset or SWRST or pin reset and inactive afterwards. Refer State Machine Document
7-0	ip_rdiv	R/W	0h	Reference clock divider. 0= Doubler ON, 1= /1, 2= /2. etc 0h = x2 1h = /1 2h = /2 3h = /3 4h = /4 5h = /5 ... FFh = /255

8.6.1.22 INPUT_DBG0 Register (Address = 1Ch) [reset = 0h]

INPUT_DBG0 is shown in and described in [Table 40](#).

Return to [Summary Table](#).

Figure 55. INPUT_DBG0 Register

15	14	13	12	11	10	9	8
RESERVED		RESERVED		RESERVED		RESERVED	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
RESERVED		ip_ldo_load_en	ip_en_test_dblrclk	ip_en_test_pfdclk	ip_en_test_refclk	ip_en_test_smclk	ip_en_test_XO
R/W-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 40. INPUT_DBG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	Reserved.
13-12	RESERVED	R/W	0h	RESERVED
11-9	RESERVED	R/W	0h	RESERVED
8-6	RESERVED	R/W	0h	RESERVED
5	ip_ldo_load_en	R/W	0h	Switches on Input path LDO output load (1K resistor).
4	ip_en_test_dblrclk	R/W	0h	Enable xo doubler clock to come out on test point.
3	ip_en_test_pfdclk	R/W	0h	Enable PFD clock to come out on test point.
2	ip_en_test_refclk	R/W	0h	Enable Ref clock (Before Doubler) to come out on test point.
1	ip_en_test_smclk	R/W	0h	Enable SM clock to come out on test point.
0	ip_en_test_XO	R/W	0h	Enables XO bias current to come out on XO. XI is pulled to ground internally.

8.6.1.23 PLL0 Register (Address = 1Dh) [reset = Ch]

PLL0 is shown in [Figure 56](#) and described in [Table 41](#).

Return to [Summary Table](#).

Figure 56. PLL0 Register

15	14	13	12	11	10	9	8
pll_psfb		pll_ndiv					
R/W-0h		R/W-Ch					
7	6	5	4	3	2	1	0
pll_ndiv							
R/W-Ch							

Table 41. PLL0 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-14	pll_psfb	R/W	0h	Programming bits for PLL feedback pre-scaler. 0h = /4 1h = /5 2h = /6
13-0	pll_ndiv	R/W	Ch	Feedback divider, must be at least 6h.

8.6.1.24 PLL1 Register (Address = 1Eh) [reset = 5140h]

PLL1 is shown in Figure 57 and described in Table 42.

Return to [Summary Table](#).

Figure 57. PLL1 Register

15	14	13	12	11	10	9	8
pll_cp_up						pll_cp_dn	
R/W-14h						R/W-14h	
7	6	5	4	3	2	1	0
pll_cp_dn				pll_psb		pll_psa	
R/W-14h				R/W-0h		R/W-0h	

Table 42. PLL1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-10	pll_cp_up	R/W	14h	Programming bits for up current of CP. 0h = 0.0 mA 1h = 0.1 mA 2h = 0.2 mA 3h = 0.3 mA [...] 1Fh = 3.1 mA 37h = 3.2 mA 38h = 3.3 mA [...] 3Dh = 3.8 mA 3Eh = 3.9 mA 3Fh = 4.0 mA
9-4	pll_cp_dn	R/W	14h	Programming bits for down current of CP. 0h = 0.0 mA 1h = 0.1 mA 2h = 0.2 mA 3h = 0.3 mA [...] 1Fh = 3.1 mA 37h = 3.2 mA 38h = 3.3 mA [...] 3Dh = 3.8 mA 3Eh = 3.9 mA 3Fh = 4.0 mA
3-2	pll_psb	R/W	0h	Programming bits for pre-scaler B. 0h = /4 1h = /5 2h = /6
1-0	pll_psa	R/W	0h	Programming bits for pre-scaler A. 0h = /4 1h = /5 2h = /6

8.6.1.25 PLL2 Register (Address = 1Fh) [reset = 1E72h]

PLL2 is shown in [Figure 58](#) and described in [Table 43](#).

Return to [Summary Table](#).

Figure 58. PLL2 Register

15	14	13	12	11	10	9	8
RESERVED			pll_lf_zcap				pll_lf_res
R/W-0h			R/W-Fh				R/W-3h
7	6	5	4	3	2	1	0
pll_lf_res			pll_lf_pcap				
R/W-3h			R/W-12h				

Table 43. PLL2 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-14	RESERVED	R/W	0h	Reserved.
13-9	pll_lf_zcap	R/W	Fh	Programming bits of cap value of zero of loop-filter. 0h = 000 pF 1h = 030 pF 2h = 060 pF 3h = 090 pF 4h = 120 pF 5h = 150 pF 6h = 180 pF 7h = 210 pF 8h = 240 pF 9h = 270 pF Ah = 300 pF Bh = 330 pF Ch = 360 pF Dh = 390 pF Eh = 420 pF Fh = 450 pF 10h = 480 pF 11h = 510 pF 12h = 540 pF 13h = 570 pF 14h = 600 pF

Table 43. PLL2 Register Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
8-5	pll_lf_res	R/W	3h	Programming bits of res value of zero of loop-filter. 0h = open k Ω 1h = 00.5 k Ω 2h = 01.5 k Ω 3h = 02.5 k Ω 4h = 03.5 k Ω 5h = 04.5 k Ω 6h = 05.5 k Ω 7h = 06.5 k Ω 8h = 07.5 k Ω 9h = 08.5 k Ω Ah = 09.5 k Ω Bh = 10.5 k Ω Ch = 11.5 k Ω
4-0	pll_lf_pcap	R/W	12h	Programming bits of cap value of pole of loop-filter. 0h = 00.0 pF 1h = 00.5 pF 2h = 01.5 pF 3h = 02.5 pF 4h = 03.5 pF 5h = 04.5 pF 6h = 05.5 pF 7h = 06.5 pF 8h = 07.5 pF 9h = 08.5 pF Ah = 09.5 pF Bh = 10.5 pF Ch = 11.5 pF Dh = 12.5 pF Eh = 13.5 pF Fh = 14.5 pF 10h = 15.5 pF 11h = 16.5 pF 12h = 17.5 pF 13h = 18.5 pF 14h = 19.5 pF

8.6.1.26 PLL4 Register (Address = 21h) [reset = 7h]

PLL4 is shown in [Figure 59](#) and described in [Table 44](#).

Return to [Summary Table](#).

Figure 59. PLL4 Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED			RESERVED			RESERVED
R/W-0h	R/W-0h			R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
RESERVED	pll_pfd_dly_ctrl		pll_lockdet_window			pll_lockdet_wait	
R/W-0h	R/W-0h		R/W-1h			R/W-3h	

Table 44. PLL4 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-7	RESERVED	R/W	0h	Reserved.
6-5	pll_pfd_dly_ctrl	R/W	0h	Programming of PFD reset delay. 0h = 2 1h = 6 2h = 10 3h = 14
4-2	pll_lockdet_window	R/W	1h	Programmability of PFD input and output time window for lock detect. 0h = disabled 1h = typ 1.4 ns 2h = typ 2.6 ns 3h = typ 3.9 ns 4h = typ 5.2 ns 5h = typ 6.4 ns 6h = typ 7.6 ns 7h = typ 8.9 ns
1-0	pll_lockdet_wait	R/W	3h	Programmability of analog lock detect timer. In PFD cycles 0h = 1 1h = 16 2h = 64 3h = 128

8.6.1.27 CH1_CTRL0 Register (Address = 23h) [reset = 8000h]

CH1_CTRL0 is shown in [Figure 60](#) and described in [Table 45](#).

Return to [Summary Table](#).

Figure 60. CH1_CTRL0 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ch1_fod_msb															
R/WEX-8000h															

Table 45. CH1_CTRL0 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	ch1_fod_msb	R/WEX	8000h	MSB Part of the FOD Fraction. Also, used in FOD_DELAY_MODE. Use FOD_Calculator for FOD Frequency

8.6.1.28 CH1_CTRL1 Register (Address = 24h) [reset = 0h]

CH1_CTRL1 is shown in [Figure 61](#) and described in [Table 46](#).

Return to [Summary Table](#).

Figure 61. CH1_CTRL1 Register

15	14	13	12	11	10	9	8
RESERVED							ch1_fod
R/W-0h							R/WEX-0h
7	6	5	4	3	2	1	0
ch1_fod							
R/WEX-0h							

Table 46. CH1_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	Reserved.
8-0	ch1_fod	R/WEX	0h	LSB Part of the FOD Fraction. Also, used in FOD_DELAY_MODE. Use FOD_Calculator for FOD Frequency

8.6.1.29 CH1_CTRL2 Register (Address = 25h) [reset = 8003h]

CH1_CTRL2 is shown in [Figure 62](#) and described in [Table 47](#).

Return to [Summary Table](#).

Figure 62. CH1_CTRL2 Register

15	14	13	12	11	10	9	8
ch1_iod_mux		ch1_iod_div					
R/W-2h		R/WEX-3h					
7	6	5	4	3	2	1	0
ch1_iod_div							
R/WEX-3h							

Table 47. CH1_CTRL2 Register Field Descriptions

BITS	FIELD	TYPE	RESET	DESCRIPTION
15-14	ch1_iod_mux	R/W	2h	Input Clock selection for IOD. 0h = PSA 1h = PSB 2h = FOD 3h = REF
13-0	ch1_iod_div	R/WEX	3h	IOD Division Value. 0h = Powers Down, Output=Input/IOD_DIV

8.6.1.30 CH1_CTRL3 Register (Address = 26h) [reset = 9h]

CH1_CTRL3 is shown in [Figure 63](#) and described in [Table 48](#).

Return to [Summary Table](#).

Figure 63. CH1_CTRL3 Register

15	14	13	12	11	10	9	8
ch1_sync_delay					ch1_sync_en	RESERVED	ch1_mute_sel
R/W-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
ch1_mute	ch1_cmos_pol		ch1_outbuf_ctrl			ch1_mux	
R/W-0h	R/W-0h		R/W-2h			R/W-1h	

Table 48. CH1_CTRL3 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-11	ch1_sync_delay	R/W	0h	Sync Delay cycles of IOD Input Clock. One cycle is a period of the selected pre-scaler clock.
10	ch1_sync_en	R/W	0h	Enables SYNC for the channel. 0h = Disabled 1h = Enabled
9	RESERVED	R/W	0h	Reserved.
8	ch1_mute_sel	R/W	0h	Mute selection for Output Channel. 0h = P=L N=H 1h = P=H N=L
7	ch1_mute	R/W	0h	To mute the output on this channel. When op_ovrd =1 - this bit will directly mute the output decoder else based on the 'mute' register bit value this signal will be driven high during the calibration. Refer State Machine Document
4-2	ch1_outbuf_ctrl	R/W	2h	Select the output buffer format. 0h = disabled 1h = LVDS ⁽¹⁾ 2h = HCSL 3h = CML 4h = LVPECL
1-0	ch1_mux	R/W	1h	Output Clock Selection. 1h = CH1 2h = CH2

(1) For DC-connection program `chx_lvds_cmtrim_inc = 2` and `ch[4:1]_1p8vdet` in [Table 69](#) and [Table 68](#) accordingly.

8.6.1.31 CH1_CTRL4 Register (Address = 27h) [reset = 679h]

CH1_CTRL4 is shown in [Figure 64](#) and described in [Table 49](#).

Return to [Summary Table](#).

Figure 64. CH1_CTRL4 Register

15	14	13	12	11	10	9	8
ch1_fod_dlymode	ch1_fod_passthrough	ch1_fod_rst	ch1_ssc_counter_src	ch1_ssc_counter			ch1_ssc_type
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-3h			R/W-0h
7	6	5	4	3	2	1	0
ch1_ssc_spread		ch1_ssc_fmod		ch1_ssc_en	RESERVED	RESERVED	ch1_glitchless_en
R/W-1h		R/W-3h		R/W-1h	R/W-0h	R/W-0h	R/W-1h

Table 49. CH1_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ch1_fod_dlymode	R/W	0h	Sets FOD in delay mode. 0h = Synthesis 1h = Delay
14	ch1_fod_passthrough	R/W	0h	Bypassed all Registers in the FOD. 0h = Normal 1h = Bypass
13	ch1_fod_rst	R/W	0h	Resets FOD. 0h = Active 1h = Reset
12	ch1_ssc_counter_src	R/W	0h	SSC counter clock source. 0h = FOD_CLK 1h = REF_CLK
11-9	ch1_ssc_counter	R/W	3h	Sets the division Value of SSC Clock.
8	ch1_ssc_type	R/W	0h	Sets SSC Type. 0h = center 1h = down
7-6	ch1_ssc_spread	R/W	1h	Sets the SSC Spread for SSC Modulation. All in percent of carrier frequency down / center spread. 0h = -0.5 or +/- 0.25 1h = -1.0 or +/- 0.5 2h = -2.0 or +/- 1.0 3h = -5.0 or +/- 2.5
5-4	ch1_ssc_fmod	R/W	3h	Sets number of cycles for SSC Modulation. 0h = 240 1h = 400 2h = 520 3h = 556
3	ch1_ssc_en	R/W	1h	Enables SSC. 0h = SSC Off 1h = SSC On
2	RESERVED	R/W	0h	RESERVED
1	RESERVED	R/W	0h	RESERVED

Table 49. CH1_CTRL4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ch1_glitchless_en	R/W	1h	Enables Glitchless switching for Output Channel. 0h = Immediate 1h = Glitch-less

8.6.1.32 CH1_CTRL5 Register (Address = 28h) [reset = 8h]

CH1_CTRL5 is shown in [Figure 65](#) and described in [Table 50](#).

Return to [Summary Table](#).

Figure 65. CH1_CTRL5 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				ch1_1p8vdet	RESERVED	RESERVED	RESERVED
R/W-0h				R/W-1h	R/W-0h	R/W-0h	R/W-0h

Table 50. CH1_CTRL5 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-4	RESERVED	R/W	0h	Reserved.
3	ch1_1p8vdet	R/W	1h	Specify supply on the channel. 0h = 2.5 V or 3.3 V 1h = 1.8 V
2	RESERVED	R/W	0h	RESERVED
1	RESERVED	R/W	0h	RESERVED
0	RESERVED	R/W	0h	RESERVED

8.6.1.33 CH2_CTRL0 Register (Address = 29h) [reset = 8000h]

CH2_CTRL0 is shown in [Figure 66](#) and described in [Table 51](#).

Return to [Summary Table](#).

Figure 66. CH2_CTRL0 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ch2_fod_msb															
R/WEX-8000h															

Table 51. CH2_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ch2_fod_msb	R/WEX	8000h	MSB Part of the FOD Fraction. Also, used in FOD_DELAY_MODE. Use FOD_Calculator for FOD Frequency

8.6.1.34 CH2_CTRL1 Register (Address = 2Ah) [reset = 0h]

CH2_CTRL1 is shown in [Figure 67](#) and described in [Table 52](#).

Return to [Summary Table](#).

Figure 67. CH2_CTRL1 Register

15	14	13	12	11	10	9	8
RESERVED							ch2_fod
R/W-0h							R/WEX-0h
7	6	5	4	3	2	1	0
ch2_fod							
R/WEX-0h							

Table 52. CH2_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	Reserved.
8-0	ch2_fod	R/WEX	0h	LSB Part of the FOD Fraction. Also, used in FOD_DELAY_MODE. Use FOD_Calculator for FOD Frequency

8.6.1.35 CH2_CTRL2 Register (Address = 2Bh) [reset = 0h]

CH2_CTRL2 is shown in [Figure 68](#) and described in [Table 53](#).

Return to [Summary Table](#).

Figure 68. CH2_CTRL2 Register

15	14	13	12	11	10	9	8
ch2_iod_mux			ch2_iod_div				
R/W-0h			R/WEX-0h				
7	6	5	4	3	2	1	0
ch2_iod_div							
R/WEX-0h							

Table 53. CH2_CTRL2 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-14	ch2_iod_mux	R/W	0h	Input Clock selection for IOD. 0h = PSA 1h = PSB 2h = FOD 3h = REF
13-0	ch2_iod_div	R/WEX	0h	IOD Division Value. 0h = Powers Down, Output=Input/IOD_DIV

8.6.1.36 CH2_CTRL3 Register (Address = 2Ch) [reset = 8h]

CH2_CTRL3 is shown in [Figure 69](#) and described in [Table 54](#).

Return to [Summary Table](#).

Figure 69. CH2_CTRL3 Register

15	14	13	12	11	10	9	8
ch2_sync_delay					ch2_sync_en	RESERVED	ch2_mute_sel
R/W-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
ch2_mute	ch2_cmos_pol		ch2_outbuf_ctrl			ch2_mux	
R/W-0h	R/W-0h		R/W-2h			R/W-0h	

Table 54. CH2_CTRL3 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-11	ch2_sync_delay	R/W	0h	Sync Delay cycles of IOD Input Clock. One cycle is a period of the selected pre-scaler clock.
10	ch2_sync_en	R/W	0h	Enables SYNC for the channel. 0h = Disabled 1h = Enabled
9	RESERVED	R/W	0h	Reserved.
8	ch2_mute_sel	R/W	0h	Mute selection for Output Channel. 0h = P=L N=H 1h = P=H N=L
7	ch2_mute	R/W	0h	To mute the output on this channel. When op_ovrd =1 - this bit will directly mute the output decoder else based on the 'mute' register bit value this signal will be driven high during the calibration. Refer State Machine Document
6-5	ch2_cmos_pol	R/W	0h	programmability of output CMOS buffer polarity. 0h = P+ N+ 1h = P+ N- 2h = P- N+ 3h = P- N-
4-2	ch2_outbuf_ctrl	R/W	2h	Select the output buffer format. 0h = disabled 1h = LVDS ⁽¹⁾ 2h = HCSL 3h = CML 4h = LVPECL 5h = CMOSPN 6h = CMOSP 7h = CMOSN
1-0	ch2_mux	R/W	0h	Output Clock Selection. 0h = CH1 1h = CH2 2h = CH3

(1) For DC-connection program *chx_lvds_cmtrim_inc* = 2 and *ch[4:1]_1p8vdet* in [Table 69](#) and [Table 68](#) accordingly.

8.6.1.37 CH2_CTRL4 Register (Address = 2Dh) [reset = 71h]

CH2_CTRL4 is shown in [Figure 70](#) and described in [Table 55](#).

Return to [Summary Table](#).

Figure 70. CH2_CTRL4 Register

15	14	13	12	11	10	9	8
ch2_fod_dlymode	ch2_fod_passthrough	ch2_fod_rst	ch2_ssc_counter_src	ch2_ssc_counter			ch2_ssc_type
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
ch2_ssc_spread		ch2_ssc_fmod		ch2_ssc_en	RESERVED	RESERVED	ch2_glitchless_en
R/W-1h		R/W-3h		R/W-0h	R/W-0h	R/W-0h	R/W-1h

Table 55. CH2_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ch2_fod_dlymode	R/W	0h	Sets FOD in delay mode. 0h = Synthesis 1h = Delay
14	ch2_fod_passthrough	R/W	0h	Bypassed all Registers in the FOD. 0h = Normal 1h = Bypass
13	ch2_fod_rst	R/W	0h	Resets FOD. 0h = Active 1h = Reset
12	ch2_ssc_counter_src	R/W	0h	SSC counter clock source. 0h = FOD_CLK 1h = REF_CLK
11-9	ch2_ssc_counter	R/W	0h	Sets the division Value of SSC Clock.
8	ch2_ssc_type	R/W	0h	Sets SSC Type. 0h = center 1h = down
7-6	ch2_ssc_spread	R/W	1h	Sets the SSC Spread for SSC Modulation.All in percent of carrier frequency. 0h = -0.5 down or +/- 0.25 1h = -1.0 or +/- 0.5 2h = -2.0 or +/- 1.0 3h = -5.0 or +/- 2.5
5-4	ch2_ssc_fmod	R/W	3h	Sets number of cycles for SSC Modulation. 0h = 240 1h = 400 2h = 520 3h = 556
3	ch2_ssc_en	R/W	0h	Enables SSC. 0h = SSC Off 1h = SSC On
2	RESERVED	R/W	0h	RESERVED
1	RESERVED	R/W	0h	RESERVED

Table 55. CH2_CTRL4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ch2_glitchless_en	R/W	1h	Enables Glitchless switching for Output Channel. 0h = Immediate 1h = Glitch-less

8.6.1.38 CH2_CTRL5 Register (Address = 2Eh) [reset = 8h]

CH2_CTRL5 is shown in [Figure 71](#) and described in [Table 56](#).

Return to [Summary Table](#).

Figure 71. CH2_CTRL5 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				ch2_1p8vdet	RESERVED	RESERVED	RESERVED
R/W-0h				R/W-1h	R/W-0h	R/W-0h	R/W-0h

Table 56. CH2_CTRL5 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-4	RESERVED	R/W	0h	Reserved.
3	ch2_1p8vdet	R/W	1h	Specify supply on the channel. 0h = 2.5 V or 3.3 V 1h = 1.8 V
2	RESERVED	R/W	0h	RESERVED
1	RESERVED	R/W	0h	RESERVED
0	RESERVED	R/W	0h	RESERVED

8.6.1.39 CH3_CTRL0 Register (Address = 2Fh) [reset = 8000h]

CH3_CTRL0 is shown in [Figure 72](#) and described in [Table 57](#).

Return to [Summary Table](#).

Figure 72. CH3_CTRL0 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ch3_fod_msb															
R/WEX-8000h															

Table 57. CH3_CTRL0 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	ch3_fod_msb	R/WEX	8000h	MSB Part of the FOD Fraction. Also, used in FOD_DELAY_MODE. Use FOD_Calculator for FOD Frequency

8.6.1.40 CH3_CTRL1 Register (Address = 30h) [reset = 0h]

CH3_CTRL1 is shown in [Figure 73](#) and described in [Table 58](#).

Return to [Summary Table](#).

Figure 73. CH3_CTRL1 Register

15	14	13	12	11	10	9	8
RESERVED							ch3_fod
R/W-0h							R/WEX-0h
7	6	5	4	3	2	1	0
ch3_fod							
R/WEX-0h							

Table 58. CH3_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	Reserved.
8-0	ch3_fod	R/WEX	0h	LSB Part of the FOD Fraction. Also, used in FOD_DELAY_MODE. Use FOD_Calculator for FOD Frequency

8.6.1.41 CH3_CTRL2 Register (Address = 31h) [reset = 0h]

CH3_CTRL2 is shown in [Figure 74](#) and described in [Table 59](#).

Return to [Summary Table](#).

Figure 74. CH3_CTRL2 Register

15	14	13	12	11	10	9	8
ch3_iod_mux		ch3_iod_div					
R/W-0h		R/WEX-0h					
7	6	5	4	3	2	1	0
ch3_iod_div							
R/WEX-0h							

Table 59. CH3_CTRL2 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-14	ch3_iod_mux	R/W	0h	Input Clock selection for IOD. 0h = PSA 1h = PSB 2h = FOD 3h = REF
13-0	ch3_iod_div	R/WEX	0h	IOD Division Value. 0h = Powers Down, Output=Input/IOD_DIV

8.6.1.42 CH3_CTRL3 Register (Address = 32h) [reset = 4h]

CH3_CTRL3 is shown in [Figure 75](#) and described in [Table 60](#).

Return to [Summary Table](#).

Figure 75. CH3_CTRL3 Register

15	14	13	12	11	10	9	8
ch3_sync_delay					ch3_sync_en	RESERVED	ch3_mute_sel
R/W-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
ch3_mute	ch3_cmos_pol		ch3_outbuf_ctrl			ch3_mux	
R/W-0h	R/W-0h		R/W-1h			R/W-0h	

Table 60. CH3_CTRL3 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-11	ch3_sync_delay	R/W	0h	Sync Delay cycles of IOD Input Clock. One cycle is a period of the selected pre-scaler clock.
10	ch3_sync_en	R/W	0h	Enables SYNC for the channel. 0h = Disabled 1h = Enabled
9	RESERVED	R/W	0h	Reserved.
8	ch3_mute_sel	R/W	0h	Mute selection for Output Channel. 0h = P=L N=H 1h = P=H N=L
7	ch3_mute	R/W	0h	To mute the output on this channel. When op_ovrd =1 - this bit will directly mute the output decoder else based on the 'mute' register bit value this signal will be driven high during the calibration. Refer State Machine Document
6-5	ch3_cmos_pol	R/W	0h	programmability of output CMOS buffer polarity. 0h = P+ N+ 1h = P+ N- 2h = P- N+ 3h = P- N-
4-2	ch3_outbuf_ctrl	R/W	1h	Select the output buffer format. 0h = disabled 1h = LVDS ⁽¹⁾ 2h = HCSL 3h = CML 4h = LVPECL 5h = CMOSPN 6h = CMOSP 7h = CMOSN
1-0	ch3_mux	R/W	0h	Output Clock Selection. 0h = CH2 1h = CH3 2h = CH4

(1) For DC-connection program *chx_lvds_cmtrim_inc* = 2 and *ch[4:1]_1p8vdet* in [Table 69](#) and [Table 68](#) accordingly.

8.6.1.43 CH3_CTRL4 Register (Address = 33h) [reset = 671h]

CH3_CTRL4 is shown in [Figure 76](#) and described in [Table 61](#).

Return to [Summary Table](#).

Figure 76. CH3_CTRL4 Register

15	14	13	12	11	10	9	8
ch3_fod_dlymode	ch3_fod_passthrough	ch3_fod_rst	ch3_ssc_counter_src	ch3_ssc_counter			ch3_ssc_type
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-3h			R/W-0h
7	6	5	4	3	2	1	0
ch3_ssc_spread		ch3_ssc_fmod		ch3_ssc_en	RESERVED	RESERVED	ch3_glitchless_en
R/W-1h		R/W-3h		R/W-0h	R/W-0h	R/W-0h	R/W-1h

Table 61. CH3_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ch3_fod_dlymode	R/W	0h	Sets FOD in delay mode. 0h = Synthesis 1h = Delay
14	ch3_fod_passthrough	R/W	0h	Bypassed all Registers in the FOD. 0h = Normal 1h = Bypass
13	ch3_fod_rst	R/W	0h	Resets FOD. 0h = Active 1h = Reset
12	ch3_ssc_counter_src	R/W	0h	SSC counter clock source. 0h = FOD_CLK 1h = REF_CLK
11-9	ch3_ssc_counter	R/W	3h	Sets the division Value of SSC Clock.
8	ch3_ssc_type	R/W	0h	Sets SSC Type. 0h = center 1h = down
7-6	ch3_ssc_spread	R/W	1h	Sets the SSC Spread for SSC Modulation.All in percent of carrier frequency. 0h = -0.5 down or +/- 0.25 1h = -1.0 or +/- 0.5 2h = -2.0 or +/- 1.0 3h = -5.0 or +/- 2.5
5-4	ch3_ssc_fmod	R/W	3h	Sets number of cycles for SSC Modulation. 0h = 240 1h = 400 2h = 520 3h = 556
3	ch3_ssc_en	R/W	0h	Enables SSC. 0h = SSC Off 1h = SSC On
2	RESERVED	R/W	0h	RESERVED
1	RESERVED	R/W	0h	RESERVED

Table 61. CH3_CTRL4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ch3_glitchless_en	R/W	1h	Enables Glitchless switching for Output Channel. 0h = Immediate 1h = Glitch-less

8.6.1.44 CH3_CTRL5 Register (Address = 34h) [reset = 8h]

CH3_CTRL5 is shown in [Figure 77](#) and described in [Table 62](#).

Return to [Summary Table](#).

Figure 77. CH3_CTRL5 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				ch3_1p8vdet	RESERVED	RESERVED	RESERVED
R/W-0h				R/W-1h	R/W-0h	R/W-0h	R/W-0h

Table 62. CH3_CTRL5 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-4	RESERVED	R/W	0h	Reserved.
3	ch3_1p8vdet	R/W	1h	Specify supply on the channel. 0h = 2.5 V or 3.3 V 1h = 1.8 V
2	RESERVED	R/W	0h	RESERVED
1	RESERVED	R/W	0h	RESERVED
0	RESERVED	R/W	0h	RESERVED

8.6.1.45 CH4_CTRL0 Register (Address = 35h) [reset = 8000h]

CH4_CTRL0 is shown in [Figure 78](#) and described in [Table 63](#).

Return to [Summary Table](#).

Figure 78. CH4_CTRL0 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ch4_fod_msb															
R/WEX-8000h															

Table 63. CH4_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ch4_fod_msb	R/WEX	8000h	MSB Part of the FOD Fraction. Also, used in FOD_DELAY_MODE. Use FOD_Calculator for FOD Frequency

8.6.1.46 CH4_CTRL1 Register (Address = 36h) [reset = 0h]

CH4_CTRL1 is shown in and described in .

Return to [Summary Table](#).

Figure 79. CH4_CTRL1 Register

15	14	13	12	11	10	9	8
RESERVED							ch4_fod
R/W-0h							R/WEX-0h
7	6	5	4	3	2	1	0
ch4_fod							
R/WEX-0h							

Table 64. CH4_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R/W	0h	Reserved.
8-0	ch4_fod	R/WEX	0h	LSB Part of the FOD Fraction. Also, used in FOD_DELAY_MODE. Use FOD_Calculator for FOD Frequency

8.6.1.47 CH4_CTRL2 Register (Address = 37h) [reset = 0h]

CH4_CTRL2 is shown in [Figure 80](#) and described in [Table 65](#).

Return to [Summary Table](#).

Figure 80. CH4_CTRL2 Register

15	14	13	12	11	10	9	8
ch4_iod_mux		ch4_iod_div					
R/W-0h		R/WEX-0h					
7	6	5	4	3	2	1	0
ch4_iod_div							
R/WEX-0h							

Table 65. CH4_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	ch4_iod_mux	R/W	0h	Input Clock selection for IOD. 0h = PSA 1h = PSB 2h = FOD 3h = REF
13-0	ch4_iod_div	R/WEX	0h	IOD Division Value. 0h = Powers Down, Output=Input/IOD_DIV

8.6.1.48 CH4_CTRL3 Register (Address = 38h) [reset = 4h]

CH4_CTRL3 is shown in [Figure 81](#) and described in [Table 66](#).

Return to [Summary Table](#).

Figure 81. CH4_CTRL3 Register

15	14	13	12	11	10	9	8
ch4_sync_delay					ch4_sync_en	RESERVED	ch4_mute_sel
R/W-0h					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
ch4_mute	ch4_cmos_pol		ch4_outbuf_ctrl			ch4_mux	
R/W-0h	R/W-0h		R/W-1h			R/W-0h	

Table 66. CH4_CTRL3 Register Field Descriptions

BITS	FIELD	TYPE	RESET	DESCRIPTION
15-11	ch4_sync_delay	R/W	0h	Sync Delay cycles of IOD Input Clock. One cycle is a period of the selected pre-scaler clock.
10	ch4_sync_en	R/W	0h	Enables SYNC for the channel. 0h = Disabled 1h = Enabled
9	RESERVED	R/W	0h	Reserved.
8	ch4_mute_sel	R/W	0h	Mute selection for Output Channel. 0h = P=L N=H 1h = P=H N=L
7	ch4_mute	R/W	0h	To mute the output on this channel. When op_ovrd =1 - this bit will directly mute the output decoder else based on the 'mute' register bit value this signal will be driven high during the calibration. Refer State Machine Document
4-2	ch4_outbuf_ctrl	R/W	1h	Select the output buffer format. 0h = disabled 1h = LVDS ⁽¹⁾ 2h = HCSL 3h = CML 4h = LVPECL
1-0	ch4_mux	R/W	0h	Output Clock Selection. 0h = Previous Channel, 1h = Current Channel, 2h = Next Channel, 3h = AGND 0h = CH3 1h = CH4

(1) For DC-connection program `chx_lvds_cmtrim_inc` = 2 and `ch[4:1]_1p8vdet` in [Table 69](#) and [Table 68](#) accordingly.

8.6.1.49 CH4_CTRL4 Register (Address = 39h) [reset = 71h]

CH4_CTRL4 is shown in [Figure 82](#) and described in [Table 67](#).

Return to [Summary Table](#).

Figure 82. CH4_CTRL4 Register

15	14	13	12	11	10	9	8
ch4_fod_dlymode	ch4_fod_passthrough	ch4_fod_rst	ch4_ssc_counter_src	ch4_ssc_counter			ch4_ssc_type
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h
7	6	5	4	3	2	1	0
ch4_ssc_spread		ch4_ssc_fmod		ch4_ssc_en	RESERVED	RESERVED	ch4_glitchless_en
R/W-1h		R/W-3h		R/W-0h	R/W-0h	R/W-0h	R/W-1h

Table 67. CH4_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ch4_fod_dlymode	R/W	0h	Sets FOD in delay mode. 0h = Synthesis 1h = Delay
14	ch4_fod_passthrough	R/W	0h	Bypassed all Registers in the FOD. 0h = Normal 1h = Bypass
13	ch4_fod_rst	R/W	0h	Resets FOD. 0h = Active 1h = Reset
12	ch4_ssc_counter_src	R/W	0h	SSC counter clock source. 0h = FOD_CLK 1h = REF_CLK
11-9	ch4_ssc_counter	R/W	0h	Sets the division Value of SSC Clock.
8	ch4_ssc_type	R/W	0h	Sets SSC Type. 0h = center 1h = down
7-6	ch4_ssc_spread	R/W	1h	Sets the SSC Spread for SSC Modulation.All in percent of carrier frequency. 0h = -0.5 down or +/- 0.25 1h = -1.0 or +/- 0.5 2h = -2.0 or +/- 1.0 3h = -5.0 or +/- 2.5
5-4	ch4_ssc_fmod	R/W	3h	Sets number of cycles for SSC Modulation. 0h = 240 1h = 400 2h = 520 3h = 556
3	ch4_ssc_en	R/W	0h	Enables SSC. 0h = SSC Off 1h = SSC On
2	RESERVED	R/W	0h	RESERVED
1	RESERVED	R/W	0h	RESERVED

Table 67. CH4_CTRL4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ch4_glitchless_en	R/W	1h	Enables Glitchless switching for Output Channel. 0h = Immediate 1h = Glitch-less

8.6.1.50 CH4_CTRL5 Register (Address = 3Ah) [reset = 8h]

CH4_CTRL5 is shown in [Figure 83](#) and described in [Table 68](#).

Return to [Summary Table](#).

Figure 83. CH4_CTRL5 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0h							
7	6	5	4	3	2	1	0
RESERVED				ch4_1p8vdet	RESERVED	RESERVED	RESERVED
R/W-0h				R/W-1h	R/W-0h	R/W-0h	R/W-0h

Table 68. CH4_CTRL5 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-4	RESERVED	R/W	0h	Reserved.
3	ch4_1p8vdet	R/W	1h	Specify supply on the channel. 0h = 2.5 V or 3.3 V 1h = 1.8 V
2	RESERVED	R/W	0h	RESERVED
1	RESERVED	R/W	0h	RESERVED
0	RESERVED	R/W	0h	RESERVED

8.6.1.51 CHX_CTRL0 Register (Address = 3Bh) [reset = 61h]

CHX_CTRL0 is shown in [Figure 84](#) and described in [Table 69](#).

Return to [Summary Table](#).

Figure 84. CHX_CTRL0 Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	chx_rst	chx_lvds_cmtrim_inc		chx_lvds_cmtrim_dec		chx_diffbuf_ibias_trim
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h		R/W-3h
7	6	5	4	3	2	1	0
	chx_diffbuf_ibias_trim		chx_lvcmos_drv	RESERVED	ch0_lvcmos_drv		RESERVED
	R/W-3h		R/W-1h	R/W-0h	R/W-0h		R/W-1h

Table 69. CHX_CTRL0 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15	RESERVED	R/W	0h	RESERVED
14	RESERVED	R/W	0h	RESERVED
13	chx_rst	R/W	0h	All Channel RST during Power Up and Later. 1h = RST, 0h = Normal.
12-11	chx_lvds_cmtrim_inc	R/W	0h	Diff output buffer output common mode programmability. Decrement Only use either increment or decrement.
10-9	chx_lvds_cmtrim_dec	R/W	0h	Diff output buffer output common mode programmability. Increment Only use either increment or decrement.
8-5	chx_diffbuf_ibias_trim	R/W	3h	Differential output buffer tail current programmability. Ch = 350uA 8h = 400uA 4h = 450uA 0h = 500uA 0h = 500uA 1h = 550uA 2h = 600uA 3h = 650uA
4	chx_lvcmos_drv	R/W	1h	Adjust CH1 to CH4 LVCMOS driver strength. 0h = Normal 1h = Fast
3	RESERVED	R/W	1h	RESERVED
2-1	ch0_lvcmos_drv	R/W	0h	Enable Y0 channel and adjust LVCMOS driver strength. 0h = Off 1h = Normal 3h = Fast
0	RESERVED	R/W	1h	RESERVED

8.6.1.52 CHX_CTRL1 Register (Address = 3Ch) [reset = 18h]

CHX_CTRL1 is shown in [Figure 85](#) and described in [Table 70](#).

Return to [Summary Table](#).

Figure 85. CHX_CTRL1 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-18h															

Table 70. CHX_CTRL1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	RESERVED	R/W	18h	RESERVED

8.6.1.53 CHX_CTRL2 Register (Address = 3Dh) [reset = 1500h]

CHX_CTRL2 is shown in [Figure 86](#) and described in [Table 71](#).

Return to [Summary Table](#).

Figure 86. CHX_CTRL2 Register

15	14	13	12	11	10	9	8
RESERVED		RESERVED	RESERVED				
R/W-0h		R/W-0h	R/W-15h				
7	6	5	4	3	2	1	0
fod_clk_ch4	fod_clk_ch3	fod_clk_ch2	fod_clk_ch1	RESERVED			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

Table 71. CHX_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0h	RESERVED
13	RESERVED	R/W	0h	RESERVED
12-8	RESERVED	R/W	15h	RESERVED
7	fod_clk_ch4	R/W	0h	FOD4 clock select. 0h = IOD4 1h = direct
6	fod_clk_ch3	R/W	0h	FOD3 clock select. 0h = IOD3 1h = direct
5	fod_clk_ch2	R/W	0h	FOD2 clock select. 0h = IOD2 1h = direct
4	fod_clk_ch1	R/W	0h	FOD1 clock select. 0h = IOD1 1h = direct
3-0	RESERVED	R/W	0h	RESERVED

8.6.1.54 CHX_CTRL3 Register (Address = 3Eh) [reset = 4210h]

CHX_CTRL3 is shown in and described in [Table 72](#).

Return to [Summary Table](#).

Figure 87. CHX_CTRL3 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-4210h															

Table 72. CHX_CTRL3 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	RESERVED	R/W	4210h	RESERVED

8.6.1.55 CHX_CTRL4 Register (Address = 3Fh) [reset = 210h]

CHX_CTRL4 is shown in [Figure 88](#) and described in [Table 73](#).

Return to [Summary Table](#).

Figure 88. CHX_CTRL4 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-210h															

Table 73. CHX_CTRL4 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	RESERVED	R/W	210h	RESERVED

8.6.1.56 DBG0 Register (Address = 42h) [reset = 200h]

DBG0 is shown in and described in [Table 74](#).

Return to [Summary Table](#).

Figure 89. DBG0 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-200h															

Table 74. DBG0 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	RESERVED	R/W	200h	RESERVED

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8.6.2 EEPROM Map

The EEPROM is split into a common base page which holds common settings. Then there are two pages for customized settings. Page 0 is selected using EEPROMSEL = Low. Page 1 is selected using EEPROMSEL = High.

The CRC value is stored at the end of page 1 in word 0x3F.

Table 75. EEPROM, Base

WORD NO.	SECTION	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0h	Base	cp_dly[0]	cal_mute	shift_left[1]	shift_left[0]	gpio3_gf_en	gpio2_gf_en	acal_en	pdn_pll_vcobuf2	pdn_pll_vcobuf	pdn_pll_vcobuf	pdn_pll_cp	pdn_pll_lockdet	pdn_pll_pfd	pdn_pll_psfb	regcommitt_page	resetn_soft
1h	Base	ac_cmp_dly[0]	pll_lock_dly[4]	pll_lock_dly[3]	pll_lock_dly[2]	pll_lock_dly[1]	pll_lock_dly[0]	ac_init_dly[5]	ac_init_dly[4]	ac_init_dly[3]	ac_init_dly[2]	ac_init_dly[1]	ac_init_dly[0]	cp_dly[4]	cp_dly[3]	cp_dly[2]	cp_dly[1]
2h	Base	0	0	0	0	0	0	err_cnt[2]	err_cnt[1]	err_cnt[0]	fc_sett_dly[1]	fc_sett_dly[0]	ac_cmp_dly[5]	ac_cmp_dly[4]	ac_cmp_dly[3]	ac_cmp_dly[2]	ac_cmp_dly[1]
3h	Base	pll_pfd_dly_ctrl[1]	pll_pfd_dly_ctrl[0]	pll_lockdet_window[2]	pll_lockdet_window[1]	pll_lockdet_window[0]	pll_lockdet_wait[1]	pll_lockdet_wait[0]	0	0	0	0	0	0	0	0	0
4h	Base	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
5h	Base	chx_diffbuf_ibias_trim[1]	chx_diffbuf_ibias_trim[0]	chx_lvcmos_drv	chx_en_cmos_slow	0	0	ch3_ssc_counter[3]	ch3_ssc_counter[2]	ch3_ssc_counter[1]	ch3_ssc_counter[0]	0	0	ch1_ssc_counter[3]	ch1_ssc_counter[2]	ch1_ssc_counter[1]	ch1_ssc_counter[0]
6h	Base	0	0	0	0	1	1	0	0	0	0	chx_lvds_cmtrim_in_c[1]	chx_lvds_cmtrim_in_c[0]	chx_lvds_cmtrim_dec[1]	chx_lvds_cmtrim_dec[0]	chx_diffbuf_ibias_trim[3]	chx_diffbuf_ibias_trim[2]
7h	Base	0	1	0	1	fod_clk_ch4	fod_clk_ch3	fod_clk_ch2	fod_clk_ch1	0	0	0	0	0	0	0	0
8h	Base	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	1
9h	Base	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1
Ah	Base	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
Bh	Base	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 76. EEPROM, Page 0

WORD NO.	SECTION	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Ch	Page 0	gpio4_input_sel[3]	gpio4_input_sel[2]	gpio4_input_sel[1]	gpio4_input_sel[0]	gpio1_input_sel[3]	gpio1_input_sel[2]	gpio1_input_sel[1]	gpio1_input_sel[0]	i2c_a0	gpio0_input_sel	gpio4_dir_sel	gpio1_dir_sel	gpio0_dir_sel	zdm_clocksel	zdm_mode	mode
Dh	Page 0	gpio4_output_sel[3]	gpio4_output_sel[2]	gpio4_output_sel[1]	gpio4_output_sel[0]	gpio1_output_sel[3]	gpio1_output_sel[2]	gpio1_output_sel[1]	gpio1_output_sel[0]	fod_size[5]	fod_size[4]	fod_size[3]	fod_size[2]	fod_size[1]	fod_size[0]	ref_mux_src	ref_mux
Eh	Page 0	pdn_pll_sscclk	pdn_ch4	pdn_ch4_ssc	pdn_ch3	pdn_ch3_ssc	pdn_ch2	pdn_ch2_ssc	pdn_ch1	pdn_ch1_ssc	iod_size	rsrvd_1[1]	rsrvd_1[0]	gpio0_output_sel[3]	gpio0_output_sel[2]	gpio0_output_sel[1]	gpio0_output_sel[0]
Fh	Page 0	ip_xo_clock_ad[2]	ip_xo_clock_ad[1]	ip_xo_clock_ad[0]	ip_xo_gm_fine[1]	ip_xo_gm_fine[0]	ip_xo_gm[3]	ip_xo_gm[2]	ip_xo_gm[1]	ip_xo_gm[0]	xin_inbuf_ctrl[1]	xin_inbuf_ctrl[0]	zdm_auto	bypass_cal	bypass_config	pdn_pll_psb	pdn_pll_psa
10h	Page 0	ip_bypass_n_ch3	ip_bypass_n_ch2	ip_bypass_n_ch1	ip_bypass_n_0	ip_bypass_mux	ip_rdiv[7]	ip_rdiv[6]	ip_rdiv[5]	ip_rdiv[4]	ip_rdiv[3]	ip_rdiv[2]	ip_rdiv[1]	ip_rdiv[0]	ref_inbuf_ctrl	ip_xo_clock_ad[4]	ip_xo_clock_ad[3]
11h	Page 0	pll_ndiv[13]	pll_ndiv[12]	pll_ndiv[11]	pll_ndiv[10]	pll_ndiv[9]	pll_ndiv[8]	pll_ndiv[7]	pll_ndiv[6]	pll_ndiv[5]	pll_ndiv[4]	pll_ndiv[3]	pll_ndiv[2]	pll_ndiv[1]	pll_ndiv[0]	ip_ldo_load_en	ip_bypass_n_ch4
12h	Page 0	pll_cp_up[3]	pll_cp_up[2]	pll_cp_up[1]	pll_cp_up[0]	pll_cp_dn[5]	pll_cp_dn[4]	pll_cp_dn[3]	pll_cp_dn[2]	pll_cp_dn[1]	pll_cp_dn[0]	pll_psb[1]	pll_psb[0]	pll_psa[1]	pll_psa[0]	pll_psfb[1]	pll_psfb[0]
13h	Page 0	pll_lf_zcap[4]	pll_lf_zcap[3]	pll_lf_zcap[2]	pll_lf_zcap[1]	pll_lf_zcap[0]	pll_lf_res[3]	pll_lf_res[2]	pll_lf_res[1]	pll_lf_res[0]	pll_lf_pcap[4]	pll_lf_pcap[3]	pll_lf_pcap[2]	pll_lf_pcap[1]	pll_lf_pcap[0]	pll_cp_up[5]	pll_cp_up[4]
14h	Page 0	ch1_fod_msb[15]	ch1_fod_msb[14]	ch1_fod_msb[13]	ch1_fod_msb[12]	ch1_fod_msb[11]	ch1_fod_msb[10]	ch1_fod_msb[9]	ch1_fod_msb[8]	ch1_fod_msb[7]	ch1_fod_msb[6]	ch1_fod_msb[5]	ch1_fod_msb[4]	ch1_fod_msb[3]	ch1_fod_msb[2]	ch1_fod_msb[1]	ch1_fod_msb[0]
15h	Page 0	ch1_iod_div[6]	ch1_iod_div[5]	ch1_iod_div[4]	ch1_iod_div[3]	ch1_iod_div[2]	ch1_iod_div[1]	ch1_iod_div[0]	ch1_iod_div[8]	ch1_iod_div[7]	ch1_iod_div[6]	ch1_iod_div[5]	ch1_iod_div[4]	ch1_iod_div[3]	ch1_iod_div[2]	ch1_iod_div[1]	ch1_iod_div[0]
16h	Page 0	0	0	ch1_outbuf_ctrl[2]	ch1_outbuf_ctrl[1]	ch1_outbuf_ctrl[0]	ch1_mux[1]	ch1_mux[0]	ch1_iod_mux[1]	ch1_iod_mux[0]	ch1_iod_div[13]	ch1_iod_div[12]	ch1_iod_div[11]	ch1_iod_div[10]	ch1_iod_div[9]	ch1_iod_div[8]	ch1_iod_div[7]
17h	Page 0	ch1_ssc_type	ch1_ssc_spread[1]	ch1_ssc_spread[0]	ch1_ssc_fmod[1]	ch1_ssc_fmod[0]	ch1_ssc_en	0	ch1_glitch_less_en	ch1_sync_delay[4]	ch1_sync_delay[3]	ch1_sync_delay[2]	ch1_sync_delay[1]	ch1_sync_delay[0]	ch1_sync_en	ch1_mute_sel	ch1_mute
18h	Page 0	ch2_fod_msb[13]	ch2_fod_msb[12]	ch2_fod_msb[11]	ch2_fod_msb[10]	ch2_fod_msb[9]	ch2_fod_msb[8]	ch2_fod_msb[7]	ch2_fod_msb[6]	ch2_fod_msb[5]	ch2_fod_msb[4]	ch2_fod_msb[3]	ch2_fod_msb[2]	ch2_fod_msb[1]	ch2_fod_msb[0]	ch1_1p8v_det	ch1_fod_dlymode
19h	Page 0	ch2_iod_div[4]	ch2_iod_div[3]	ch2_iod_div[2]	ch2_iod_div[1]	ch2_iod_div[0]	ch2_fod[8]	ch2_fod[7]	ch2_fod[6]	ch2_fod[5]	ch2_fod[4]	ch2_fod[3]	ch2_fod[2]	ch2_fod[1]	ch2_fod[0]	ch2_fod_msb[15]	ch2_fod_msb[14]
1Ah	Page 0	ch2_outbuf_ctrl[2]	ch2_outbuf_ctrl[1]	ch2_outbuf_ctrl[0]	ch2_mux[1]	ch2_mux[0]	ch2_iod_mux[1]	ch2_iod_mux[0]	ch2_iod_div[13]	ch2_iod_div[12]	ch2_iod_div[11]	ch2_iod_div[10]	ch2_iod_div[9]	ch2_iod_div[8]	ch2_iod_div[7]	ch2_iod_div[6]	ch2_iod_div[5]
1Bh	Page 0	ch2_ssc_spread[0]	ch2_ssc_fmod[1]	ch2_ssc_fmod[0]	ch2_ssc_en	0	ch2_glitch_less_en	ch2_sync_delay[4]	ch2_sync_delay[3]	ch2_sync_delay[2]	ch2_sync_delay[1]	ch2_sync_delay[0]	ch2_mute_sel	ch2_mute	ch2_cmos_pol[1]	ch2_cmos_pol[0]	ch2_ssc_spread[1]
1Ch	Page 0	ch3_fod_msb[11]	ch3_fod_msb[10]	ch3_fod_msb[9]	ch3_fod_msb[8]	ch3_fod_msb[7]	ch3_fod_msb[6]	ch3_fod_msb[5]	ch3_fod_msb[4]	ch3_fod_msb[3]	ch3_fod_msb[2]	ch3_fod_msb[1]	ch3_fod_msb[0]	ch2_1p8v_det	ch2_fod_dlymode	ch2_ssc_type	ch2_ssc_spread[1]
1Dh	Page 0	ch3_iod_div[2]	ch3_iod_div[1]	ch3_iod_div[0]	ch3_fod[8]	ch3_fod[7]	ch3_fod[6]	ch3_fod[5]	ch3_fod[4]	ch3_fod[3]	ch3_fod[2]	ch3_fod[1]	ch3_fod[0]	ch3_fod_msb[15]	ch3_fod_msb[14]	ch3_fod_msb[13]	ch3_fod_msb[12]
1Eh	Page 0	ch3_outbuf_ctrl[0]	ch3_mux[1]	ch3_mux[0]	ch3_iod_mux[1]	ch3_iod_mux[0]	ch3_iod_div[13]	ch3_iod_div[12]	ch3_iod_div[11]	ch3_iod_div[10]	ch3_iod_div[9]	ch3_iod_div[8]	ch3_iod_div[7]	ch3_iod_div[6]	ch3_iod_div[5]	ch3_iod_div[4]	ch3_iod_div[3]
1Fh	Page 0	ch3_ssc_fmod[0]	ch3_ssc_en	0	ch3_glitch_less_en	ch3_sync_delay[4]	ch3_sync_delay[3]	ch3_sync_delay[2]	ch3_sync_delay[1]	ch3_sync_delay[0]	ch3_sync_en	ch3_mute_sel	ch3_mute	ch3_cmos_pol[1]	ch3_cmos_pol[0]	ch3_outbuf_ctrl[2]	ch3_outbuf_ctrl[1]
20h	Page 0	ch4_fod_msb[9]	ch4_fod_msb[8]	ch4_fod_msb[7]	ch4_fod_msb[6]	ch4_fod_msb[5]	ch4_fod_msb[4]	ch4_fod_msb[3]	ch4_fod_msb[2]	ch4_fod_msb[1]	ch4_fod_msb[0]	ch3_1p8v_det	ch3_fod_dlymode	ch3_ssc_type	ch3_ssc_spread[1]	ch3_ssc_spread[0]	ch3_ssc_fmod[1]

Table 76. EEPROM, Page 0 (continued)

WORD NO.	SECTION	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
21h	Page 0	ch4_iod_div[0]	ch4_fod[8]	ch4_fod[7]	ch4_fod[6]	ch4_fod[5]	ch4_fod[4]	ch4_fod[3]	ch4_fod[2]	ch4_fod[1]	ch4_fod[0]	ch4_fod_msb[15]	ch4_fod_msb[14]	ch4_fod_msb[13]	ch4_fod_msb[12]	ch4_fod_msb[11]	ch4_fod_msb[10]
22h	Page 0	ch4_mux[0]	ch4_iod_mux[1]	ch4_iod_mux[0]	ch4_iod_div[13]	ch4_iod_div[12]	ch4_iod_div[11]	ch4_iod_div[10]	ch4_iod_div[9]	ch4_iod_div[8]	ch4_iod_div[7]	ch4_iod_div[6]	ch4_iod_div[5]	ch4_iod_div[4]	ch4_iod_div[3]	ch4_iod_div[2]	ch4_iod_div[1]
23h	Page 0	0	ch4_glitch_less_en	ch4_sync_delay[4]	ch4_sync_delay[3]	ch4_sync_delay[2]	ch4_sync_delay[1]	ch4_sync_delay[0]	ch4_sync_en	ch4_mute_sel	ch4_mute	0	0	ch4_outb_uf_ctrl[2]	ch4_outb_uf_ctrl[1]	ch4_outb_uf_ctrl[0]	ch4_mux[1]
24h	Page 0	0	0	1	1	pll_en_cp	ch0_lvcm_os_drv[1]	ch0_lvcm_os_drv[0]	1	ch4_1p8v_det	ch4_fod_dlymode	ch4_ssc_type	ch4_ssc_spread[1]	ch4_ssc_spread[0]	ch4_ssc_fmod[1]	ch4_ssc_fmod[0]	ch4_ssc_en
25h	Page 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 77. EEPROM, Page 1

WORD NO.	SECTION	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
26h	Page 1	gpio4_input_sel[3]	gpio4_input_sel[2]	gpio4_input_sel[1]	gpio4_input_sel[0]	gpio1_input_sel[3]	gpio1_input_sel[2]	gpio1_input_sel[1]	gpio1_input_sel[0]	i2c_a0	gpio0_input_sel	gpio4_dir_sel	gpio1_dir_sel	gpio0_dir_sel	zdm_clocksel	zdm_mode	mode
27h	Page 1	gpio4_output_sel[3]	gpio4_output_sel[2]	gpio4_output_sel[1]	gpio4_output_sel[0]	gpio1_output_sel[3]	gpio1_output_sel[2]	gpio1_output_sel[1]	gpio1_output_sel[0]	fod_size[5]	fod_size[4]	fod_size[3]	fod_size[2]	fod_size[1]	fod_size[0]	ref_mux_src	ref_mux
28h	Page 1	pdn_pll_sscclk	pdn_ch4	pdn_ch4_ssc	pdn_ch3	pdn_ch3_ssc	pdn_ch2	pdn_ch2_ssc	pdn_ch1	pdn_ch1_ssc	iod_size	rsrvd_1[1]	rsrvd_1[0]	gpio0_output_sel[3]	gpio0_output_sel[2]	gpio0_output_sel[1]	gpio0_output_sel[0]
29h	Page 1	ip_xo_clock_ad[2]	ip_xo_clock_ad[1]	ip_xo_clock_ad[0]	ip_xo_gm_fine[1]	ip_xo_gm_fine[0]	ip_xo_gm[3]	ip_xo_gm[2]	ip_xo_gm[1]	ip_xo_gm[0]	xin_inbuf_ctrl[1]	xin_inbuf_ctrl[0]	zdm_auto	bypass_cal	bypass_config	pdn_pll_psb	pdn_pll_psa
2Ah	Page 1	ip_bypass_en_ch3	ip_bypass_en_ch2	ip_bypass_en_ch1	ip_bypass_en_ch0	ip_bypass_mux	ip_rdiv[7]	ip_rdiv[6]	ip_rdiv[5]	ip_rdiv[4]	ip_rdiv[3]	ip_rdiv[2]	ip_rdiv[1]	ip_rdiv[0]	ref_inbuf_ctrl	ip_xo_clock_ad[4]	ip_xo_clock_ad[3]
2Bh	Page 1	pll_ndiv[13]	pll_ndiv[12]	pll_ndiv[11]	pll_ndiv[10]	pll_ndiv[9]	pll_ndiv[8]	pll_ndiv[7]	pll_ndiv[6]	pll_ndiv[5]	pll_ndiv[4]	pll_ndiv[3]	pll_ndiv[2]	pll_ndiv[1]	pll_ndiv[0]	ip_ldo_load_en	ip_bypass_en_ch4
2Ch	Page 1	pll_cp_up[3]	pll_cp_up[2]	pll_cp_up[1]	pll_cp_up[0]	pll_cp_dn[5]	pll_cp_dn[4]	pll_cp_dn[3]	pll_cp_dn[2]	pll_cp_dn[1]	pll_cp_dn[0]	pll_psb[1]	pll_psb[0]	pll_psa[1]	pll_psa[0]	pll_psfb[1]	pll_psfb[0]
2Dh	Page 1	pll_lf_zcap[4]	pll_lf_zcap[3]	pll_lf_zcap[2]	pll_lf_zcap[1]	pll_lf_zcap[0]	pll_lf_res[3]	pll_lf_res[2]	pll_lf_res[1]	pll_lf_res[0]	pll_lf_pcap[4]	pll_lf_pcap[3]	pll_lf_pcap[2]	pll_lf_pcap[1]	pll_lf_pcap[0]	pll_cp_up[5]	pll_cp_up[4]
2Eh	Page 1	ch1_fod_msb[15]	ch1_fod_msb[14]	ch1_fod_msb[13]	ch1_fod_msb[12]	ch1_fod_msb[11]	ch1_fod_msb[10]	ch1_fod_msb[9]	ch1_fod_msb[8]	ch1_fod_msb[7]	ch1_fod_msb[6]	ch1_fod_msb[5]	ch1_fod_msb[4]	ch1_fod_msb[3]	ch1_fod_msb[2]	ch1_fod_msb[1]	ch1_fod_msb[0]
2Fh	Page 1	ch1_iod_div[6]	ch1_iod_div[5]	ch1_iod_div[4]	ch1_iod_div[3]	ch1_iod_div[2]	ch1_iod_div[1]	ch1_iod_div[0]	ch1_iod[8]	ch1_iod[7]	ch1_iod[6]	ch1_iod[5]	ch1_iod[4]	ch1_iod[3]	ch1_iod[2]	ch1_iod[1]	ch1_iod[0]
30h	Page 1	0	0	ch1_outbuf_ctrl[2]	ch1_outbuf_ctrl[1]	ch1_outbuf_ctrl[0]	ch1_mux[1]	ch1_mux[0]	ch1_iod_mux[1]	ch1_iod_mux[0]	ch1_iod_div[13]	ch1_iod_div[12]	ch1_iod_div[11]	ch1_iod_div[10]	ch1_iod_div[9]	ch1_iod_div[8]	ch1_iod_div[7]
31h	Page 1	ch1_ssc_type	ch1_ssc_spread[1]	ch1_ssc_spread[0]	ch1_ssc_fmod[1]	ch1_ssc_fmod[0]	ch1_ssc_en	0	ch1_glitch_less_en	ch1_sync_delay[4]	ch1_sync_delay[3]	ch1_sync_delay[2]	ch1_sync_delay[1]	ch1_sync_delay[0]	ch1_sync_en	ch1_mute_sel	ch1_mute
32h	Page 1	ch2_fod_msb[13]	ch2_fod_msb[12]	ch2_fod_msb[11]	ch2_fod_msb[10]	ch2_fod_msb[9]	ch2_fod_msb[8]	ch2_fod_msb[7]	ch2_fod_msb[6]	ch2_fod_msb[5]	ch2_fod_msb[4]	ch2_fod_msb[3]	ch2_fod_msb[2]	ch2_fod_msb[1]	ch2_fod_msb[0]	ch1_1p8v_det	ch1_fod_dlymode
33h	Page 1	ch2_iod_div[4]	ch2_iod_div[3]	ch2_iod_div[2]	ch2_iod_div[1]	ch2_iod_div[0]	ch2_fod[8]	ch2_fod[7]	ch2_fod[6]	ch2_fod[5]	ch2_fod[4]	ch2_fod[3]	ch2_fod[2]	ch2_fod[1]	ch2_fod[0]	ch2_fod_msb[15]	ch2_fod_msb[14]
34h	Page 1	ch2_outbuf_ctrl[2]	ch2_outbuf_ctrl[1]	ch2_outbuf_ctrl[0]	ch2_mux[1]	ch2_mux[0]	ch2_iod_mux[1]	ch2_iod_mux[0]	ch2_iod_div[13]	ch2_iod_div[12]	ch2_iod_div[11]	ch2_iod_div[10]	ch2_iod_div[9]	ch2_iod_div[8]	ch2_iod_div[7]	ch2_iod_div[6]	ch2_iod_div[5]
35h	Page 1	ch2_ssc_spread[0]	ch2_ssc_fmod[1]	ch2_ssc_fmod[0]	ch2_ssc_en	0	ch2_glitch_less_en	ch2_sync_delay[4]	ch2_sync_delay[3]	ch2_sync_delay[2]	ch2_sync_delay[1]	ch2_sync_delay[0]	ch2_sync_en	ch2_mute_sel	ch2_mute	ch2_cmos_pol[1]	ch2_cmos_pol[0]
36h	Page 1	ch3_fod_msb[11]	ch3_fod_msb[10]	ch3_fod_msb[9]	ch3_fod_msb[8]	ch3_fod_msb[7]	ch3_fod_msb[6]	ch3_fod_msb[5]	ch3_fod_msb[4]	ch3_fod_msb[3]	ch3_fod_msb[2]	ch3_fod_msb[1]	ch3_fod_msb[0]	ch2_1p8v_det	ch2_fod_dlymode	ch2_ssc_type	ch2_ssc_spread[1]
37h	Page 1	ch3_iod_div[2]	ch3_iod_div[1]	ch3_iod_div[0]	ch3_fod[8]	ch3_fod[7]	ch3_fod[6]	ch3_fod[5]	ch3_fod[4]	ch3_fod[3]	ch3_fod[2]	ch3_fod[1]	ch3_fod[0]	ch3_fod_msb[15]	ch3_fod_msb[14]	ch3_fod_msb[13]	ch3_fod_msb[12]
38h	Page 1	ch3_outbuf_ctrl[0]	ch3_mux[1]	ch3_mux[0]	ch3_iod_mux[1]	ch3_iod_mux[0]	ch3_iod_div[13]	ch3_iod_div[12]	ch3_iod_div[11]	ch3_iod_div[10]	ch3_iod_div[9]	ch3_iod_div[8]	ch3_iod_div[7]	ch3_iod_div[6]	ch3_iod_div[5]	ch3_iod_div[4]	ch3_iod_div[3]
39h	Page 1	ch3_ssc_fmod[0]	ch3_ssc_en	0	ch3_glitch_less_en	ch3_sync_delay[4]	ch3_sync_delay[3]	ch3_sync_delay[2]	ch3_sync_delay[1]	ch3_sync_delay[0]	ch3_sync_en	ch3_mute_sel	ch3_mute	ch3_cmos_pol[1]	ch3_cmos_pol[0]	ch3_outbuf_ctrl[2]	ch3_outbuf_ctrl[1]
3Ah	Page 1	ch4_fod_msb[9]	ch4_fod_msb[8]	ch4_fod_msb[7]	ch4_fod_msb[6]	ch4_fod_msb[5]	ch4_fod_msb[4]	ch4_fod_msb[3]	ch4_fod_msb[2]	ch4_fod_msb[1]	ch4_fod_msb[0]	ch3_1p8v_det	ch3_fod_dlymode	ch3_ssc_type	ch3_ssc_spread[1]	ch3_ssc_spread[0]	ch3_ssc_fmod[1]

Table 77. EEPROM, Page 1 (continued)

WORD NO.	SECTION	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3Bh	Page 1	ch4_iod_div[0]	ch4_fod[8]	ch4_fod[7]	ch4_fod[6]	ch4_fod[5]	ch4_fod[4]	ch4_fod[3]	ch4_fod[2]	ch4_fod[1]	ch4_fod[0]	ch4_fod_msb[15]	ch4_fod_msb[14]	ch4_fod_msb[13]	ch4_fod_msb[12]	ch4_fod_msb[11]	ch4_fod_msb[10]
3Ch	Page 1	ch4_mux[0]	ch4_iod_mux[1]	ch4_iod_mux[0]	ch4_iod_div[13]	ch4_iod_div[12]	ch4_iod_div[11]	ch4_iod_div[10]	ch4_iod_div[9]	ch4_iod_div[8]	ch4_iod_div[7]	ch4_iod_div[6]	ch4_iod_div[5]	ch4_iod_div[4]	ch4_iod_div[3]	ch4_iod_div[2]	ch4_iod_div[1]
3Dh	Page 1	0	ch4_glitch_less_en	ch4_sync_delay[4]	ch4_sync_delay[3]	ch4_sync_delay[2]	ch4_sync_delay[1]	ch4_sync_delay[0]	ch4_sync_en	ch4_mute_sel	ch4_mute	0	0	ch4_outb_uf_ctrl[2]	ch4_outb_uf_ctrl[1]	ch4_outb_uf_ctrl[0]	ch4_mux[1]
3Eh	Page 1	0	0	1	1	pll_en_cp	ch0_lvcm_os_drv[1]	ch0_lvcm_os_drv[0]	1	ch4_1p8v_det	ch4_fod_dlymode	ch4_ssc_type	ch4_ssc_spread[1]	ch4_ssc_spread[0]	ch4_ssc_fmod[1]	ch4_ssc_fmod[0]	ch4_ssc_en
3Fh	Page 1	1	1	0	0	1	0	0	1	0	1	1	0	0	1	0	0

9 Application and Implementation

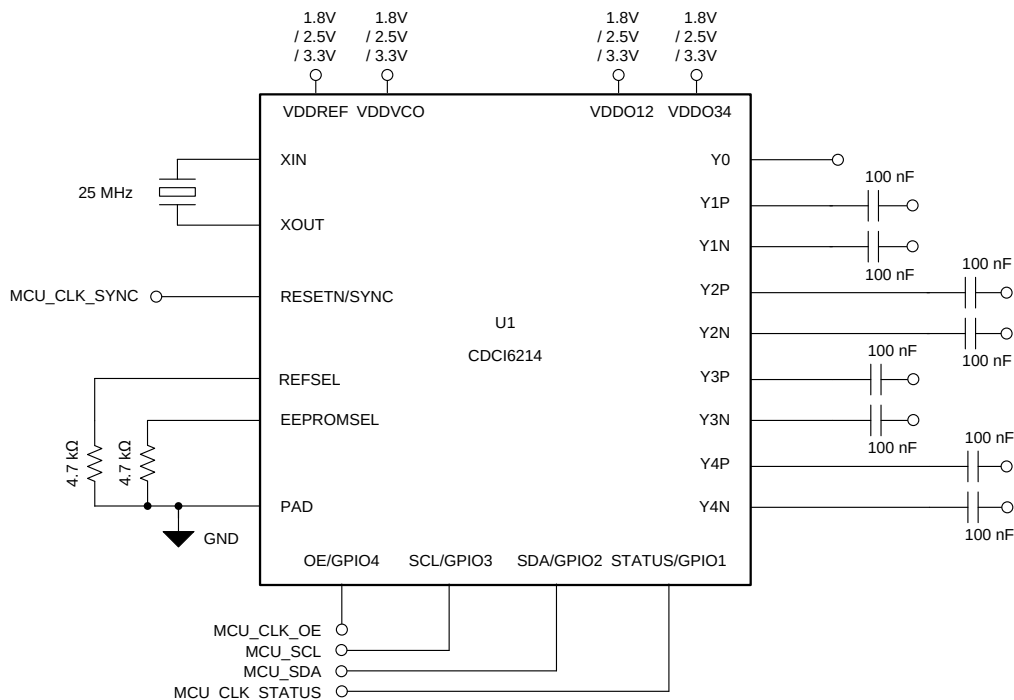
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

An ultra-low power clock generator is ideal to drive clocks in industrial, portable and data center applications. The device is flexible in its configuration and be pre-preprogrammed with two separate configuration. For example a production test and an application configuration, or two different configurations for two flavors of a product. The internal EEPROM is protected by a CRC hash which is available as a status bit. The two EEPROM pages are selected using a control pin. As each major block of the device is powered by its own supply pin, the device can easily be used for signal translation and to accommodate various supply voltages which may be available in a system. Up to five different frequencies can be generated from a single device and feed different parts of an application. Each of the four differential outputs supports various signal standards. On one hand the general purpose pin functionality allows to provide status information to other parts of the system, on the other hand it adds modularity and flexibility to an application. Clock outputs can be muted individually or globally, the division ratio updated, the output dividers synchronized and a spread spectrum function enabled or disabled. The clock generator PLL can also be used in a zero delay mode which will compensate most of the seen phase delay between an external reference clock and the output clocks. Together with an external feedback option this allows to compensate traces on top of the digital delay steps provided inside the device. All these features make the ultra-low power clock generator for design library integration and re-use in modular projects.

9.2 Typical Applications



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Figure 90. Typical Serial Interface Application Schematic

Typical Applications (continued)

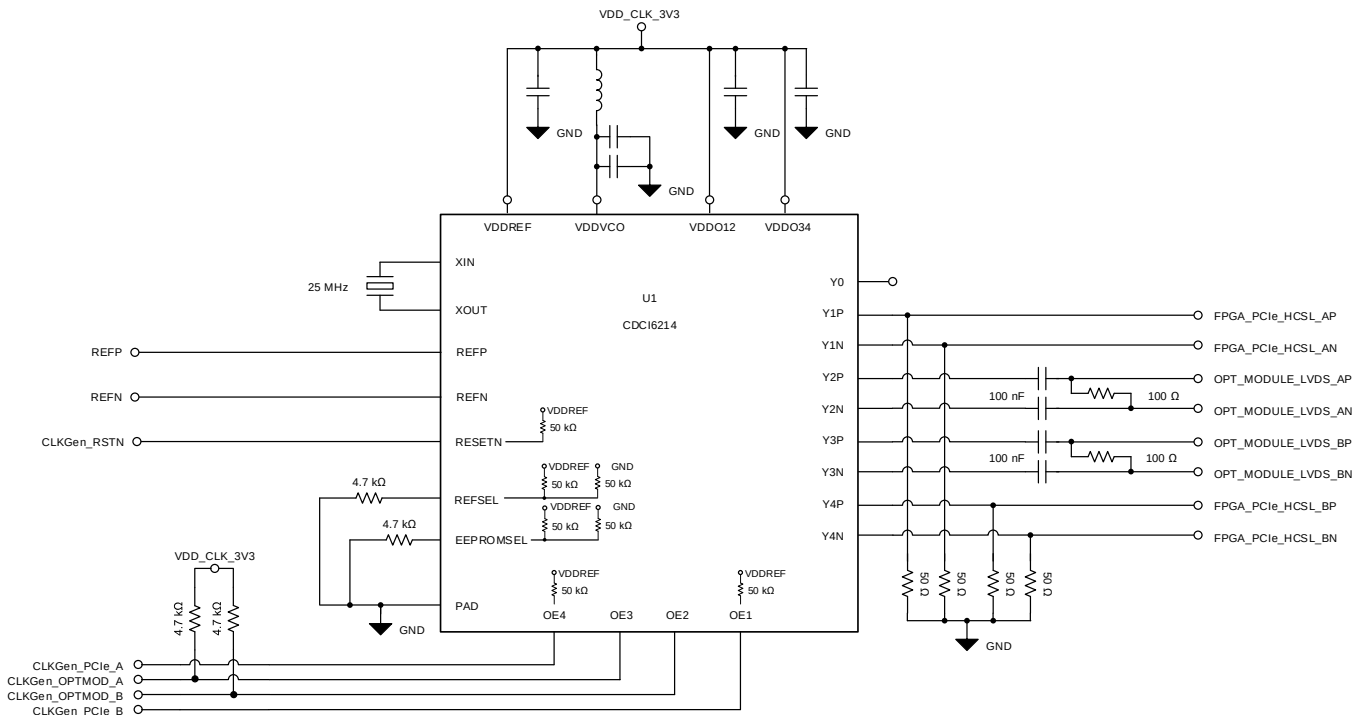


Figure 91. Typical Individual Output Enable Application Schematic

9.2.1 Design Requirements

For this example, the design parameters are listed in [Table 78](#)

Table 78. Design Parameters

PARAMETER	EXAMPLE VALUE
t_{VDD}	Larger than 50 μ s and smaller than 3 ms
t_{PWL_SYNC}	Larger than $(1 / f_{XIN})$
f_{XIN}	Crystal 8 MHz to 50 MHz
dV_{IN} / dT	Input slew rate for external clock reference better than 3 V / ns

9.2.2 Detailed Design Procedure

For this application, TI recommends the following steps:

1. Decide how the device shall receive the register settings to plan for in-system programming of the EEPROM.
2. Choose which operation mode to use on the device (I²C or GPIOs) and which pins are inputs and which are outputs (see registers [GENERIC0](#), [GENERIC1](#), and [GENERIC2](#)).
3. Consider that the serial interface and the GPIOs are supplied by VDDREF as well as the input pins (for example, a 3.3-V crystal oscillator (XO) driving XIN forces uses 3.3-V I²C).
4. Keep track of which voltage levels the output supplies will have. There are configuration bits in the output channels (see [CH1_CTRL5](#), [CH2_CTRL5](#), [CH3_CTRL5](#), and [CH4_CTRL5](#)).
5. Consider which output frequency has the most stringent phase noise specifications. Select this frequency to decide on the reference and VCO frequency.
6. Cross-check if your specific bandwidth requirement for an external reference can be achieved using the internal loop filter components (see registers [PLL1](#) and [PLL2](#)).
7. Optimize the clock distribution using output muxes to run the least amount of blocks to conserve power,

8. For HCSL output buffer format, optimize the signal integrity and slew rate at the receiver input using a series resistor between device pin and the 50 Ω termination to GND. Y1, Y4 provide higher slew rates compared to Y2, Y3.

Use Equation 6 through Equation 9 to calculate the a basic frequency plan or use the provided software TICS Pro to generate settings.

NOTE

The user has to ensure PLL stability is given by applying the adequate loop filter and charge pump settings. A phase margin of $\geq 68^\circ$ is recommended. The target bandwidth is recommended between 600 kHz .. 1100 kHz.

$$f_{Y0} = f_{XIN} = f_{REF} \quad (6)$$

$$f_{PFD} = f_{REF} / ip_ref_div$$

where

- $ip_ref_div \geq 1$
- $1 \text{ MHz} \leq f_{PFD} \leq 100 \text{ MHz}$ (7)

$$f_{VCO} = f_{PFD} \cdot pll_nc \cdot (pll_ps + 4)$$

with

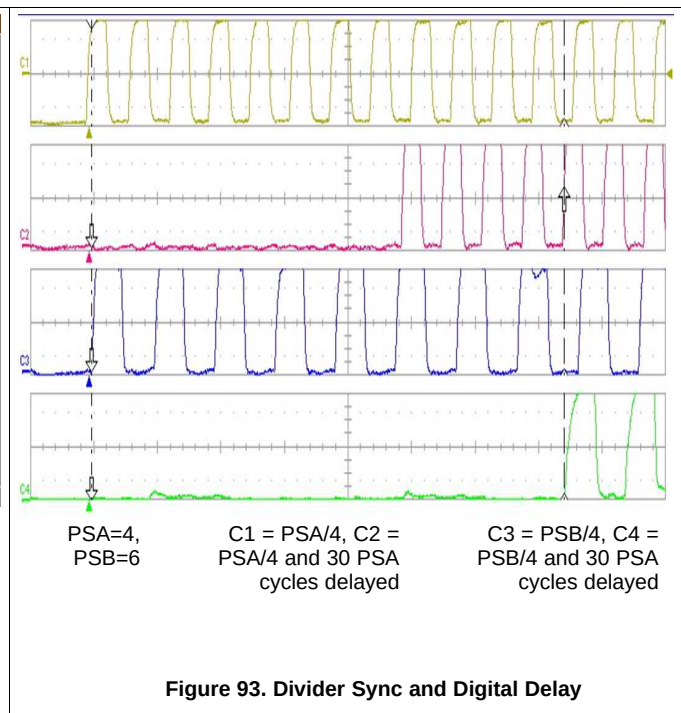
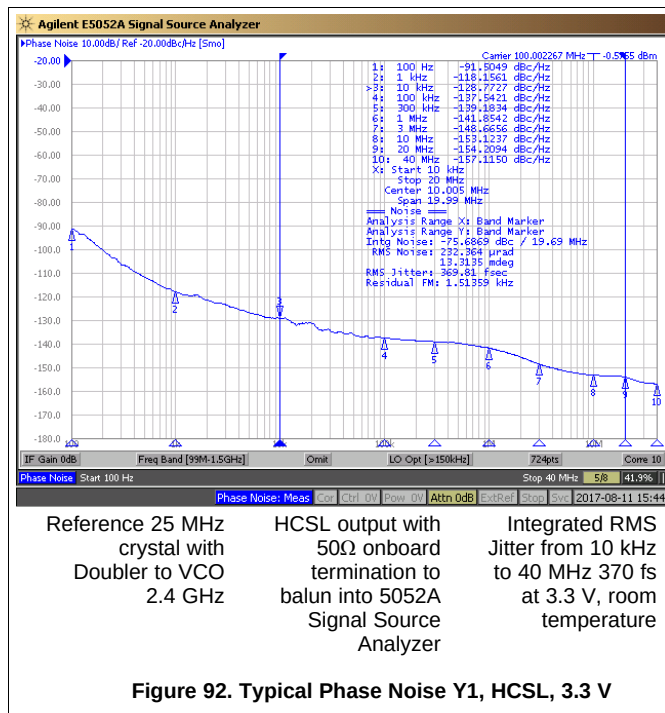
- $2400 \leq f_{VCO} \leq 2800$
- $0 \leq pll_ps \leq 2$ (8)

$$f_{Y[4:1]} = f_{VCO} / ((pll_ps[ab] + 4) \cdot ch[4:1]_{iod_div})$$

with

- $0 \leq pll_ps[ab] \leq 2$
- $1 \leq ch[4:1]_{iod_div} \leq 16383$
- $44.1 \text{ kHz} \leq f_{Y[4:1]} \leq 350 \text{ MHz}$ (9)

9.2.3 Application Curves



9.3 Do's and Don'ts

The maximum swing and level must match to the applied VDDREF (for example, for a 3.3-V XO as reference, VDDREF must be 3.3 V).

9.4 Initialization Setup

The device digital logic starts after the internal power-on-release circuit triggered (POR). The digital core is connected to the VDDREF domain. The EEPROM settings are loaded into the device registers and the new settings applied to the device. The EEPROM page is selected according to the EEPROMSEL pin logic level. A low level loads *page 0*, and a logic high level loads *page 1*. By default, the differential outputs are muted for the initial VCO calibration and PLL lock process. After the PLL circuit achieved a phase lock to the input reference, the output dividers are synchronized and then released to operation. By default, pin 8 is configured as RESETN pin (see [gpio0_dir_sel](#) and [gpio0_input_sel](#)). The start of the initialization sequence, as well the as serial interface, can be kept in reset using RESETN= LOW. When pin 8 is not configured as RESETN, the device initialization relies on the POR triggered by application of VDDREF.

Initialization Setup (continued)

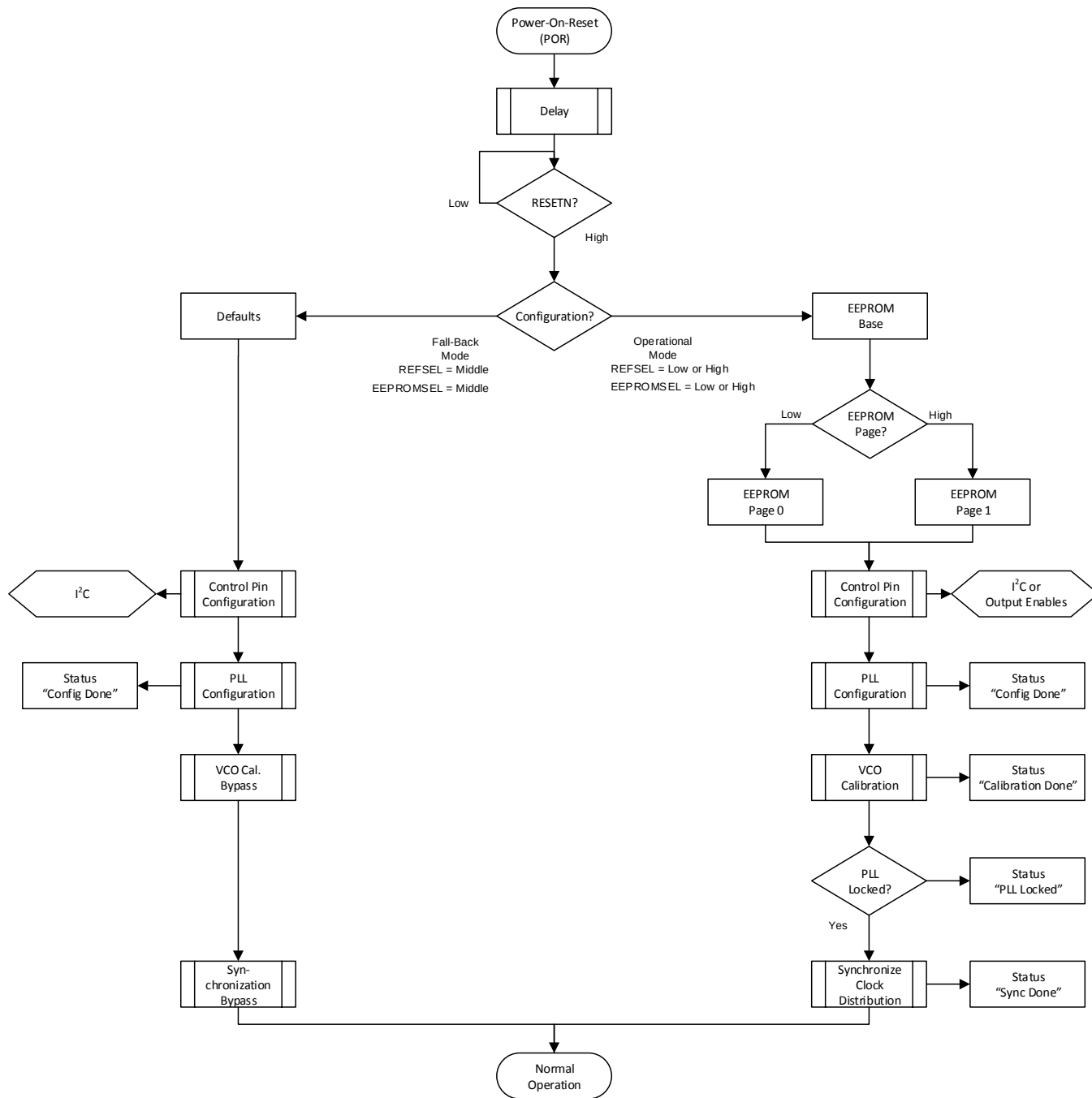


Figure 94. Initialization Flow Chart

The pins 8, 11, 12, 19, and 20 are general-purpose inputs and outputs (GPIO). The functions are determined through the register settings saved in the selected EEPROM page. See [GENERIC0](#), [GENERIC1](#), and [GENERIC2](#) for the relevant bit-fields.

The EEPROM allows to choose between two modes of operation: pin Mode and serial interface mode. This is done using [mode](#).

10 Power Supply Recommendations

10.1 Power-Up Sequence

There are no restrictions from the device for applying power to the supply pins. From an application perspective, TI recommends to either apply all VDDs at the same time or apply VDDREF first. The digital core is connected to VDDREF and thus settings of the EEPROM are applied automatically.

10.2 De-Coupling

TI recommends isolating all power supplies using a ferrite bead and provide decoupling for each of the supplies. TI also recommends optimizing the decoupling for the respective layout and consider the power supply impedance and optimize for the individual frequency plan.

An example for a decoupling per supply pin: 1x 4.7 μ F, 1x 470 nF, and 1x 100 nF.

11 Layout

11.1 Layout Guidelines

For this example, follow these guidelines:

- Isolate inputs and outputs using a GND shield. [Figure 95](#) routes all inputs and outputs as differential pairs.
- Isolate outputs to adjacent outputs when generating multiple frequencies.
- Isolate the crystal area, connect the GND pads of the crystal package and flood the adjacent area. [Figure 96](#) shows a foot print which supports multiple crystal sizes.
- Try to avoid impedance jumps in the fan-in and fan-out areas when possible.
- Use five VIAs to connect the thermal pad to a solid GND plane. Full-through VIAs are preferred.
- Place decoupling capacitors with small capacitance values very close to the supply pins. Try to place them very close on the same layer or directly on the backside layer. Larger values can be placed more far away. [Figure 96](#) shows three de-coupling capacitors close to the device. Ferrite beads are recommended to isolate the different frequency domains and the VDDVCO domain.
- Preferably use multiple VIAs to connect wide supply traces to the respective power planes.

11.2 Layout Examples

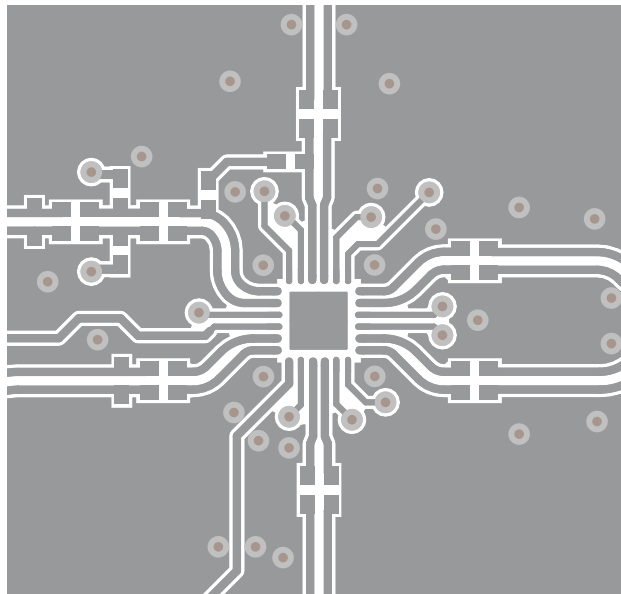


Figure 95. Layout Example, Top Layer

Layout Examples (continued)

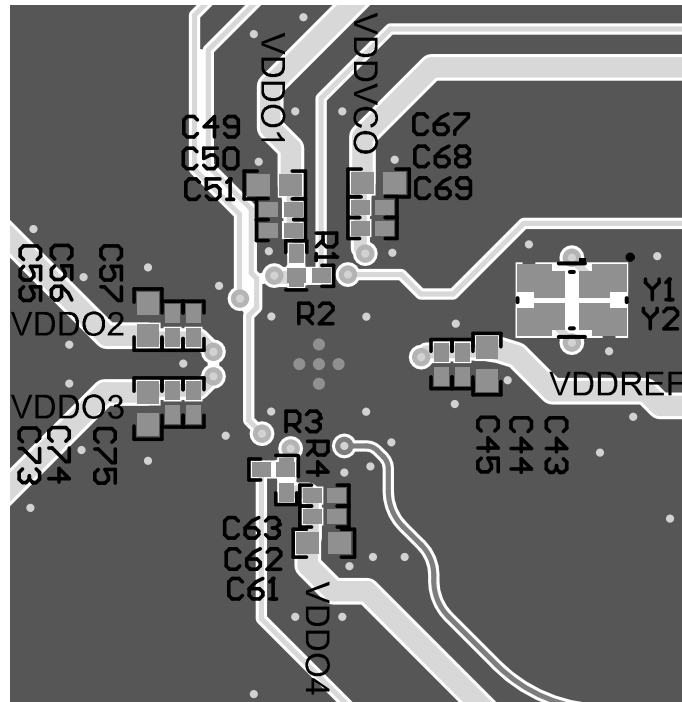


Figure 96. Layout Example, Bottom Layer

Land Pattern Example

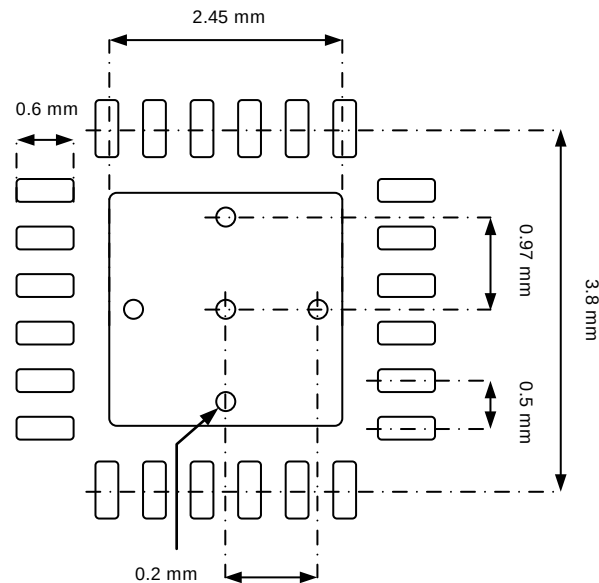


Figure 97. Layout Example, Land Pattern

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

Contact your TI representative for more information.

12.1.2 Device Nomenclature

CDCI6214 - 62= clock generator 1= 1x PLL 4=4x outputs I = individual output enables

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

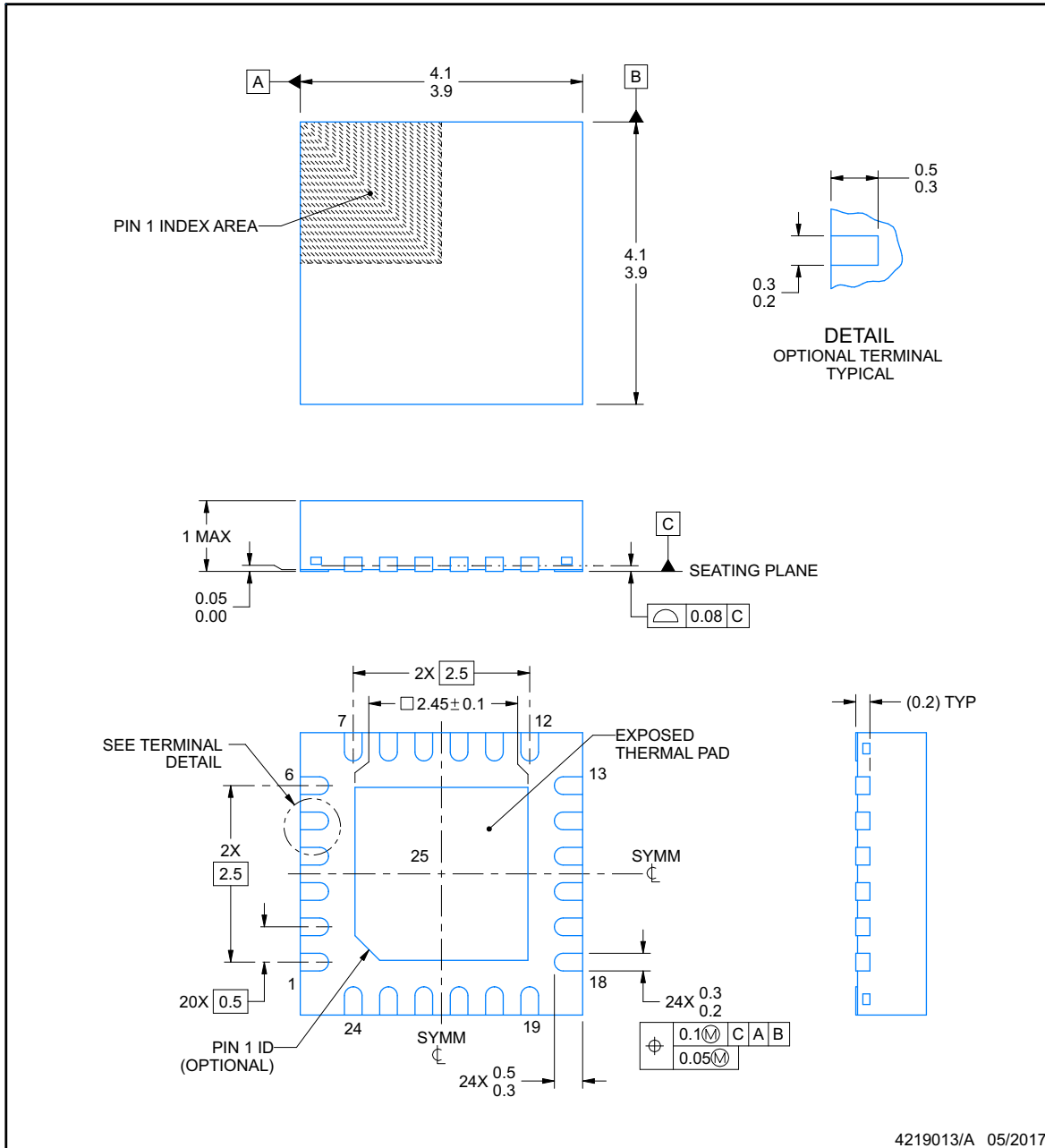


RGE0024B

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

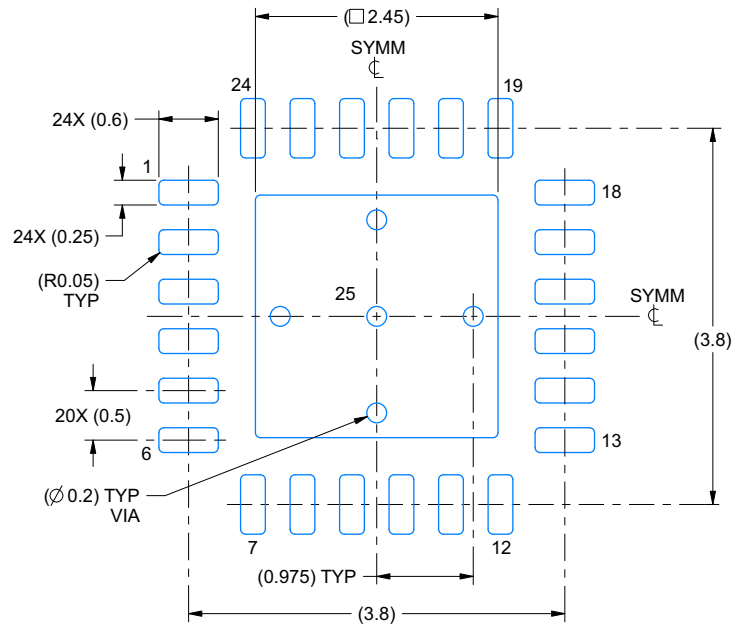
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

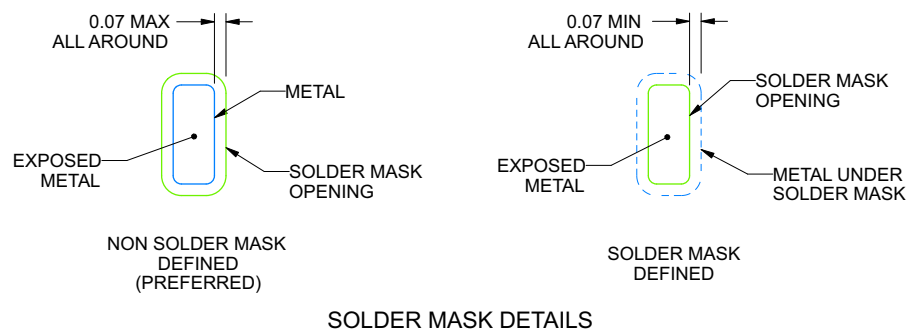
RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

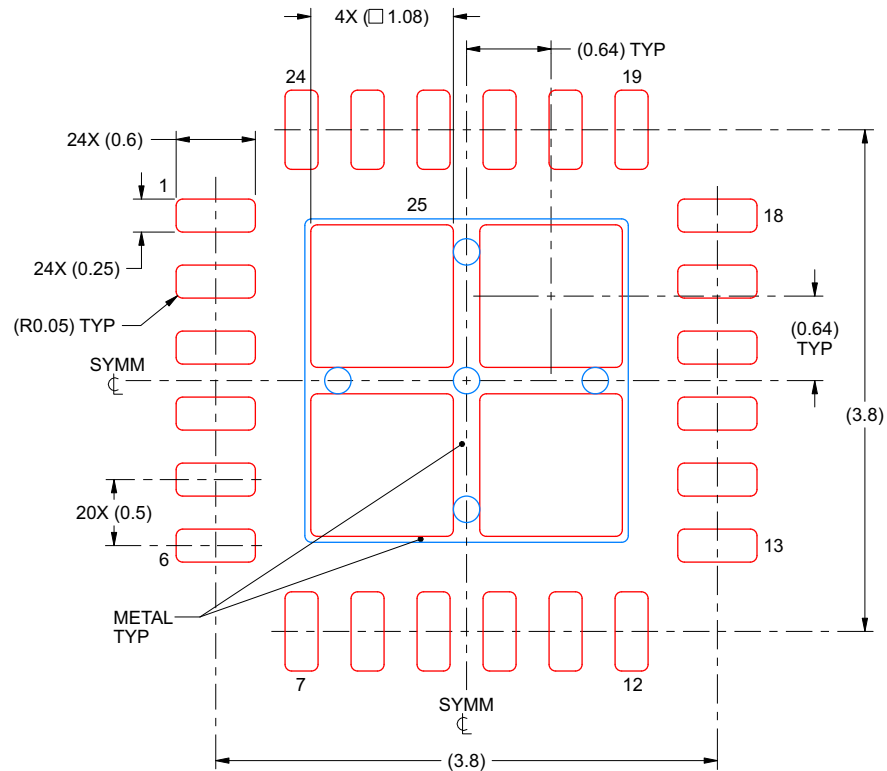
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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN**RGE0024B****VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
 78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
 SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCI6214RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCI 6214A1	Samples
CDCI6214RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCI 6214A1	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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