

## 12-Bit Input-Buffered 80 MSPS ADC with JESD204A Output Interface

Check for Samples: [ADS61JB23](#)

### FEATURES

- **Output Interface:**
  - Single-Lane and Dual-Lane Interfaces
  - Maximum Data Rate of 1.6 Gbps
  - Meets JESD204A Specification
  - CML Outputs with Current Programmable from 2 mA – 32 mA
- **Power Dissipation:**
  - 440 mW at 80 MSPS in Single Lane Mode
  - Power Scales Down with Clock Rate
- **Input Interface: Buffered Analog Inputs**
- **71.7 dBFS SNR at 70 MHz IF**
- **Analog Input FSR: 2 Vpp**
- **External and Internal (trimmed) Reference Support**
- **1.8V Supply (Analog and digital), 3.3 V Supply for Input Buffer**
- **Programmable Digital Gain: 0dB – 6dB**
- **Straight Offset Binary or Twos Complement Output**
- **Package:**
  - 6 mm x 6 mm QFN-40

### APPLICATIONS

- **Wireless Base-station Infrastructure**
- **Test and Measurement Instrumentation**

### DESCRIPTION

The ADS61JB23 is a high-performance, low-power, single channel analog-to-digital converter with an integrated JESD204A output interface. Available in a 6 mm x 6 mm QFN package, with both single-lane and dual-lane output modes, the ADS61JB23 offers an unprecedented level of compactness. The output interface is compatible to the JESD204A standard, with an additional mode (as per IEEE Std 802.3-2002 part3, Clause 36.2.4.12) to interface seamlessly to the TI TLK family of SERDES transceivers. Equally impressive is the inclusion of an on-chip analog input buffer, providing isolation between the sample/hold switches and higher and more consistent input impedance.

The ADS61JB23 is specified over the industrial temperature range (–40°C to 85°C).

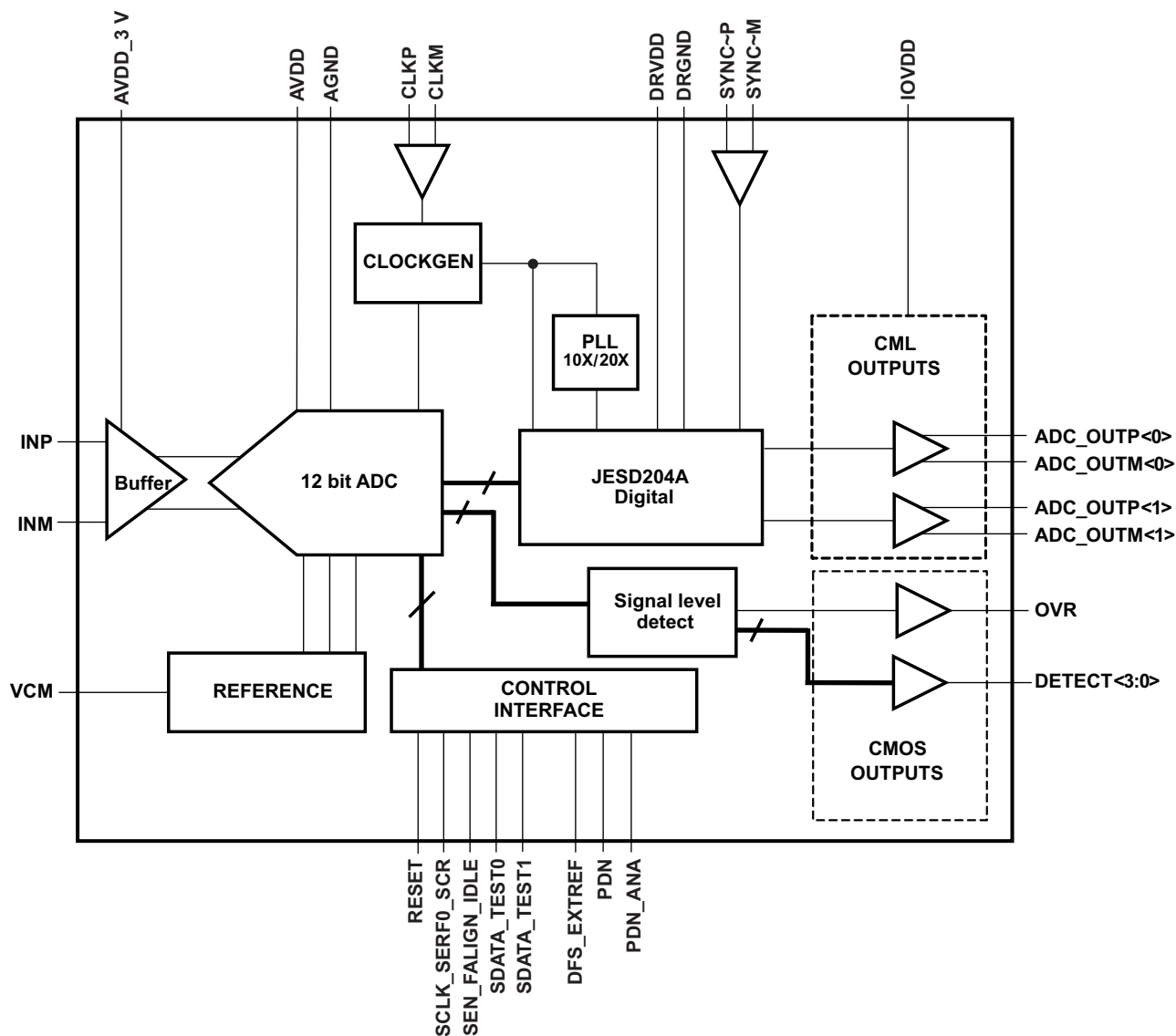


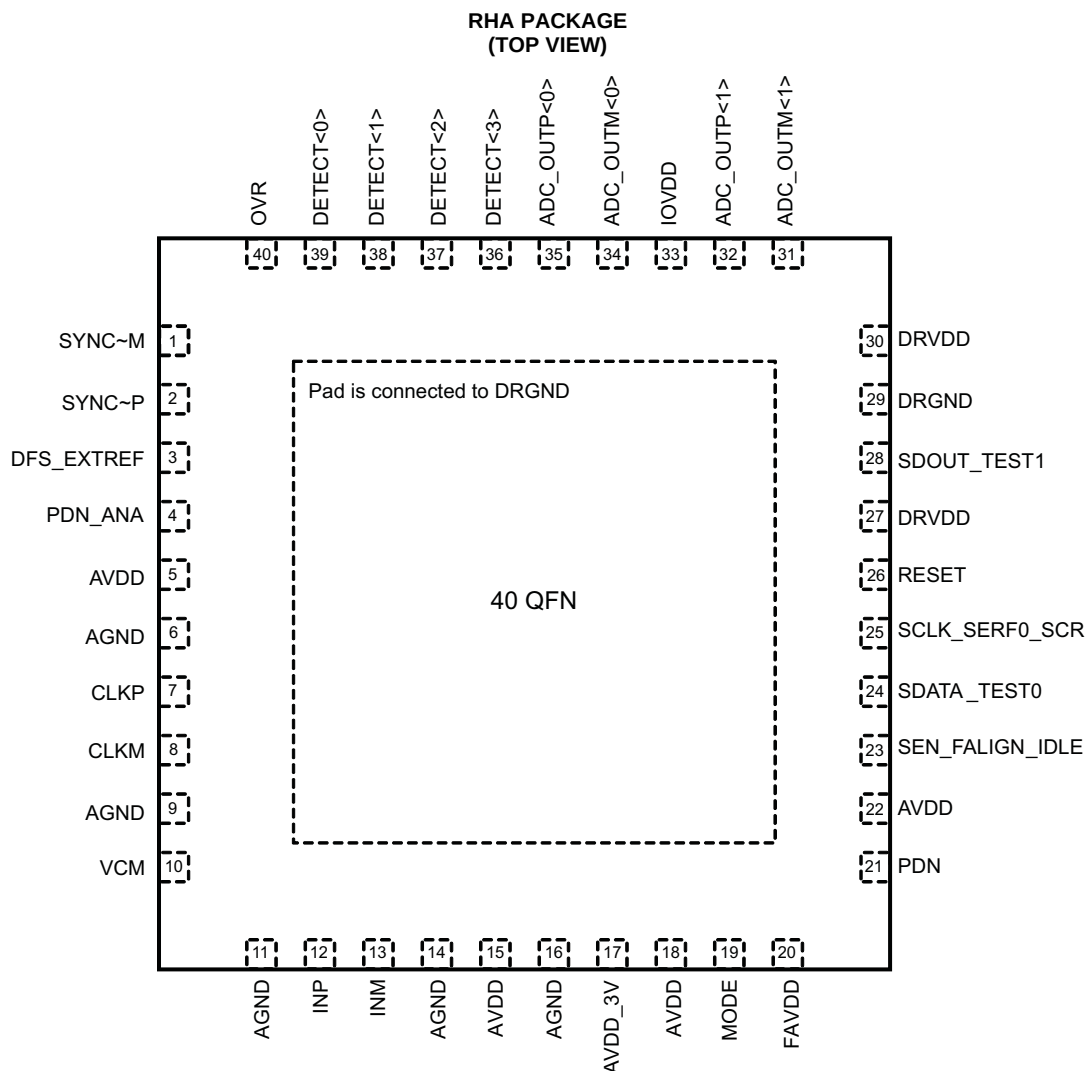
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## FUNCTIONAL BLOCK DIAGRAM





### PIN FUNCTIONS

| PIN         |                      | DESCRIPTION                           |
|-------------|----------------------|---------------------------------------|
| NAME        | NO.                  |                                       |
| ADC_OUTM<1> | 31                   | CML output Lane 2 – Negative output   |
| ADC_OUTM<0> | 34                   | CML output Lane 1 – Negative output   |
| ADC_OUTP<1> | 32                   | CML output Lane 2 – Positive output   |
| ADC_OUTP<0> | 35                   | CML output Lane 1 – Positive output   |
| AGND        | 5, 6, 9, 11, 14, 16, | Analog ground                         |
| AVDD        | 15, 18, 22           | Analog supply, 1.8 V                  |
| AVDD_3V     | 17                   | Analog supply for input buffer, 3.3 V |
| CLKM        | 8                    | Conversion clock – Negative input     |
| CLKP        | 7                    | Conversion clock – Positive input     |
| DRGND       | 29                   | Digital ground                        |
| DRVDD       | 27, 30               | Digital supply, 1.8 V                 |

**PIN FUNCTIONS (continued)**

| PIN              |     | DESCRIPTION                                                                                                                                |
|------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------|
| NAME             | NO. |                                                                                                                                            |
| DETECT<3>        | 36  | Signal level detect output pins: Can be used to either output a 4-bit ADC code with low latency or to output a 16-level RMS power estimate |
| DETECT<2>        | 37  |                                                                                                                                            |
| DETECT<1>        | 38  |                                                                                                                                            |
| DETECT<0>        | 39  |                                                                                                                                            |
| DFS_EXTREF       | 3   | 4-level analog control for Data Format select and Internal/ External reference mode                                                        |
| FAVDD            | 20  | Fuse supply – connect externally to AVDD, 1.8 V                                                                                            |
| IOVDD            | 33  | CML buffer supply – 1.2 V to 1.9 V                                                                                                         |
| INM              | 13  | Analog input - Negative                                                                                                                    |
| INP              | 12  | Analog input – Positive                                                                                                                    |
| MODE             | 19  | 4-level control for Serial interface/ Parallel interface modes selection                                                                   |
| OVR              | 40  | Over-range output                                                                                                                          |
| PDN              | 21  | Full chip Powerdown (also referred to as Complete Powerdown mode)                                                                          |
| PDN_ANA          | 4   | Analog section power down, JESD interface still active. This is referred to as fast recovery powerdown mode                                |
| RESET            | 26  | Chip Reset input                                                                                                                           |
| SCLK_SERF0_SCR   | 25  | In Serial interface mode : Serial clock input In parallel interface mode : 4-level control for JESD modes (single/dual lane & scrambling)  |
| SDATA_TEST0      | 24  | In Serial interface mode : Serial data input In parallel interface mode : JESD test mode                                                   |
| SDOUT_TEST1      | 28  | In Serial interface mode : Serial data output (for register readout) In parallel interface mode : JESD test mode                           |
| SEN_FALIGN_I_DLE | 23  | In Serial interface mode : Serial enable (Chip select) In parallel interface mode : 4-level control for JESD modes                         |
| SYNC~M           | 1   | JESD Synchronization request – Negative input                                                                                              |
| SYNC~P           | 2   | JESD Synchronization request – Positive input                                                                                              |
| VCM              | 10  | Common mode output for setting input common mode: 1.95V, Reference input in external reference mode                                        |

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

|                                                    |                                      | VALUE                          | UNIT |
|----------------------------------------------------|--------------------------------------|--------------------------------|------|
| AVDD                                               | Supply voltage range                 | −0.3 to +2.2                   | V    |
| DRVDD                                              |                                      | −0.3 to +2.2                   | V    |
| IOVDD                                              |                                      | −0.3 to +2.2                   | V    |
| AVDD_3V                                            |                                      | −0.3 to +3.9                   | V    |
| Voltage between AGND and DRGND                     |                                      | −0.3 to +0.3                   | V    |
| Voltage applied to external VCM pin                |                                      | −0.3 to +2.2                   | V    |
| Voltage applied to analog input pins               |                                      | −0.3 to min (3, AVDD_3V + 0.3) | V    |
| Voltage applied to digital input pins              |                                      | −0.3 to AVDD + 0.3             | V    |
| Voltage applied to clock input pins <sup>(2)</sup> |                                      | −0.3 to AVDD + 0.3             | V    |
| T <sub>A</sub>                                     | Operating free-air temperature range | −40 to 85                      | °C   |
| Peak solder temperature                            |                                      | 260                            | °C   |
| Junction temperature                               |                                      | 105                            | °C   |

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.
- (2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is less than |0.3V|. This prevents the ESD protection diodes at the clock input pins from turning on.

## THERMAL INFORMATION

| THERMAL METRIC <sup>(1)</sup> |                                              | ADS61JB23  | UNITS |
|-------------------------------|----------------------------------------------|------------|-------|
|                               |                                              | QFN 40 PIN |       |
| $\theta_{JA}$                 | Junction-to-ambient thermal resistance       | 30.7       | °C/W  |
| $\theta_{JCTop}$              | Junction-to-case (top) thermal resistance    | 17         |       |
| $\theta_{JB}$                 | Junction-to-board thermal resistance         | 5.7        |       |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 0.2        |       |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 5.7        |       |
| $\theta_{JBot}$               | Junction-to-case (bottom) thermal resistance | 1          |       |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## RECOMMENDED OPERATING CONDITIONS

|                                                                                              |                                                          | MIN    | TYP                      | MAX  | UNIT            |
|----------------------------------------------------------------------------------------------|----------------------------------------------------------|--------|--------------------------|------|-----------------|
| <b>SUPPLIES, ANALOG INPUTS AND REFERENCE VOLTAGES</b>                                        |                                                          |        |                          |      |                 |
| Analog supply voltage, AVDD                                                                  |                                                          | 1.7    | 1.8                      | 1.9  | V               |
| Digital supply voltage, DRVDD                                                                |                                                          | 1.7    | 1.8                      | 1.9  | V               |
| CML buffer supply voltage, IOVDD                                                             |                                                          | 1.2    | 1.8                      | 1.9  | V               |
| Analog buffer supply voltage, AVDD_3V                                                        |                                                          | 3.0    | 3.3                      | 3.6  | V               |
| Differential input voltage range                                                             |                                                          |        | 2                        |      | V <sub>PP</sub> |
| Input common-mode voltage                                                                    |                                                          |        | V <sub>CM</sub><br>±0.05 |      | V               |
| VCM (output) – Internal reference mode <sup>(1)</sup>                                        |                                                          |        | 1.95                     |      | V               |
| VCM (input) – External reference mode                                                        |                                                          |        | 1.4                      |      | V               |
| <b>CLOCK INPUT</b>                                                                           |                                                          |        |                          |      |                 |
| Input clock rate in JESD204A single lane mode                                                |                                                          | 15.625 |                          | 80   | MSPS            |
| Input clock rate in JESD204A dual lane mode                                                  |                                                          | 31.25  |                          | 80   | MSPS            |
| Input clock amplitude differential (V <sub>CLKP</sub> - V <sub>CLKM</sub> )                  | Sine wave, ac-coupled                                    | 0.2    | 3.0                      |      | V <sub>PP</sub> |
|                                                                                              | LVPECL, ac-coupled                                       |        | 1.6                      |      | V <sub>PP</sub> |
|                                                                                              | LVDS, ac-coupled                                         |        | 0.7                      |      | V <sub>PP</sub> |
|                                                                                              | CMOS, single-ended, ac-coupled                           |        | 1.5                      |      | V               |
| Input clock duty cycle                                                                       |                                                          | 35%    | 50%                      | 65%  |                 |
| <b>DIGITAL OUTPUTS</b>                                                                       |                                                          |        |                          |      |                 |
| Output data rate in single-lane mode                                                         |                                                          | 312.5  | 20x<br>(sample rate)     | 1600 | MBPS            |
| Output data rate in dual-lane mode                                                           |                                                          | 312.5  | 10x<br>(sample rate)     | 800  | MBPS            |
| C <sub>LOAD</sub>                                                                            | Maximum external load capacitance from each pin to DRGND |        | 5                        |      | pF              |
| R <sub>LOAD</sub>                                                                            | External termination from each output pin to IOVDD       |        | 50                       |      | Ω               |
| T <sub>A</sub>                                                                               | Operating free-air temperature                           | -40    |                          | 85   | °C              |
| <b>HIGH SFDR MODE</b>                                                                        |                                                          |        |                          |      |                 |
| Write register 2h, value 71h to get best HD3 for input frequencies between 150MHz to 250MHz. |                                                          |        |                          |      |                 |

(1) Typical VCM reduces to 1.85V after HIGH SFDR MODE is written.

## ELECTRICAL CHARACTERISTICS

Typical values at 25°C, MIN and MAX values are across the full temperature range  $T_{MIN} = -40^{\circ}\text{C}$  to  $T_{MAX} = 85^{\circ}\text{C}$ ,  $AVDD = 1.8\text{V}$ ,  $AVDD\_3V = 3.3\text{V}$ ,  $DRVDD = 1.8\text{V}$ ,  $IOVDD = 1.8\text{V}$ , Clock frequency = 80MSPS, 50% clock duty cycle, –1dBFS differential analog input, internal reference mode, CML buffer current setting = 16 mA, unless otherwise noted.

| PARAMETER                                                             |                                            | TEST CONDITIONS                           | MIN  | TYP            | MAX       | UNIT                   |
|-----------------------------------------------------------------------|--------------------------------------------|-------------------------------------------|------|----------------|-----------|------------------------|
| <b>REFERENCE VOLTAGES – INTERNAL</b>                                  |                                            |                                           |      |                |           |                        |
| VCM analog input common mode voltage (output)                         |                                            |                                           |      | 1.95           |           | V                      |
| VCM output current (resulting in a VCM change of $\pm 50\text{ mV}$ ) |                                            |                                           |      | 2.5            |           | mA                     |
| <b>REFERENCE VOLTAGES – EXTERNAL</b>                                  |                                            |                                           |      |                |           |                        |
| VCM reference voltage (Input)                                         |                                            |                                           |      | 1.4 $\pm$ 0.1  |           | V                      |
| <b>ANALOG INPUT</b>                                                   |                                            |                                           |      |                |           |                        |
| Differential input voltage range                                      |                                            |                                           |      | 2.0            |           | V <sub>pp</sub>        |
| Differential input capacitance                                        |                                            |                                           |      | 3              |           | pF                     |
| Analog input bandwidth                                                |                                            |                                           |      | 480            |           | MHz                    |
| Analog input common mode range                                        |                                            |                                           |      | VCM $\pm$ 0.05 |           | V                      |
| Analog input common mode current (per input pin)                      |                                            |                                           |      | 1.6            |           | $\mu\text{A}$          |
| <b>DC ACCURACY</b>                                                    |                                            |                                           |      |                |           |                        |
| Offset error                                                          |                                            |                                           | –20  |                | 20        | mV                     |
| Gain error                                                            | Due to internal reference inaccuracy alone |                                           | –2.5 |                | 2.5       | %FS                    |
|                                                                       | Due to channel alone                       |                                           |      | 5              |           | %FS                    |
| Gain error temperature coefficient                                    |                                            |                                           |      | 0.006          |           | mV/ $^{\circ}\text{C}$ |
| AC Power Supply Rejection Ratio, PSRR                                 |                                            | 50 mV <sub>PP</sub> signal on AVDD supply |      | >30            |           | dB                     |
| <b>POWERDOWN MODES</b>                                                |                                            |                                           |      |                |           |                        |
| Complete powerdown mode                                               |                                            |                                           |      | 10             |           | mW                     |
| Fast recovery powerdown mode                                          |                                            |                                           |      | 210            |           | mW                     |
| Power with no clock                                                   |                                            |                                           |      | 115            |           | mW                     |
| DNL differential nonlinearity                                         |                                            |                                           | –0.7 | $\pm$ 0.3      | 0.8       | LSB                    |
| INL integral nonlinearity                                             |                                            |                                           |      | $\pm$ 0.7      | $\pm$ 1.5 | LSB                    |
| <b>POWER SUPPLY CURRENTS</b>                                          |                                            |                                           |      |                |           |                        |
| AVDD current                                                          |                                            |                                           |      | 105            | 122       | mA                     |
| AVDD_3V current                                                       |                                            |                                           |      | 40             | 51        | mA                     |
| DRVDD current                                                         |                                            |                                           |      | 50             | 61        | mA                     |
| IOVDD current                                                         |                                            |                                           |      | 16             | 21        | mA                     |
| Total power                                                           |                                            |                                           |      | 440            | 500       | mW                     |
| <b>DYNAMIC PERFORMANCE<sup>(1)</sup></b>                              |                                            |                                           |      |                |           |                        |
| SFDR                                                                  | IF = 10 MHz                                |                                           |      | 80             |           | dBc                    |
|                                                                       | IF = 185 MHz                               |                                           | 70   | 80             |           | dBc                    |
| SNR                                                                   | IF = 10 MHz                                |                                           |      | 71.7           |           | dBFS                   |
|                                                                       | IF = 185 MHz                               |                                           | 68   | 70.5           |           | dBFS                   |
| SINAD                                                                 | IF = 10 MHz                                |                                           |      | 71.2           |           | dBFS                   |
|                                                                       | IF = 185 MHz                               |                                           |      | 70.1           |           | dBFS                   |
| HD3                                                                   | IF = 10 MHz                                |                                           |      | 80             |           | dBc                    |
|                                                                       | IF = 185 MHz                               |                                           | 70   | 80             |           | dBc                    |
| HD2                                                                   | IF = 10 MHz                                |                                           |      | 100            |           | dBc                    |
|                                                                       | IF = 185 MHz                               |                                           | 70   | 80             |           | dBc                    |
| Worst spur (excluding HD2, HD3)                                       | IF = 10 MHz                                |                                           |      | 90             |           | dBc                    |
|                                                                       | IF = 185 MHz                               |                                           | 81   | 87             |           | dBc                    |

(1) HIGH SFDR MODE is enabled.

## DIGITAL CHARACTERISTICS

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1

| PARAMETER                                                     | TEST CONDITIONS                                                       | MIN       | TYP       | MAX  | UNIT  |
|---------------------------------------------------------------|-----------------------------------------------------------------------|-----------|-----------|------|-------|
| DIGITAL INPUTS                                                |                                                                       |           |           |      |       |
| High-level input voltage                                      |                                                                       | 1.2       |           |      | V     |
| Low-level input voltage                                       |                                                                       |           |           | 0.6  | V     |
| High-level input current                                      | SEN                                                                   |           | 0         |      | μA    |
|                                                               | SCLK, SDATA, RESET, PDN, PDN_ANA                                      |           | 10        |      |       |
| Low-level input current                                       | SEN                                                                   |           | 10        |      | μA    |
|                                                               | SCLK, SDATA, RESET, PDN, PDN_ANA                                      |           | 0         |      |       |
| DIGITAL OUTPUTS (SDOUT)                                       |                                                                       |           |           |      |       |
| High-level output voltage                                     |                                                                       | DRVDD-0.1 | DRVDD     |      | V     |
| Low-level output voltage                                      |                                                                       |           | 0         | 0.1  | V     |
| CML OUTPUTS – 50 Ω SINGLE-ENDED EXTERNAL TERMINATION TO IOVDD |                                                                       |           |           |      |       |
| IOVDD supply range                                            |                                                                       | 1.2       | 1.8       | 1.9  | V     |
| High-level output voltage                                     |                                                                       |           | IOVDD     |      | V     |
| Low-level output voltage                                      |                                                                       |           | IOVDD-0.4 |      | V     |
| Output differential voltage,  VOD                             |                                                                       |           | 0.4       |      | V     |
| Output common-mode voltage, V <sub>OCM</sub>                  |                                                                       |           | IOVDD-0.2 |      | V     |
| Transmitter short circuit current                             | Transmitter terminals shorted to any voltage between –0.25V and 1.45V | -90       |           | 50   | mA    |
| Single-ended output impedance                                 |                                                                       |           | 50        |      | Ω     |
| Unit interval, UI                                             |                                                                       | 625       |           | 3200 | UI    |
| Total Jitter, T <sub>J</sub>                                  |                                                                       |           | 0.35      |      | p-pUI |
| Rise/ fall times                                              | 5 pF single-ended load capacitance to ground                          |           | 175       |      | ps    |

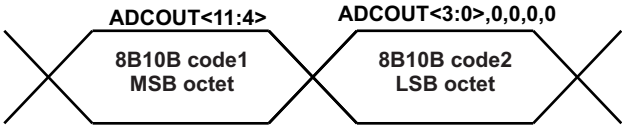
## WAKE-UP TIMING CHARACTERISTICS

| PARAMETER    | TEST CONDITIONS                                                     | MIN | TYP | MAX | UNIT    |
|--------------|---------------------------------------------------------------------|-----|-----|-----|---------|
| Wake-up time | Time to valid data after coming out of COMPLETE POWERDOWN mode      |     | 50  |     | $\mu$ s |
|              | Time to valid data after coming out of FAST RECOVERY POWERDOWN mode |     | 50  |     | $\mu$ s |
|              | Time to valid data after coming out of SOFTWARE POWERDOWN mode      |     | 10  |     | $\mu$ s |
|              | Time to valid data after stopping and restarting the input clock    |     | 5   |     | $\mu$ s |

**DETAILED DESCRIPTION**

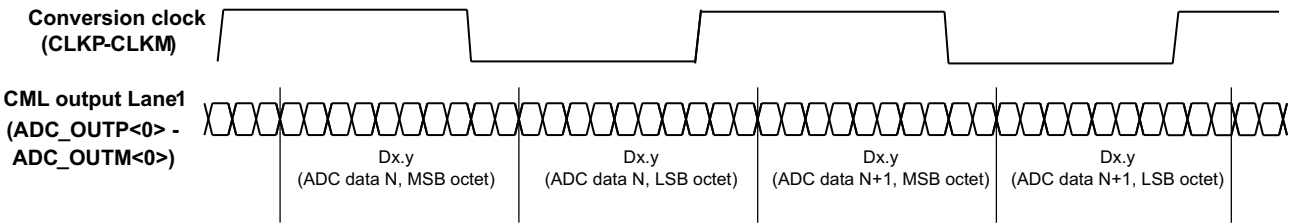
**JESD204A OUTPUT INTERFACE**

The 12-bit ADC output is padded with 4 zeros on the LSB side to form a 16-bit output. Two 8B10B codes are formed – one from the 8 MSBs and the other from the 6 LSBs and the 2 padded zeros .

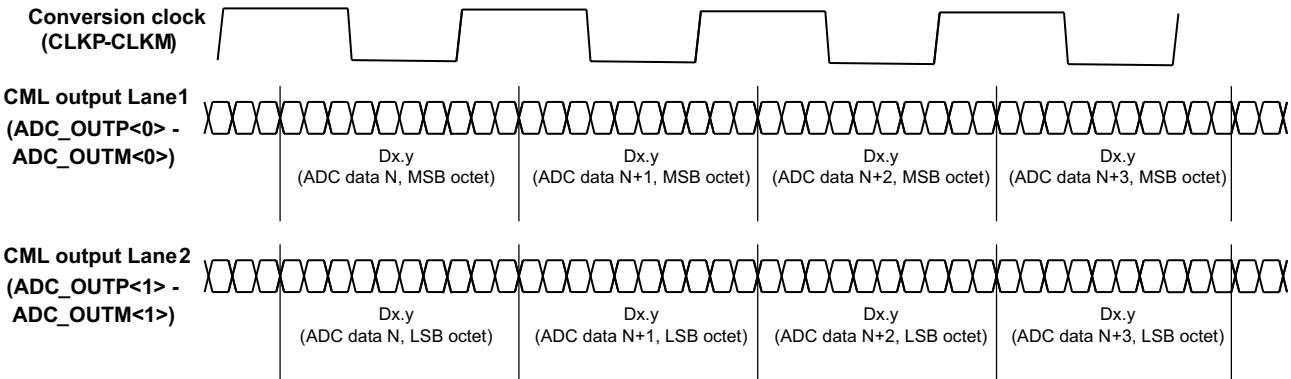


**Figure 1. Mapping of ADC Output to Two 8B10B Codes**

The two octets can be either transmitted on the same lane (single lane interface) or on two lanes (dual lane interface). By default, the device operates in single lane interface.



**Figure 2. Single Lane Timing**



**Figure 3. Dual Lane Timing**

The detailed timing diagram in the dual lane mode is shown below:

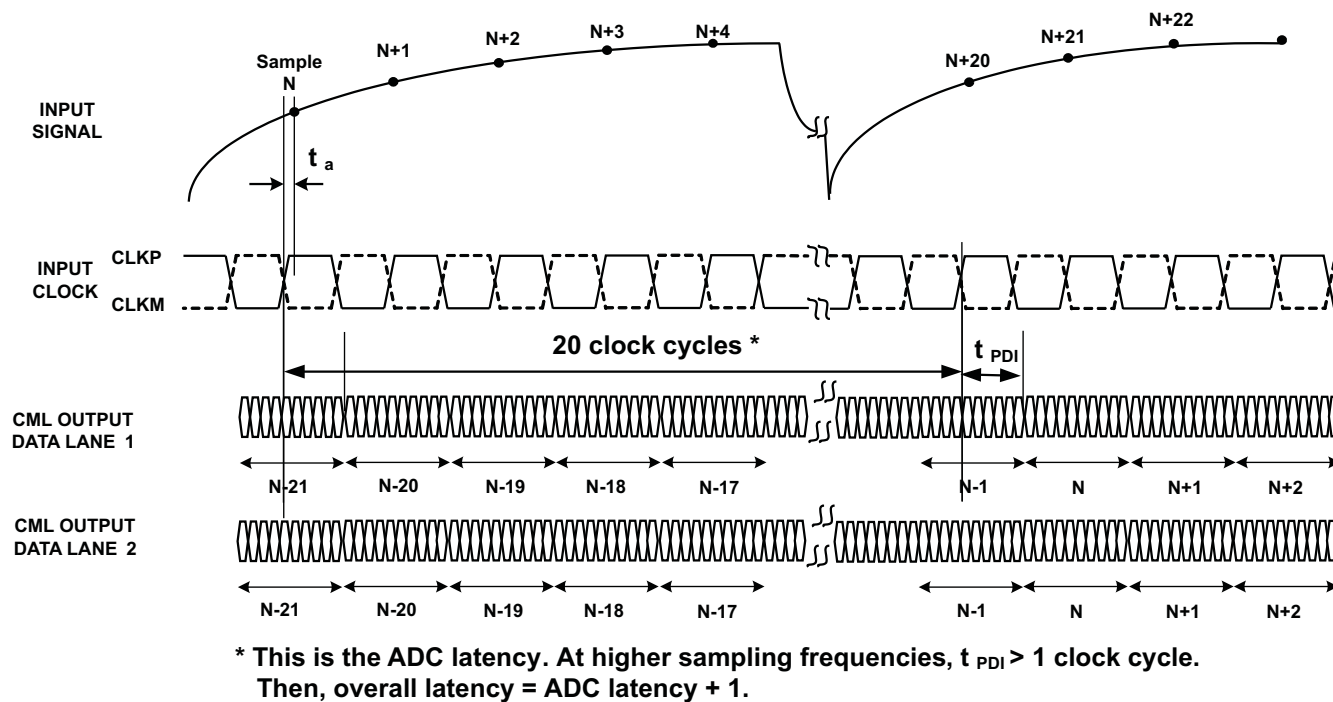
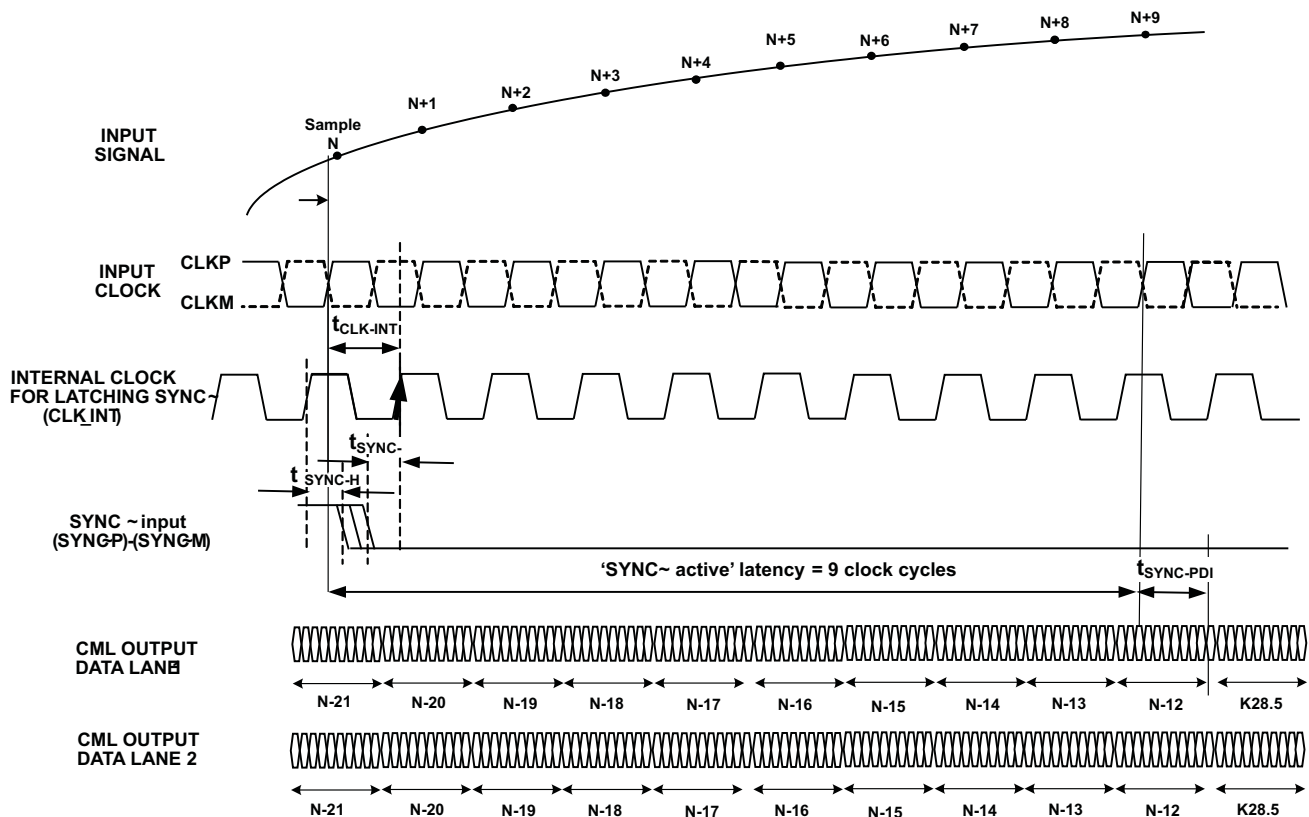


Figure 4. Data Timing Diagram - Dual Lane Mode

| PARAMETER                        | 30 MSPS   | 40 MSPS   | 60 MSPS   | 80 MSPS   |
|----------------------------------|-----------|-----------|-----------|-----------|
| Aperture delay – $T_A$           | 560 ps    | 560 ps    | 560 ps    | 560 ps    |
| Aperture jitter (RMS) – $T_J$    | 125 fs    | 125 fs    | 125 fs    | 125 fs    |
| Latency                          | 20 clocks | 20 clocks | 20 clocks | 20 clocks |
| $t_{PDI}$ Data propagation delay | 33.3 ns   | 26.2 ns   | 18.9 ns   | 15.3 ns   |

Whenever there is a need to synchronize to the frame boundary of the output data stream, the receiver issues a synchronization request through the SYNC~P, SYNC~M pins. Below diagram shows how the transmission switches from normal data (D) to code group synchronization symbols K28.5 symbols during and after a synchronization request.



**Figure 5. SYNC~ ACTIVE Timing Diagram**

**Table 1. SYNC~ Falling Edge Timing at 80 MSPS**

| PARAMETER             |                              | DESCRIPTION                                                                                                               | TYP  | UNIT   |
|-----------------------|------------------------------|---------------------------------------------------------------------------------------------------------------------------|------|--------|
| $t_{\text{CLK-INT}}$  |                              | Delay from input clock rising edge to the rising edge of the internal clock (CLK_INT) used to latch falling edge of SYNC~ | 10.5 | ns     |
| $t_{\text{SYNC-SU}}$  | SYNC~ active edge setup time | Minimum delay required from SYNC~ falling edge to CLK_INT rising edge                                                     | 2    | ns     |
| $t_{\text{SYNC-H}}$   | SYNC~ active edge hold time  | Minimum delay required from CLK_INT rising edge to SYNC~ falling edge                                                     | 2    | ns     |
|                       | SYNC~ active latency         | Number of clocks for K28.5 to appear at the output after a SYNC~ request                                                  | 9    | clocks |
| $t_{\text{SYNC-PDI}}$ | SYNC~ data propagation delay | Similar to data propagation delay                                                                                         | 15.3 | ns     |

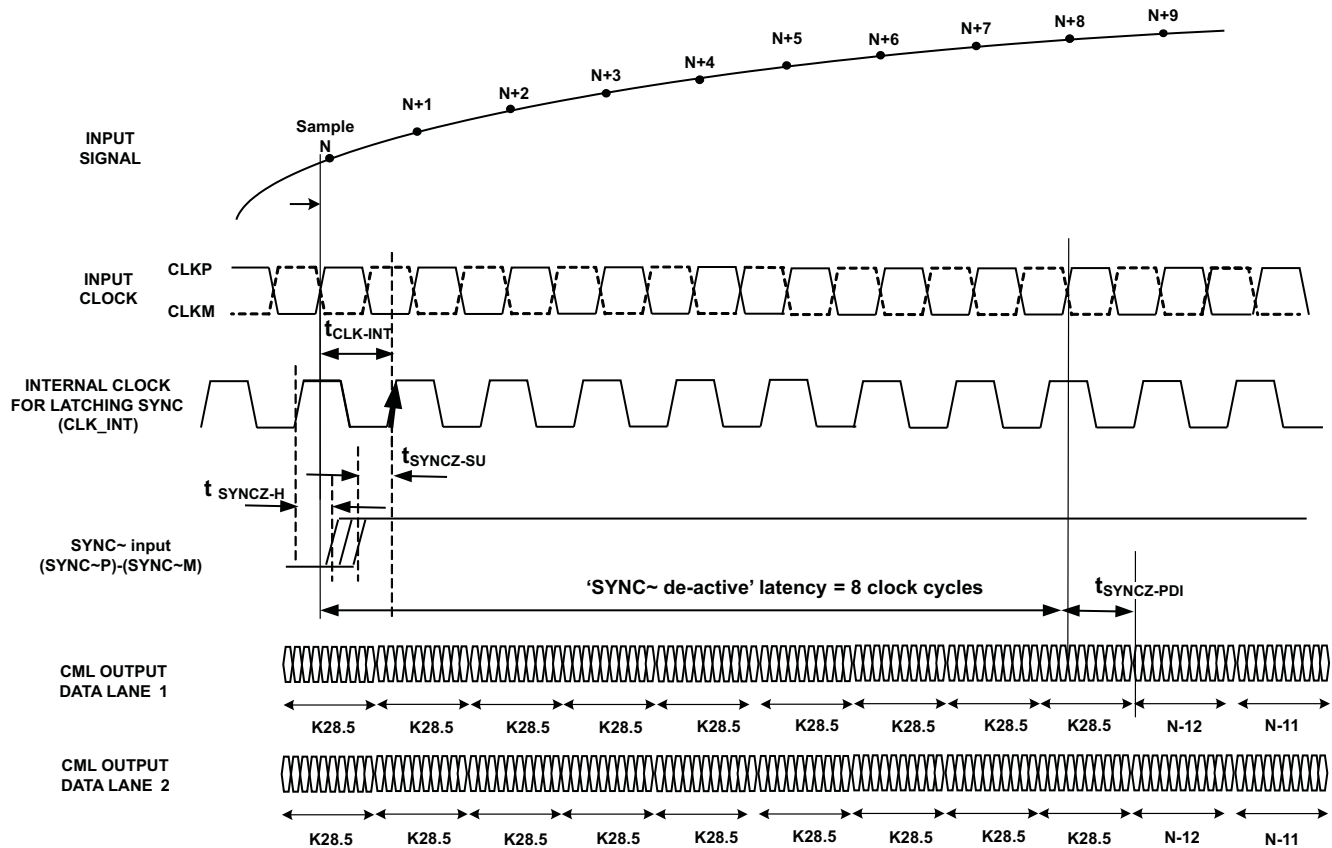


Figure 6. SYNC~ DE-ACTIVE Timing Diagram

Table 2. SYNC~ Rising Edge Timing at 80 MSPS

| PARAMETER                                                     | DESCRIPTION                                                                                                              | TYP  | UNIT   |
|---------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------|------|--------|
| $t_{\text{CLK-INT}}$                                          | Delay from input clock rising edge to the rising edge of the internal clock (CLK_INT) used to latch rising edge of SYNC~ | 10.5 | ns     |
| $t_{\text{SYNCZ-SU}}$ SYNC~ active edge setup time            | Minimum delay required from SYNC~ rising edge to CLK_INT rising edge                                                     | 2    | ns     |
| $t_{\text{SYNCZ-H}}$ SYNC~ active edge hold time              | Minimum delay required from CLK_INT rising edge to SYNC~ rising edge                                                     | 2    | ns     |
| SYNC~ de-active latency                                       | Number of clocks for normal data to appear at the output after a SYNC~ de-activate request                               | 8    | clocks |
| $t_{\text{SYNCZ-PDI}}$ SYNC~ de-active data propagation delay | Similar to data propagation delay                                                                                        | 15.3 | ns     |

## 4-LEVEL CONTROL

In the ADS61JB23 the DFS\_EXTREF and MODE pins function as 4-level control pins as described in [Table 3](#) and [Table 4](#). A simple scheme to generate 4-level voltage is shown in [Figure 7](#).

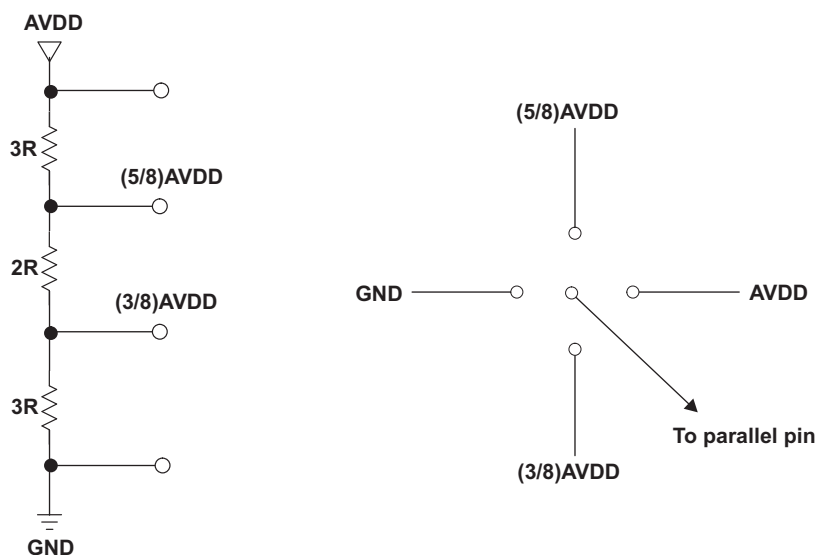


Figure 7. Simple Scheme to Configure 4-Level Control Pins

Table 3. Pin 3 – DFS\_EXTREF

| DFS_EXTREF            | DESCRIPTION         |
|-----------------------|---------------------|
| 0<br>+150 mV/–0 mV    | EXTREF = 0, DFS = 0 |
| (3/8)AVDD<br>±150 mV  | EXTREF = 1, DFS = 0 |
| (5/8)AVDD<br>±150 mV  | EXTREF = 1, DFS = 1 |
| AVDD<br>+0 mV/–150 mV | EXTREF = 0, DFS = 1 |

**Key:**

**EXTREF:** 0 = Internal reference mode, 1 = External reference mode.

**DFS:** 0 = 2's complement output, 1 = Offset binary output.

## PARALLEL INTERFACE MODE

The ADS61JB23 operates in parallel interface mode when a suitable voltage is applied on the MODE pin as described in [Table 4](#). In parallel interface mode, the SEN, SDATA, SCLK, and SDOUT pins function differently compared to serial interface mode. In this mode, the SEN\_FALIGN\_IDLE and SCLK\_SERF0\_SCR pins turn into 4-level control pins for JESD interface as described in [Table 5](#) and [Table 6](#), whereas the SDATA\_TEST0 and SDOUT\_TEST1 pins turn into 2-level control pins as described in [Table 7](#).

**Table 4. Pin 19 - Mode**

| MODE                  | DESCRIPTION                                                                                                                                                                                                                 |
|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0<br>+150 mV/-0 mV    | Serial interface mode. Pins 23, 24 and 25 are configured as SEN, SDATA, SCLK. Pins 36, 37, 38, 39 are configured to output either early signal estimate or signal power estimate – selection is based on register settings. |
| (3/8)AVDD<br>±150 mV  | Do not use                                                                                                                                                                                                                  |
| (5/8)AVDD<br>±150 mV  | Parallel interface mode. Pins 23, 24 and 25 are configured as parallel input pins for controlling JESD204A modes. Pins 36,37,38, 39 outputs early signal estimate always.                                                   |
| AVDD<br>+0 mV/-150 mV | Do not use.                                                                                                                                                                                                                 |

**Table 5. Pin 23 - SEN\_FALIGN\_IDLE (in Parallel Interface Mode)**

| SEN_FALIGN_IDLE       | DESCRIPTION          |
|-----------------------|----------------------|
| 0<br>+150 mV/-0 mV    | FALIGN = 0, IDLE = 0 |
| (3/8)AVDD<br>±150 mV  | FALIGN = 1, IDLE = 0 |
| (5/8)AVDD<br>±150 mV  | FALIGN = 1, IDLE = 1 |
| AVDD<br>+0 mV/-150 mV | FALIGN = 0, IDLE = 1 |

**Key:**

**FALIGN:** When the last octet of the current frame is the same as the last octet of the previous frame, then FALIGN determines whether the last octet of the current frame is transmitted as is, or replaced by a K28.7 control symbol. When FALIGN=0, it is transmitted as is. When FALIGN=1, it is replaced with a K28.7 control symbol.

**IDLE:** IDLE determines the synchronization characters transmitted during and immediately after a SYNC event. When IDLE=0, the device transmits K28.5 as per the JESD204A spec. When IDLE=1, the device alternately transmits K28.5 and D5.6/D16.2 characters as per IEEE Std 802.3-2002 part3, Clause 36.2.4.12. This is the case in both single and dual lane modes.

**Table 6. Pin 25 - SCLK\_SERF0\_SCR (in Parallel Interface Mode)**

| SCLK_SERF0_SCR        | DESCRIPTION        |
|-----------------------|--------------------|
| 0<br>+150 mV/-0 mV    | SERF0 = 0, SCR = 0 |
| (3/8)AVDD<br>±150 mV  | SERF0 = 1, SCR = 0 |
| (5/8)AVDD<br>±150 mV  | SERF0 = 1, SCR = 1 |
| AVDD<br>+0 mV/-150 mV | SERF0 = 0, SCR = 1 |

**Key:**

**SERF0:** Output serialization factor. When SERF0=0, the device transmits 2 octets per frame (entire ADC channel in a single lane) with an output serialization factor of 20. When SERF0=1, the device transmits 1 octet per frame (ADC channel over 2 lanes) with an output serialization factor of 10.

**SCR:** SCR=0: Scrambling disabled. SCR=1: Scrambling (as per JESD204A) enabled

**Table 7. Pins 24 and 28 - SDATA\_TEST0 and SDOUT\_TEST1 (in Parallel Interface Mode)**

| TEST1 | TEST0 | MODE                                                                                                                             |
|-------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 0     | 0     | Normal mode. Input to JESD204A encoder is ADC data                                                                               |
| 0     | 1     | Input to JESD204A encoder is B5B5. Output is a stream of D21.5 (alternating 1 and 0)                                             |
| 1     | 0     | Input to JESD204A encoder is FF00                                                                                                |
| 1     | 1     | Input to JESD204A encoder is a pseudo random pattern $1 + X^{14} + X^{15}$ (irrespective of whether scrambler is enabled or not) |

## SERIAL INTERFACE

The ADC has a set of internal registers, which can be accessed by the serial interface formed by pins Serial interface Enable (SEN), Serial Interface Clock (SCLK) and Serial Interface Data (SDATA).

Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every falling edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 16<sup>th</sup> SCLK falling edge when SEN is low. In case the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiple of 16-bit words within a single active SEN pulse.

The first 8 bits form the register address and the remaining 8 bits are the register data. The interface can work with SCLK frequency from 20 MHz down to very low speeds (few Hertz) and also with non-50% SCLK duty cycle.

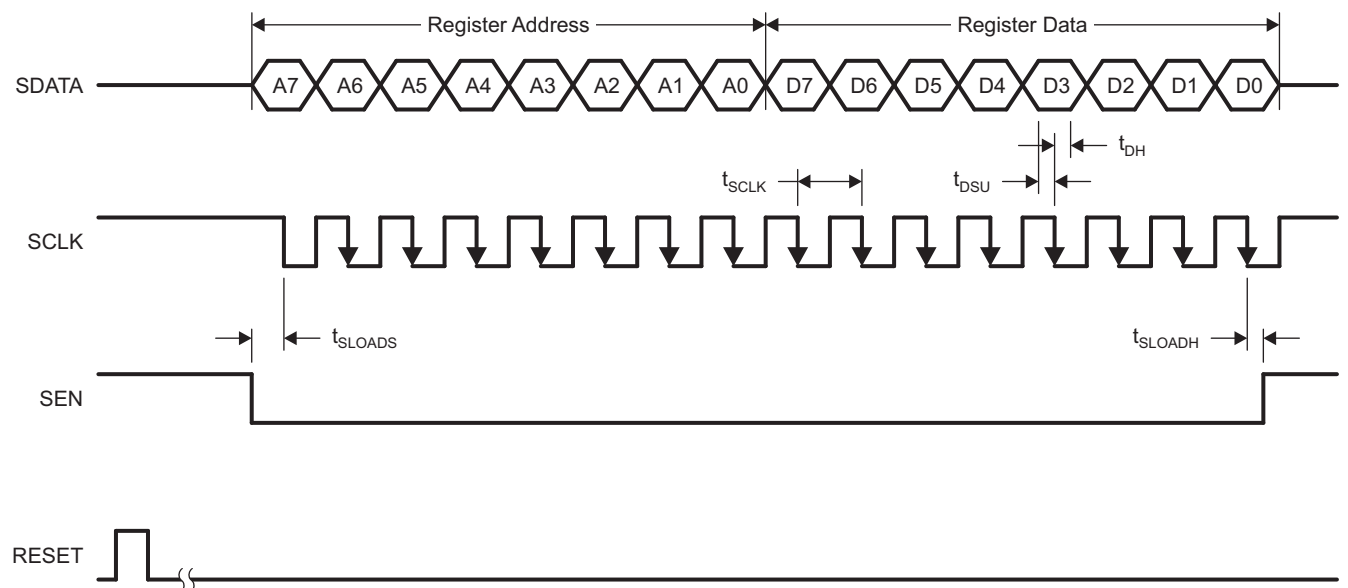
## REGISTER INITIALIZATION

After power-up, the internal registers MUST be initialized to their default values. This can be done in one of two ways:

1. Either through hardware reset by applying a high-going pulse on RESET pin (of width greater than 10ns) as shown in [Figure 8](#)

OR

2. By applying software reset. Using the serial interface, set the S\_RESET bit (D1 in register 0x00) to HIGH. This initializes internal registers to their default values and then self-resets the S\_RESET bit to LOW. In this case the RESET pin is kept LOW.



T0109-04

**Figure 8. Serial Interface Timing**

## SERIAL INTERFACE TIMING CHARACTERISTICS

Typical values at 25°C, MIN and MAX values across the full temperature range  $T_{MIN} = -40^{\circ}\text{C}$  to  $T_{MAX} = 85^{\circ}\text{C}$ , AVDD = 1.8V, DRVDD = 1.8V, unless otherwise noted.

| PARAMETER    |                                   | MIN  | TYP | MAX | UNIT |
|--------------|-----------------------------------|------|-----|-----|------|
| $f_{SCLK}$   | SCLK frequency ( $= 1/t_{SCLK}$ ) | > DC |     | 20  | MHz  |
| $t_{SLOADS}$ | SEN to SCLK setup time            | 25   |     |     | ns   |
| $t_{SLOADH}$ | SCLK to SEN hold time             | 25   |     |     | ns   |
| $t_{DS}$     | SDATA setup time                  | 25   |     |     | ns   |
| $t_{DH}$     | SDATA hold time                   | 25   |     |     | ns   |

### Serial Register Readout

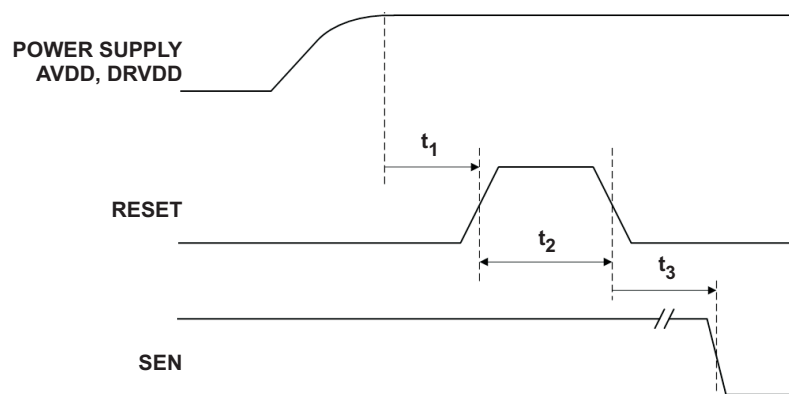
The device includes an option where the contents of the internal registers can be read back. This may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

1. First, set register bit <SERIAL READOUT> = 1. This also disables any further writes into the registers (EXCEPT register bit <SERIAL READOUT> itself).
2. Initiate a serial interface cycle specifying the address of the register (A7-A0) whose content has to be read.
3. The device outputs the contents (D7-D0) of the selected register on SDOUT\_TEST1 pin.
4. The external controller can latch the contents at the falling edge of SCLK.
5. To enable register writes, reset register bit <SERIAL READOUT> = 0.

### RESET TIMING

Typical values at 25°C, MIN and MAX values across the full temperature range  $T_{MIN} = -40^{\circ}\text{C}$  to  $T_{MAX} = 85^{\circ}\text{C}$ , unless otherwise noted.

| PARAMETER | CONDITIONS                             | MIN | TYP | MAX | UNIT |
|-----------|----------------------------------------|-----|-----|-----|------|
| $t_1$     | Power-on delay                         |     | 1   |     | ms   |
| $t_2$     | Reset pulse width                      | 10  |     |     |      |
| $t_3$     | Delay from RESET disable to SEN active | 100 |     |     | ns   |



NOTE: A high-going pulse on RESET pin is required in case of initialization through hardware reset.

**Figure 9. Reset Timing Diagram**

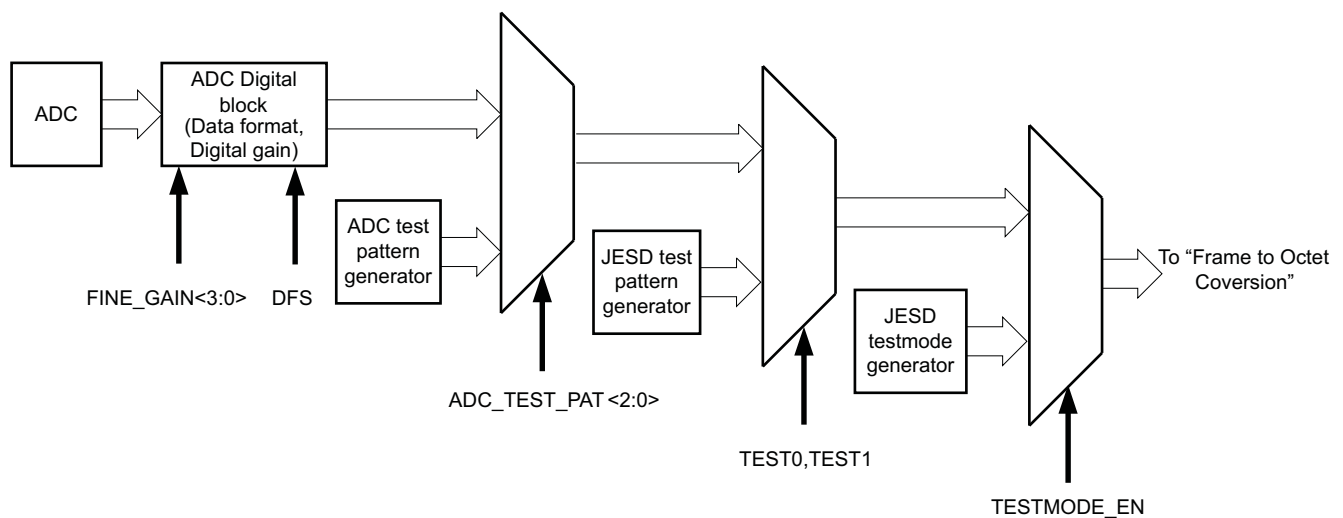
**SERIAL INTERFACE REGISTER MAP**

| MODE              | BIT LOCATION<br>(Address in Hex<br><Bit location>) | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------------------|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| S_RESET           | 00<1>                                              | Software RESET. Same function as hardware reset.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| SERIAL_READOUT    | 00<0>                                              | Default = 0 for serial interface write. 1 for serial readout.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| HIGH_SFDR_MODE    | 2<6:4> and 2<0>                                    | Set these bits to get best HD3 when input frequency is between 150MHz to 250MHz.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| DFS_OVERRIDE      | 3C<7>                                              | Override control of DFS_EXTREF pin in controlling DFS select mode, and control it using register bit DFS_REG.<br>When '0', DFS functionality determined by DFS_EXTREF pin.<br>When '1', DFS functionality determined by DFS_REG.                                                                                                                                                                                                                                                                                                                                                                                                                        |
| DFS_REG           | 3C<6>                                              | Register bit for DFS control.<br>When '0', output format is 2's complement.<br>When '1', output format is offset binary.Takes effect when DFS_OVERRIDE is set to '1'.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| INT_REF_OVERRIDE  | 44<3>                                              | Override control of DFS_EXTREF pin in controlling Internal/ External reference select mode, and control it using register bit INT_REF_REG.<br>When '0', Internal/ External reference mode determined by DFS_EXTREF pin.<br>When '1', Internal/ External reference mode determined by INT_REF_REG.                                                                                                                                                                                                                                                                                                                                                       |
| INT_REF_REG       | 44<2>                                              | Register bit for Internal/ External reference mode control.<br>When '0', Internal reference mode.<br>When '1', External reference mode.Takes effect when INT_REF_OVERRIDE is set to '1'.                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| S_PDN             | 44<6>                                              | Software powerdown.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| FINE_GAIN<3:0>    | 45<7:4>                                            | 0-6 dB digital gain in steps of 0.5 dB. Default is 0 dB. Refer section titled "FINE GAIN CONTROL"                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| BYPASS_FINE_GAIN  | 45<3>                                              | Digital gain bypass. When set to 1, fine gain is bypassed.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| ADC_TEST_PAT<2:0> | 45<2:0>                                            | Output Test patterns:<br>000: ADC output data bus is input to JESD204A encoder block<br>001: ADC bus replaced by min code (00000000000000 in offset binary).<br>010: ADC bus replaced by max code (11111111111111 in offset binary).<br>100: ADC bus replaced by a ramping code pattern that increments by 1 LSB every 4 clocks (and folds back to min code once max code is reached).<br>011,101,110,111: Do not use                                                                                                                                                                                                                                   |
| TXMIT_LINKDATA_EN | A0<0>                                              | When set to 1, initial lane alignment sequence (as per JESD204A) is sent after Code group sync in both single lane and dual lane interfaces. When this bit is 0 (default) initial lane alignment sequence is not transmitted.                                                                                                                                                                                                                                                                                                                                                                                                                           |
| S_FALIGN          | A0<1>                                              | Software Frame Align control.<br>Enables frame alignment monitoring. When this bit is set to 1 (with scrambling turned off) – If the last octet in the previous frame is the same as the last octet in the current frame, then the last octet in the current frame will be replaced with a frame alignment symbol K28.7. When this bit is 0, there is no replacement.<br>When scrambling is ON and this bit is '1': When the last scrambled octet in a frame equals 0xFC, it is encoded as K28.7.<br>This bit control is similar to the FALIGN pin control.                                                                                             |
| MFALIGN           | A0<2>                                              | Multi-frame Align control.<br>Similar to frame align, this refers to multi-frame.<br>Multi-frame alignment symbol is K28.3.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| FLIP_ADC_BUS      | A0<3>                                              | By default, the last octet in the frame gets derived from the data octet on the LSB side. Since usually the LSB octets switch more (frame to frame) than the MSB octets, the occurrence of consecutive "last octets" might be rare. This might lead to infrequent occurrence of frame alignment symbols. To increase the rate of consecutive last octets (and thereby the rate of frame and multi-frame alignment symbols), this bit can be set to 1. Setting this bit to 1 will flip the bit order of the ADC inputs (N bits) to the JESD204A logic. Note that the 2 zeros padded at the end to make the input to the JESD204A logic remain unchanged. |
| TESTMODE_EN       | A0<4>                                              | Enables the transmission of test sequence mentioned in the JESD204A document.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| S_IDLE            | A0<5>                                              | Software idle generation control.<br>Normally the output during code group synchronization is K28.5. When idle_sync is set to 1, it is a K28.5 comma followed by either a D5.6 or a D16.2. This is as per IEEE Std 802.3-2002 part3, Clause 36.2.4.12 and enables compatibility with TI's TLK family of devices.This bit control is similar to the IDLE pin control.                                                                                                                                                                                                                                                                                    |
| S_TEST0           | A0<6>                                              | These 2 bit controls are similar to the TEST1 and TEST0 pin controls.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| S_TEST1           | A0<7>                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| CTRL_F            | A1<0>                                              | Enables write into A6<7:0>.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| CTRL_K            | A1<1>                                              | Enables write into A7<4:0>.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| S_SCR             | A5<7>                                              | Software Scrambling enable. This bit control is similar to the SCR pin control.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

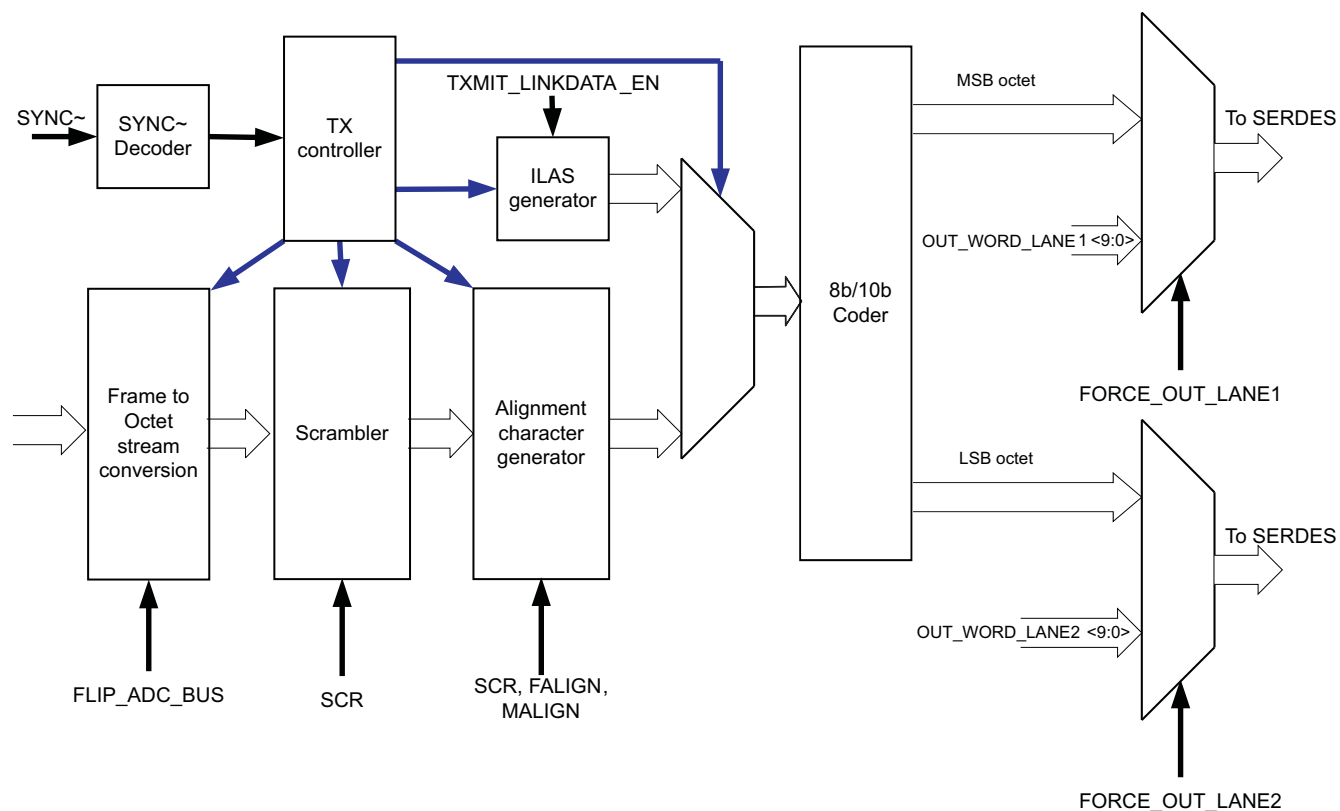
| MODE                 | BIT LOCATION<br>(Address in Hex<br><Bit location>) | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|----------------------|----------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| F<7:0>               | A6<7:0>                                            | Number of octets per frame. Default set to 00000001 (2-1) which is 2 octets per frame (single lane). For 2-lane output (1 octet per frame), set to 00000000. Note that to override default, CTRL_F needs to be set to 1.                                                                                                                                                                                                                                                                   |
| K<4:0>               | A7<4:0>                                            | Number of frames per multiframe (minus 1). Default depends on value of F<7:0>.<br>When F=0 (10X mode): K=16 (17 frames per multiframe)<br>When F=1 (20X mode): K=8 (9 frames per multiframe)<br>Note that to override the default value of K<4:0>, CTRL_K needs to be set to 1. When CTRL_K is set to 1, the value programmed in A7<4:0> denotes the number of frames per multiframe (minus 1). For eg., to set the number of frames per multiframe to 23, set CTRL_K=1 and A7<4:0>=10110. |
| CML_I<3:0>           | B0<3:0>                                            | CML buffer current select. Default (0000) is 16 mA.<br>Current is calculated as: 16 mA+16 mA×<3>–8 m×<2>–4 mA×<1>–2 mA×<0>                                                                                                                                                                                                                                                                                                                                                                 |
| FORCE_OUT_LANE1      | B4<3>                                              | Replaces the output of the 8b/10b coder (corresponding to the MSB octet) with a 10-bit word specified in OUT_WORD_LANE1<9:0>                                                                                                                                                                                                                                                                                                                                                               |
| OUT_WORD_LANE1<9:0>  | B6<7:0>,<br>B7<7:6>                                | 10-bit word replacing the output of the 8b/10b coder when FORCE_OUT_LANE1 is set to '1'                                                                                                                                                                                                                                                                                                                                                                                                    |
| FORCE_OUT_LANE2      | B4<6>                                              | Replaces the output of the 8b/10b coder (corresponding to the LSB octet) with a 10-bit word specified in OUT_WORD_LANE2<9:0>                                                                                                                                                                                                                                                                                                                                                               |
| OUT_WORD_LANE2<9:0>  | B8<7:4>,<br>B9<7:2>                                | 10-bit word replacing the output of the 8b/10b coder when FORCE_OUT_LANE2 is set to '1'                                                                                                                                                                                                                                                                                                                                                                                                    |
| EN_SIG_EST           | D6<0>                                              | Outputs a 4-bit ADC code with low latency on pins DETECT<3:0>                                                                                                                                                                                                                                                                                                                                                                                                                              |
| EN_PWR_EST           | D6<5>                                              | Outputs a 4-bit average power estimate of input signal on DETECT<3:0>.<br>Power estimate is in dB scale in steps of roughly 1 dB. Refer section titled SIGNAL POWER ESTIMATION                                                                                                                                                                                                                                                                                                             |
| SAMPLES_PWR_EST<2:0> | D6<4:2>                                            | Determines number of samples to average for power estimation.<br>Programmable from 1K to 16K.                                                                                                                                                                                                                                                                                                                                                                                              |

## REGISTER MODES

A brief summary of different register modes and their location in the digital processing flow of the ADS61JB23 is shown in [Figure 10](#) and [Figure 11](#).



**Figure 10. Register Modes Preceding Frame to Octet Conversion Block**



**Figure 11. Register Modes Following Frame to Octet Conversion Block**

## INITIAL LANE ALIGNMENT SEQUENCE

By default the initial lane alignment sequence is not transmitted. To enable transmission of the initial lane alignment sequence,

For the two settings of F, the Mapping of link configuration fields to octets Table of the JESD204A spec is shown in [Table 8](#).

**Table 8. Mapping of Link Configuration Fields to Octets**

| Configuration Octet No. | MSB                      | 6 | 5 | 4                                                             | 3               | 2 | 1 | LSB |
|-------------------------|--------------------------|---|---|---------------------------------------------------------------|-----------------|---|---|-----|
| F=1 (20X mode)          |                          |   |   |                                                               |                 |   |   |     |
| 0                       | DID<7:0> = 00000000      |   |   |                                                               |                 |   |   |     |
| 1                       | X                        | X | X | X                                                             | BID<3:0> = 0000 |   |   |     |
| 2                       | X                        | X | X | LID<4:0> = 00000                                              |                 |   |   |     |
| 3                       | SCR<0> - set by S_SCR    | X | X | L<4:0> = 00000                                                |                 |   |   |     |
| 4                       | F<7:0> = 00000001        |   |   |                                                               |                 |   |   |     |
| 5                       | X                        | X | X | K<4:0> = 01000 (or programmed value of A7<4:0> if CTRL_K = 1) |                 |   |   |     |
| 6                       | M<7:0> = 00000000        |   |   |                                                               |                 |   |   |     |
| 7                       | CS<1:0>=00               |   | X | N<4:0> = 01101                                                |                 |   |   |     |
| 8                       | X                        | X | X | N'<4:0> = 01111                                               |                 |   |   |     |
| 9                       | X                        | X | X | S<4:0>=00000                                                  |                 |   |   |     |
| 10                      | HD<0>=0                  | X | X | CF<4:0>=00000                                                 |                 |   |   |     |
| 11                      | RES1<7:0> - Set to all 0 |   |   |                                                               |                 |   |   |     |
| 12                      | RES2<7:0> - Set to all 0 |   |   |                                                               |                 |   |   |     |
| 13                      | FCHK<7:0>                |   |   |                                                               |                 |   |   |     |
| F=0 (10X mode)          |                          |   |   |                                                               |                 |   |   |     |
| 0                       | DID<7:0> = 00000000      |   |   |                                                               |                 |   |   |     |
| 1                       | X                        | X | X | X                                                             | BID<3:0> = 0000 |   |   |     |
| 2                       | X                        | X | X | LID<4:0> = 00000 for Lane 1 and 00001 for Lane 2              |                 |   |   |     |
| 3                       | SCR<0> - set by S_SCR    | X | X | L<4:0> = 00001                                                |                 |   |   |     |
| 4                       | F<7:0> = 00000000        |   |   |                                                               |                 |   |   |     |
| 5                       | X                        | X | X | K<4:0> = 10000 (or programmed value of A7<4:0> if CTRL_K = 1) |                 |   |   |     |
| 6                       | M<7:0> = 00000000        |   |   |                                                               |                 |   |   |     |
| 7                       | CS<1:0>=00               |   | X | N<4:0> = 01101                                                |                 |   |   |     |
| 8                       | X                        | X | X | N'<4:0> = 01111                                               |                 |   |   |     |
| 9                       | X                        | X | X | S<4:0>=00000                                                  |                 |   |   |     |
| 10                      | HD<0>=0                  | X | X | CF<4:0>=00000                                                 |                 |   |   |     |
| 11                      | RES1<7:0> - Set to all 0 |   |   |                                                               |                 |   |   |     |
| 12                      | RES2<7:0> - Set to all 0 |   |   |                                                               |                 |   |   |     |
| 13                      | FCHK<7:0>                |   |   |                                                               |                 |   |   |     |

## TYPICAL CHARACTERISTICS

At +25°C, AVDD = 1.8V, AVDD\_3V = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, -1dBFS differential analog input, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0dB gain mode

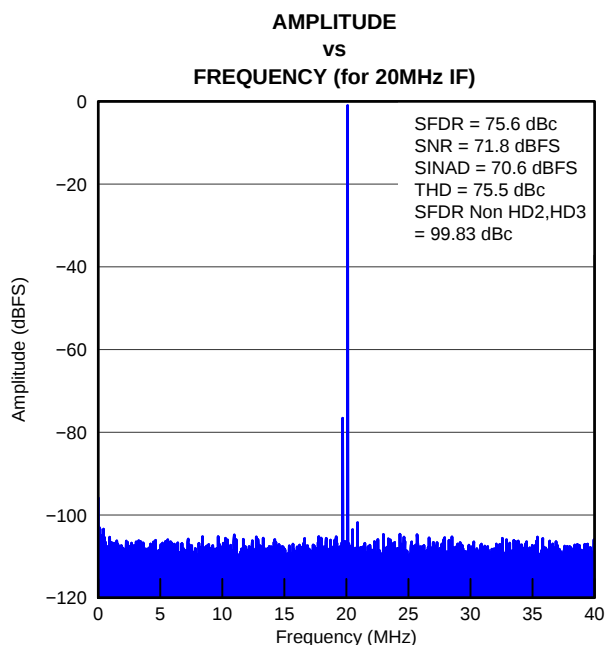


Figure 12.

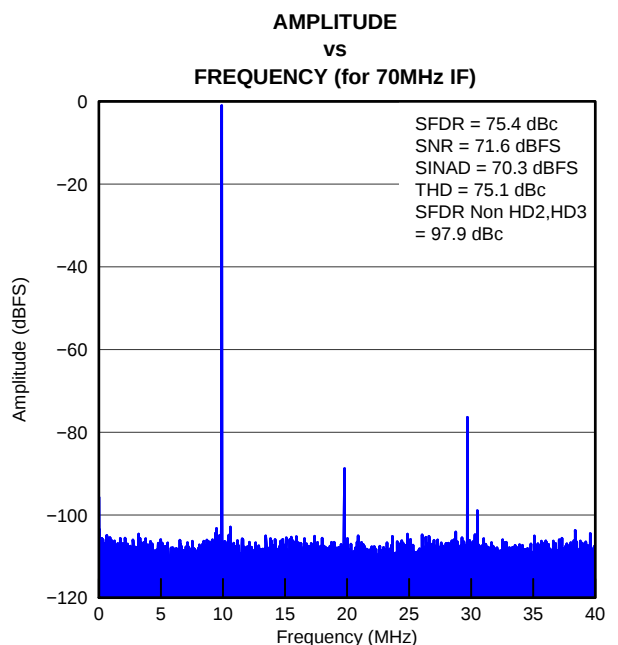


Figure 13.

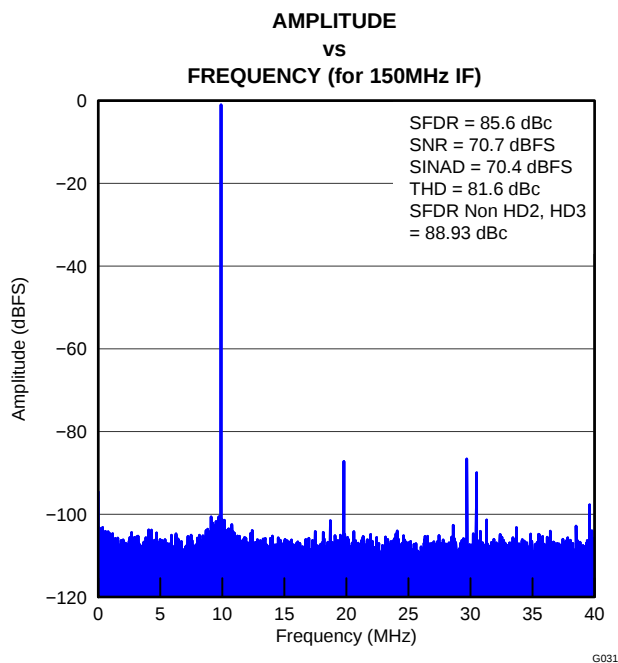


Figure 14.

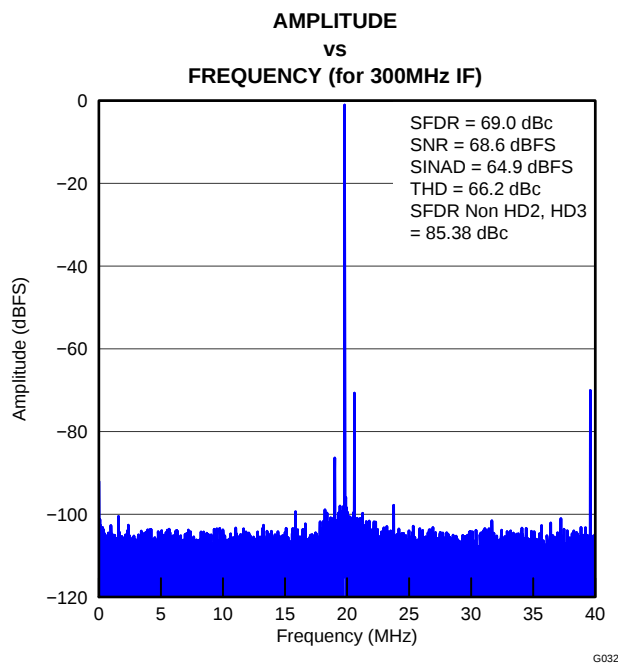


Figure 15.

## TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.8V, AVDD\_3V = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, -1dBFS differential analog input, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0dB gain mode

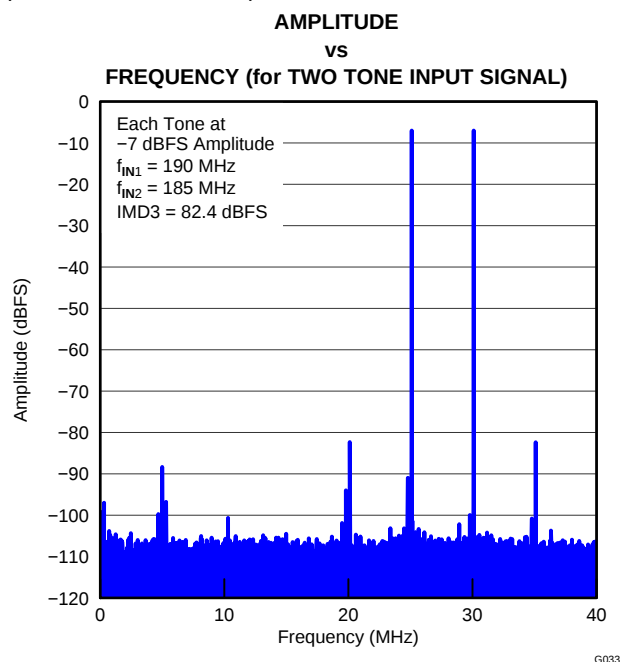


Figure 16.

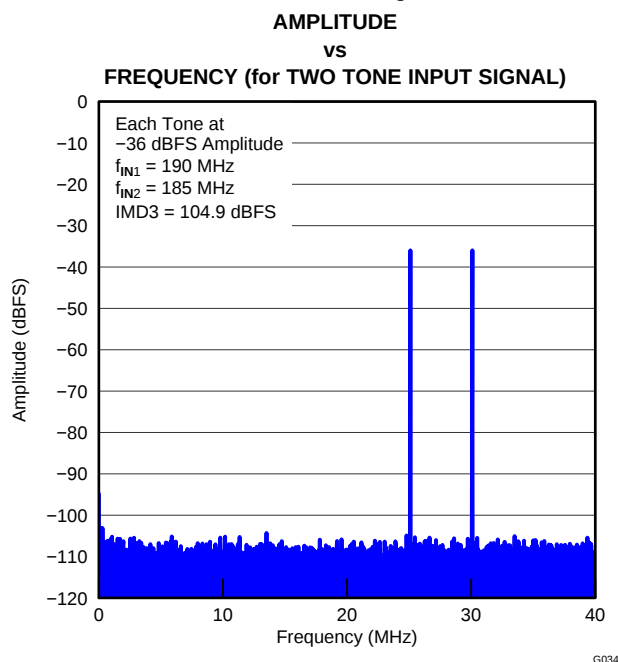


Figure 17.

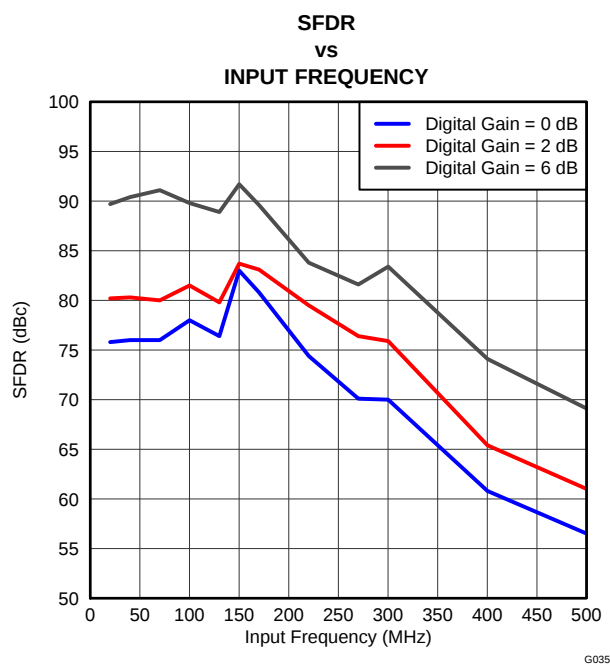


Figure 18.

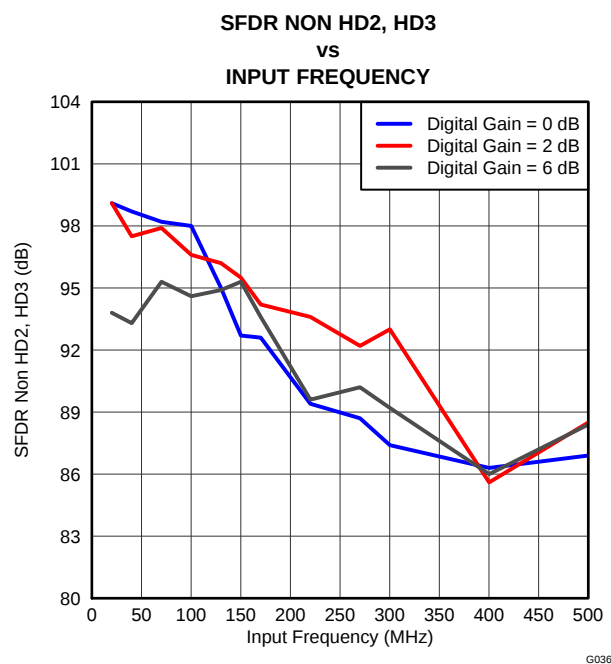


Figure 19.

### TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.8V, AVDD\_3V = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, -1dBFS differential analog input, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0dB gain mode

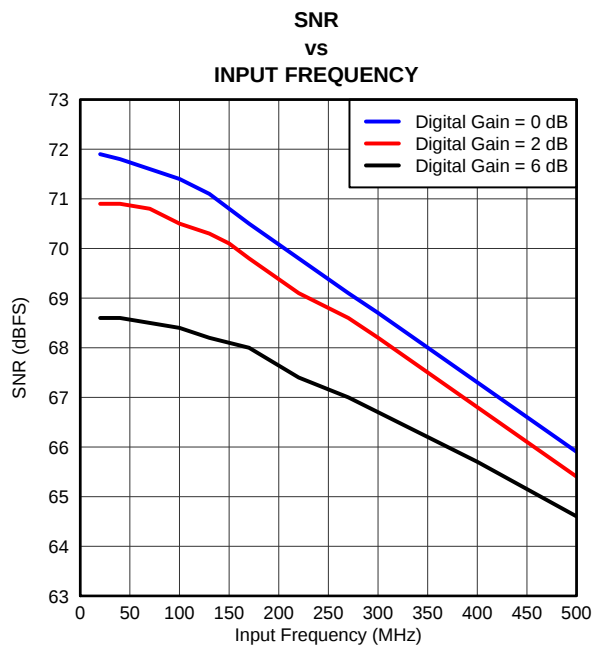


Figure 20.

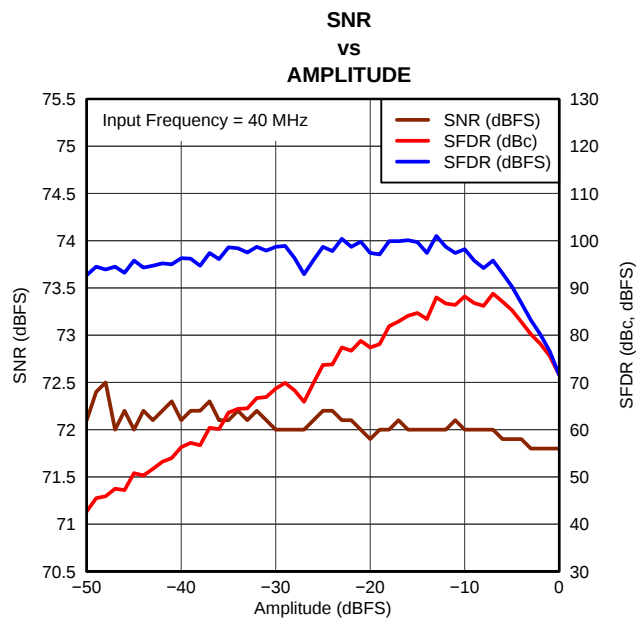


Figure 21.

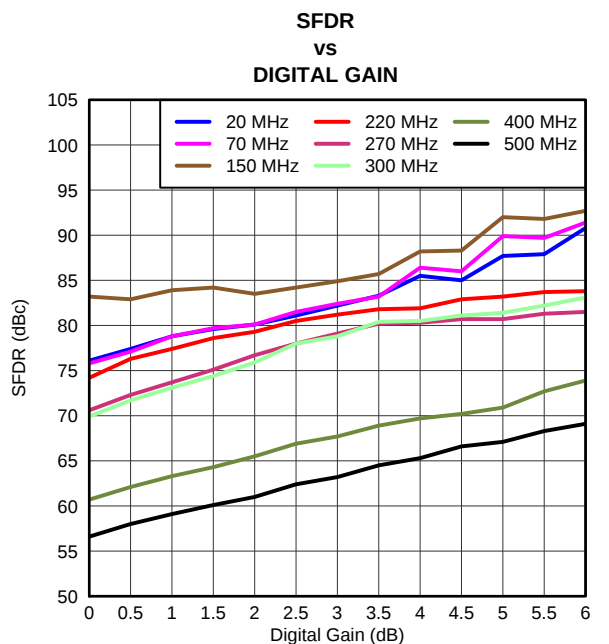


Figure 22.

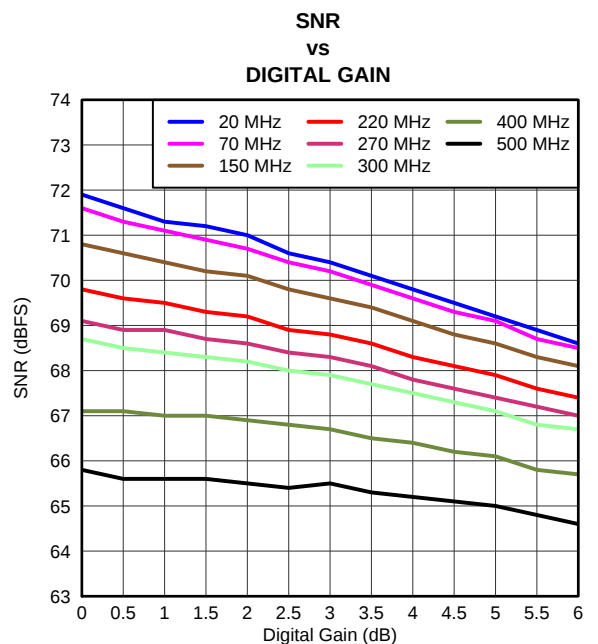


Figure 23.

## TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.8V, AVDD\_3V = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, -1dBFS differential analog input, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0dB gain mode

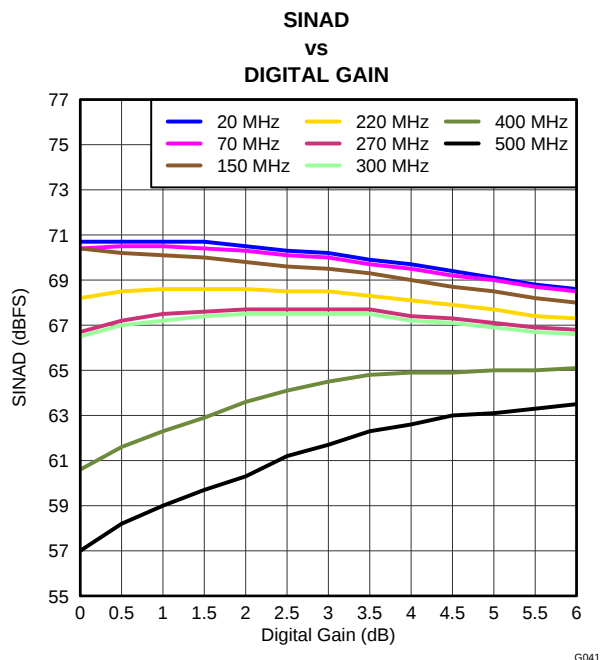


Figure 24.

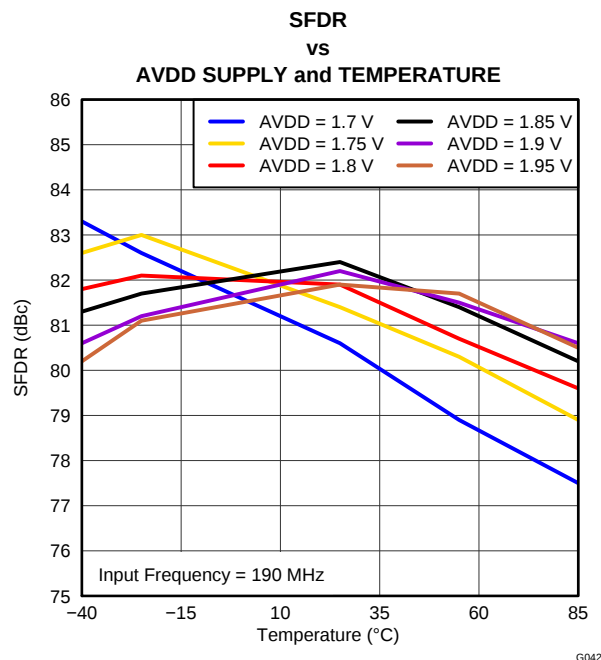


Figure 25.

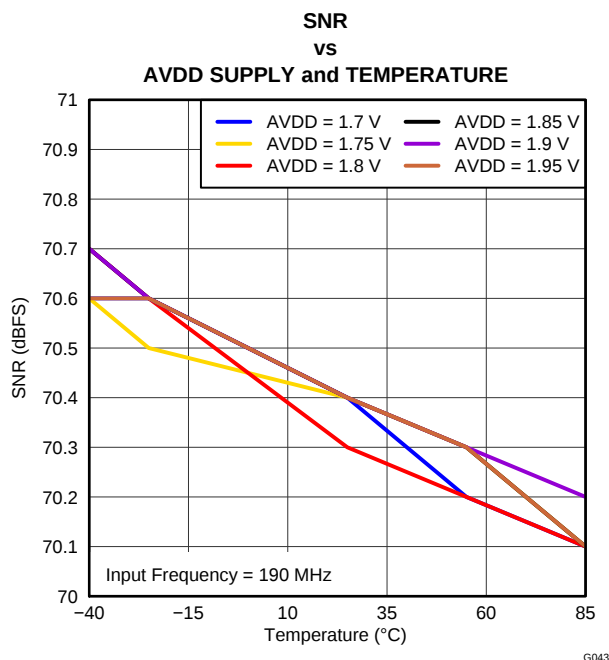


Figure 26.

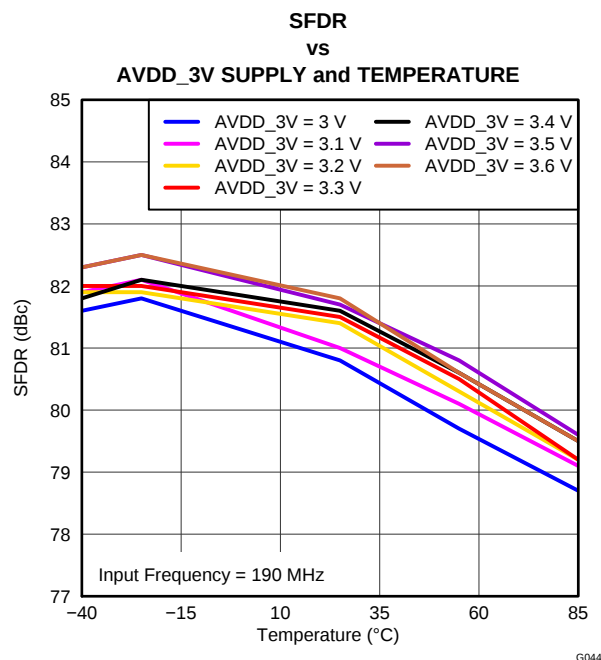


Figure 27.

### TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.8V, AVDD\_3V = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, -1dBFS differential analog input, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0dB gain mode

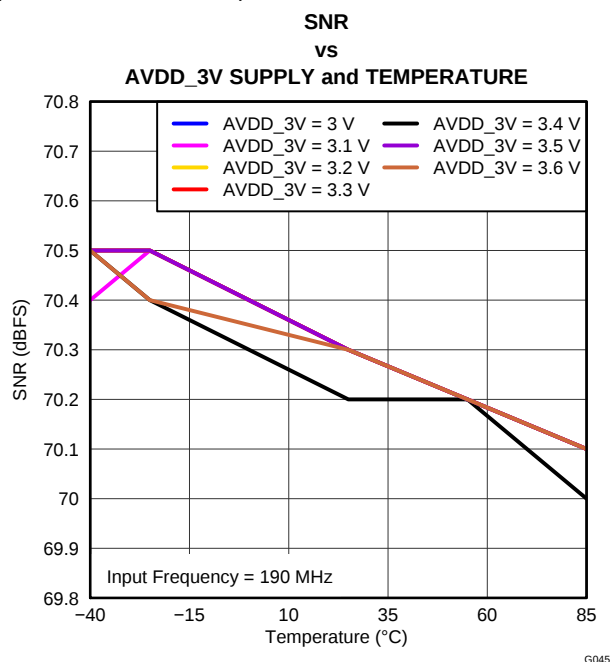


Figure 28.

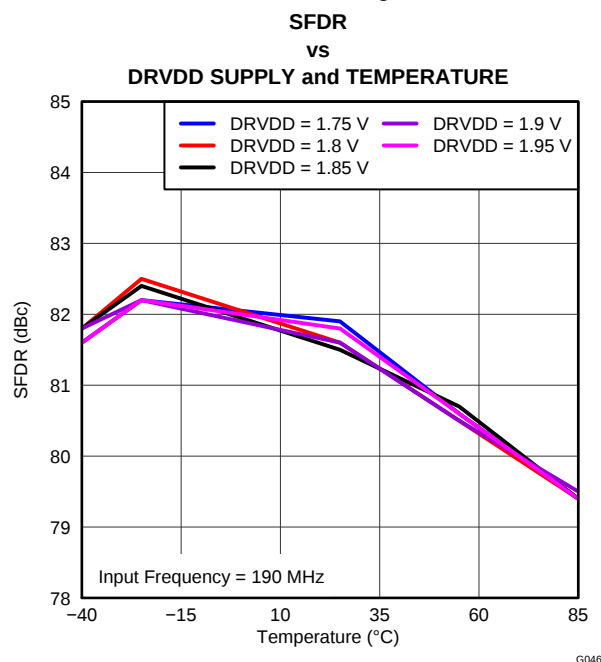


Figure 29.

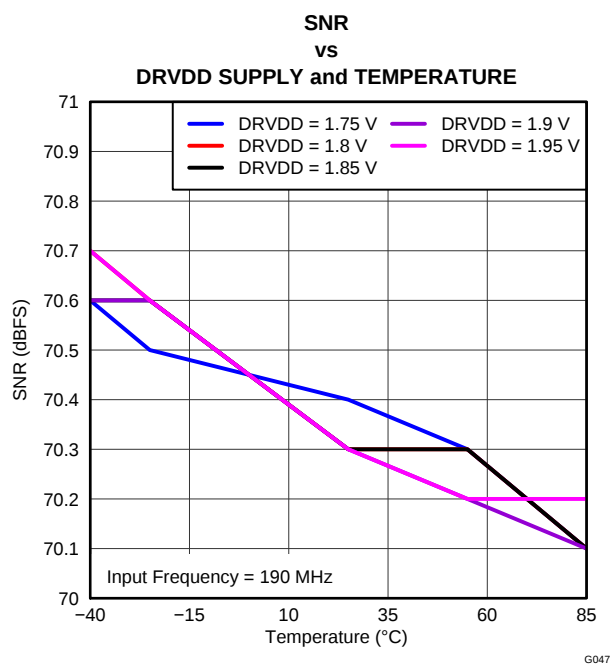


Figure 30.

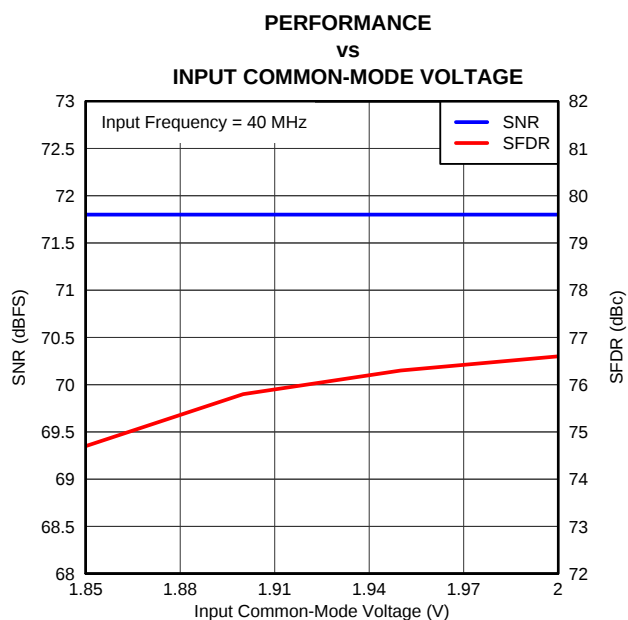


Figure 31.

## TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.8V, AVDD\_3V = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, -1dBFS differential analog input, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0dB gain mode

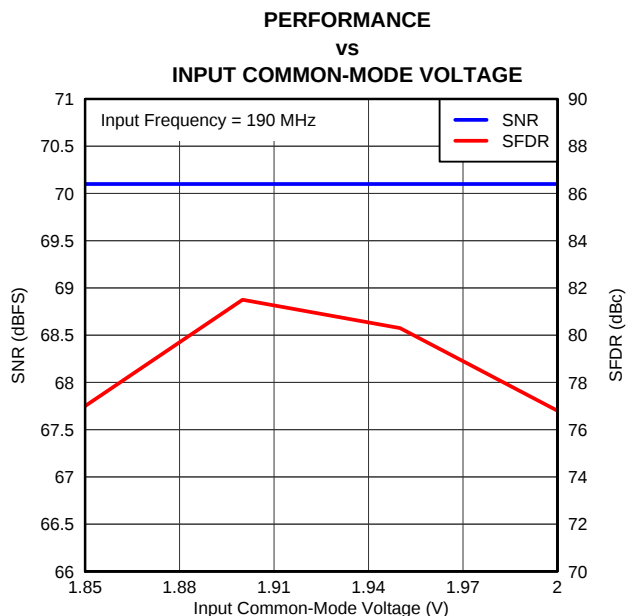


Figure 32.

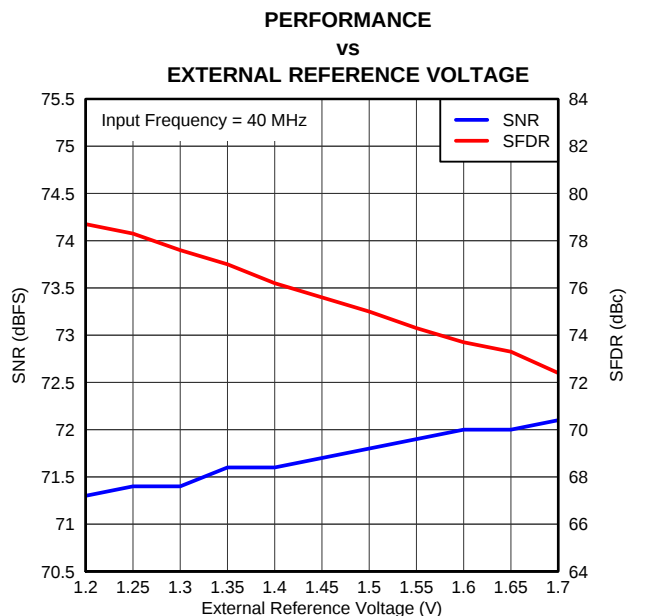


Figure 33.

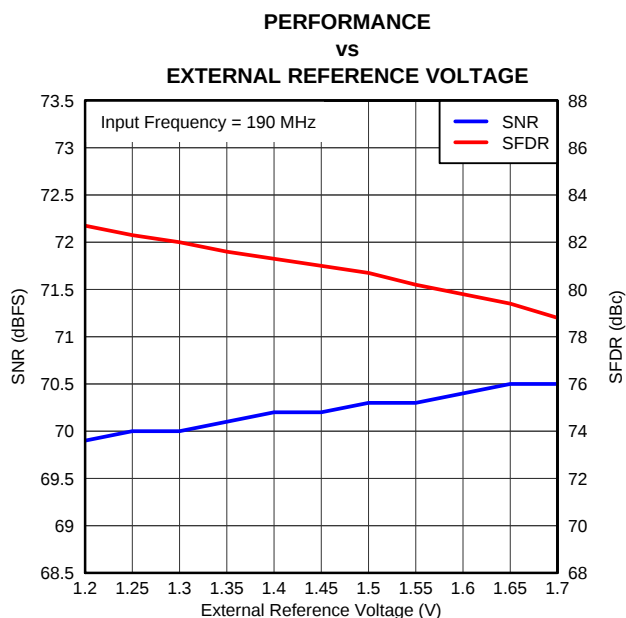


Figure 34.

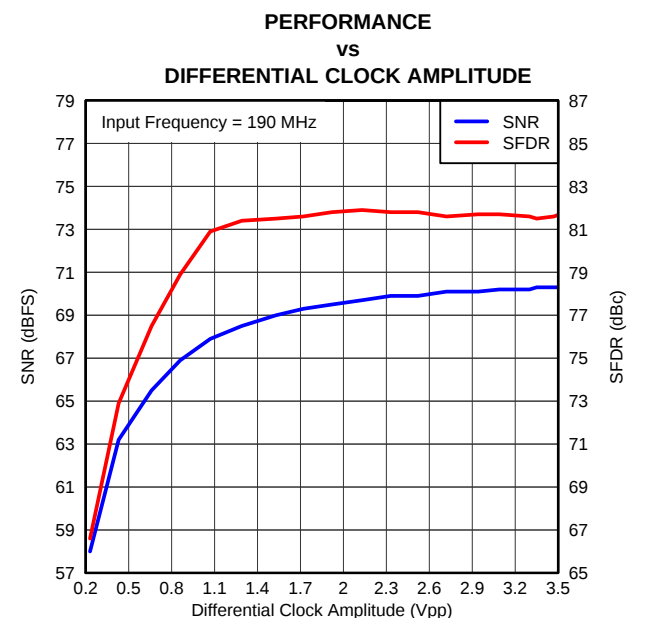
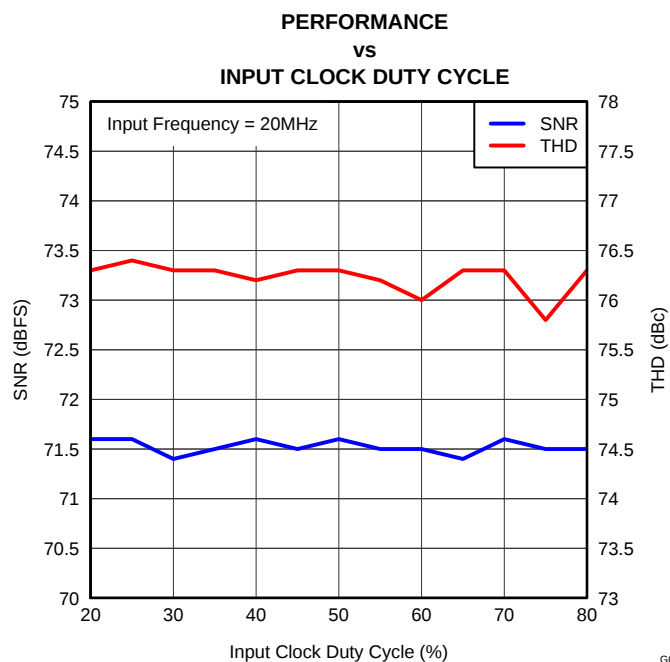


Figure 35.

### TYPICAL CHARACTERISTICS (continued)

At +25°C, AVDD = 1.8V, AVDD\_3V = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0dB gain mode



**Figure 36.**

## TYPICAL CHARACTERISTICS: COMMON

At +25°C, AVDD = 1.8V, AVDD\_3V = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, -1dBFS differential analog input, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0dB gain mode

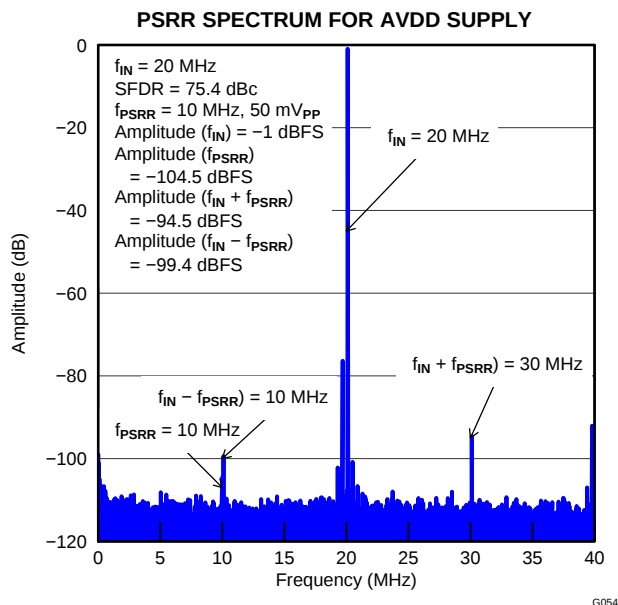


Figure 37.

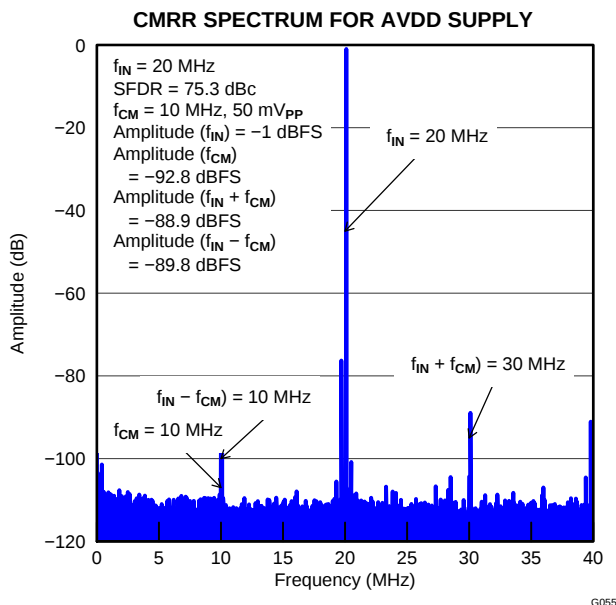


Figure 38.

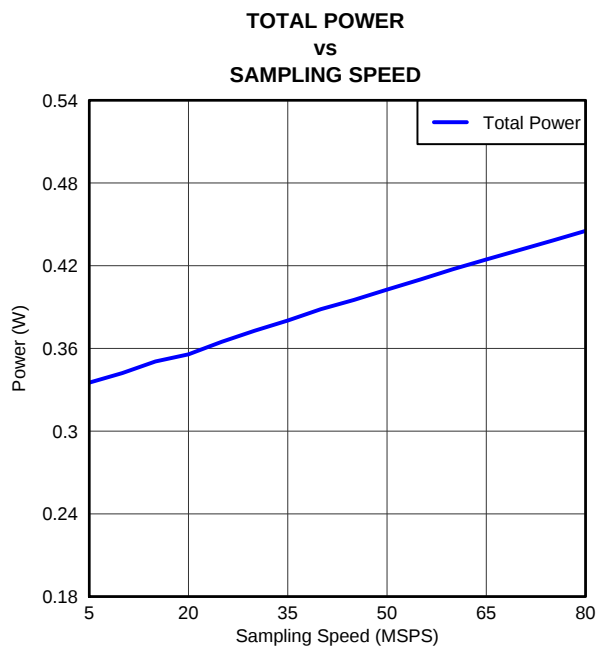


Figure 39.

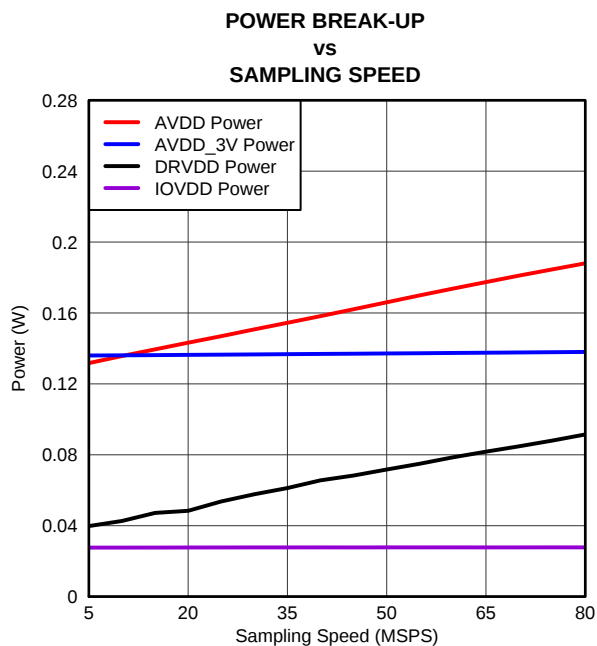
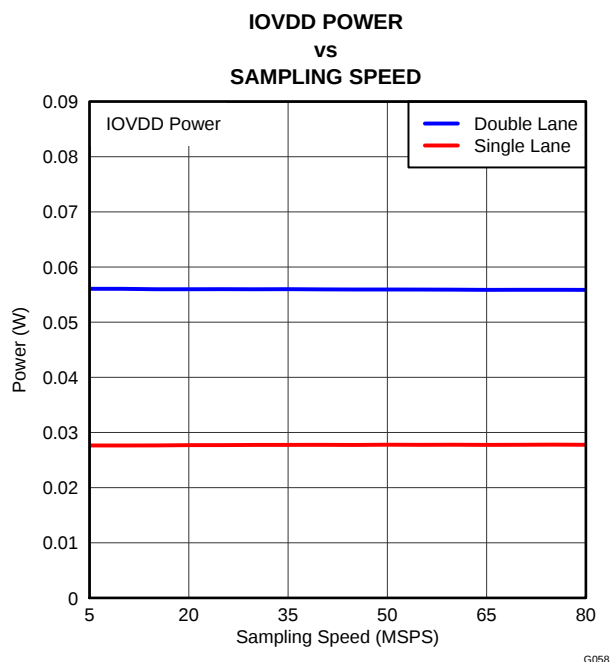


Figure 40.

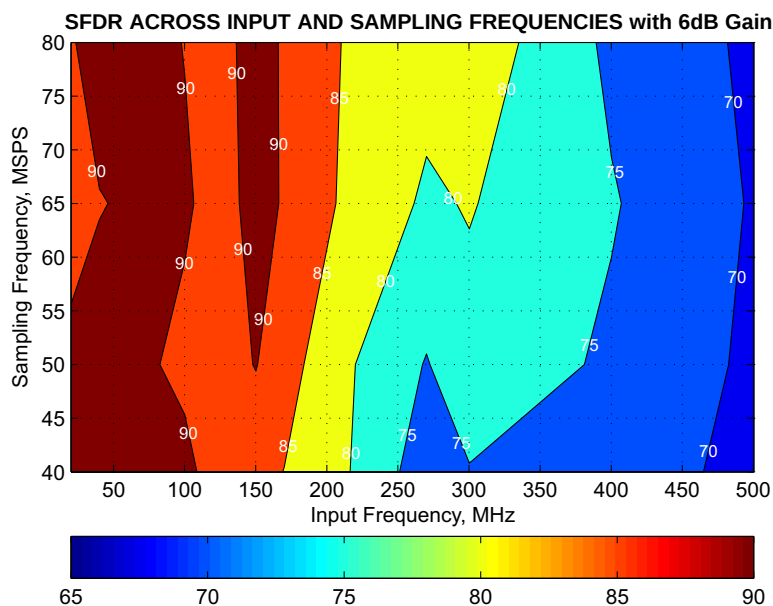
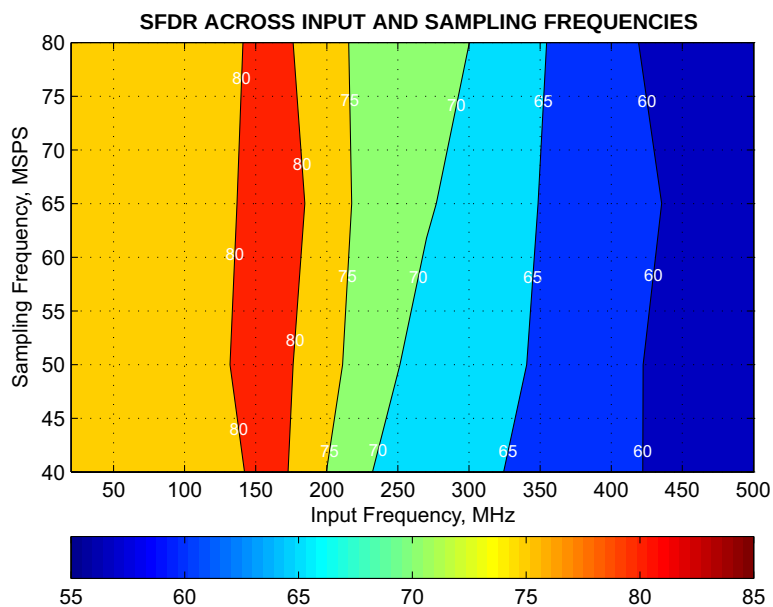
**TYPICAL CHARACTERISTICS: COMMON (continued)**

At +25°C, AVDD = 1.8V, AVDD\_3V = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0dB gain mode

**Figure 41.**

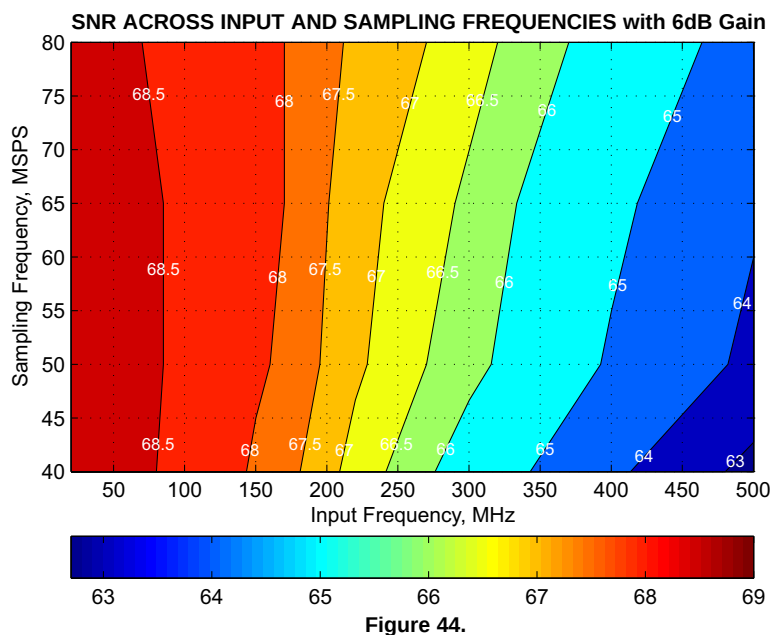
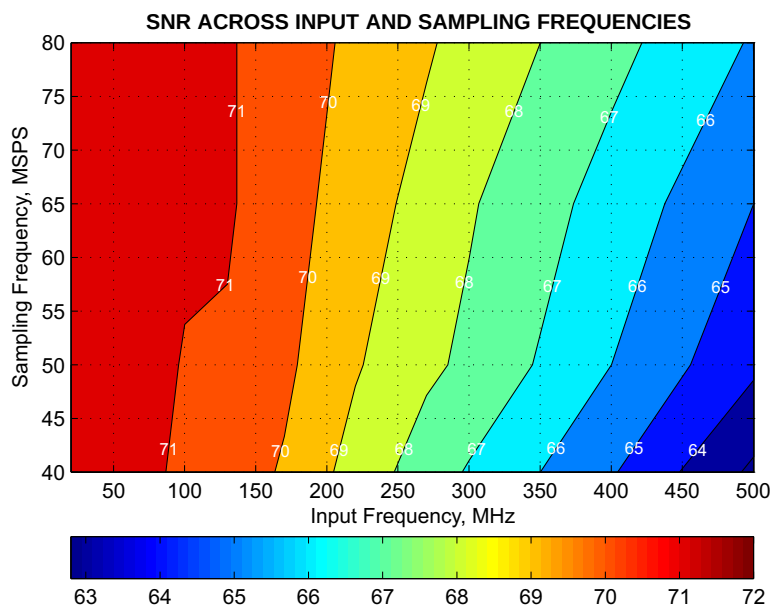
## TYPICAL CHARACTERISTICS: CONTOUR

At +25°C, AVDD = 1.8V, AVDD\_3V = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, –1dBFS differential analog input, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0dB gain mode



### TYPICAL CHARACTERISTICS: CONTOUR (continued)

At +25°C, AVDD = 1.8V, AVDD\_3V = 3.3V, DRVDD = 1.8V, maximum rated sampling frequency, sine wave input clock, 1.5VPP differential clock amplitude, 50% clock duty cycle, -1dBFS differential analog input, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted. Note that after reset, the device is in 0dB gain mode



## APPLICATION INFORMATION

### THEORY OF OPERATION

The ADS61JB23 is a family of buffered analog input and ultralow power ADCs with maximum sampling rates up to 80MSPS. The conversion process is initiated by a rising edge of the external input clock and the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline, resulting in a data latency of 21 clock cycles. The output is available as 12-bit data, coded in either straight offset binary or binary twos complement format, with JESD207A interface in CML logic levels.

### ANALOG INPUTS

The analog input pins have analog buffers (running off the AVDD3V supply) that internally drive the differential sampling circuit. As a result of the analog buffer, the input pins present high input impedance to the external driving source (10kΩ dc resistance and 2pF input capacitance). The buffer helps to isolate the external driving source from the switching currents of the sampling circuit. This buffering makes it easy to drive the buffered inputs compared to an ADC without the buffer.

The input common-mode is set internally using a 5kΩ resistor from each input pin to 1.95V, so the input signal can be ac-coupled to the pins. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.5V) and (VCM – 0.5V), resulting in a 2V<sub>PP</sub> differential input swing.

The input sampling circuit has a high 3dB bandwidth that extends up to 450 MHz (measured from the input pins to the sampled voltage). Figure 45 shows an equivalent circuit for the analog input.

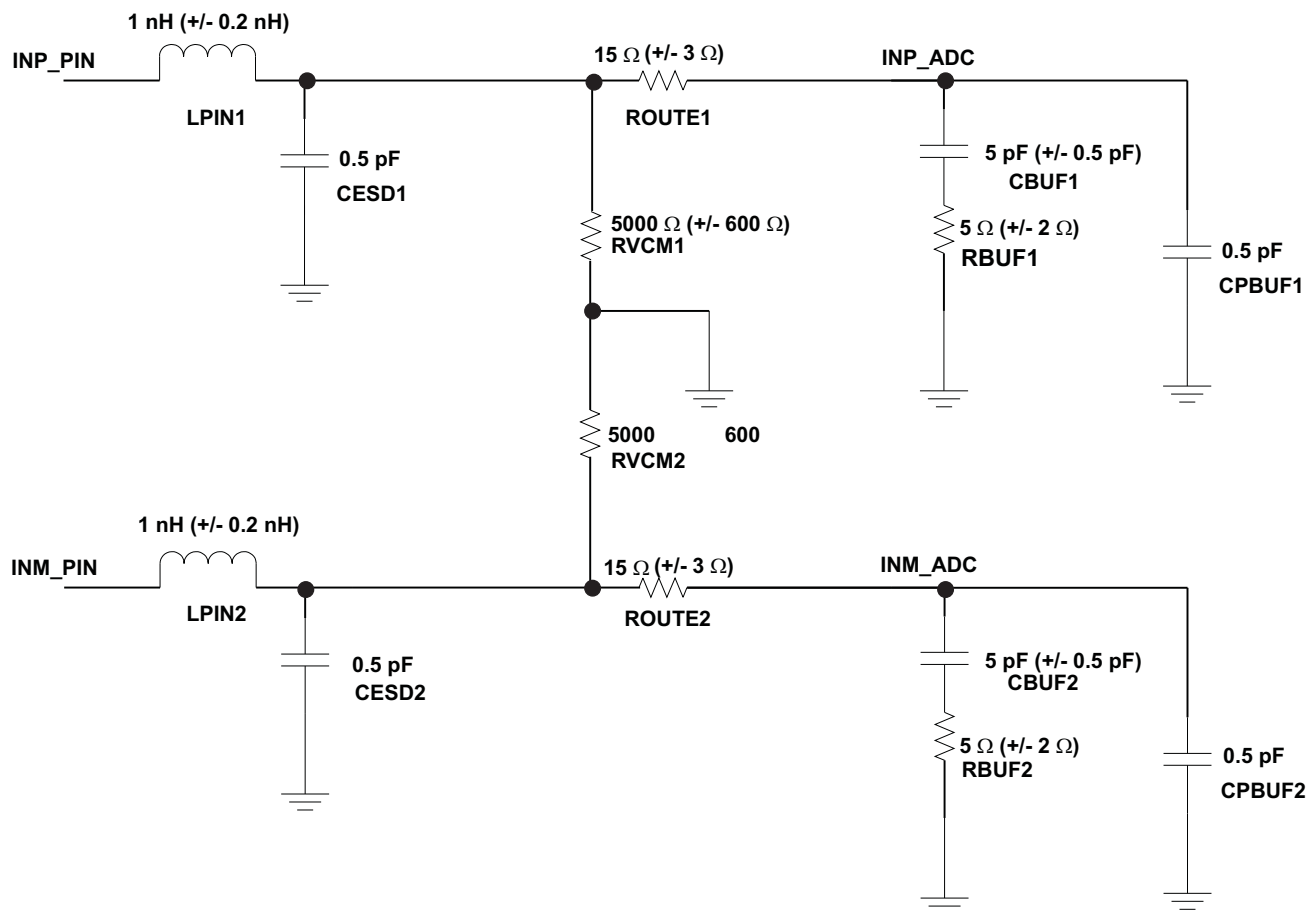
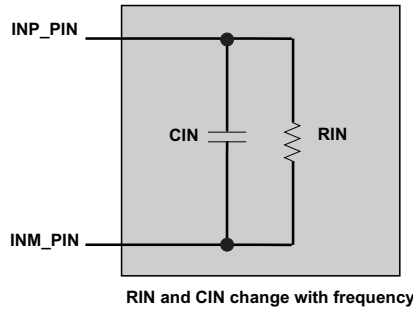


Figure 45. Equivalent Circuit

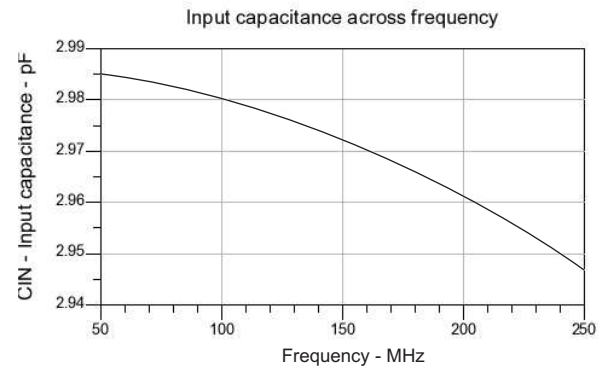
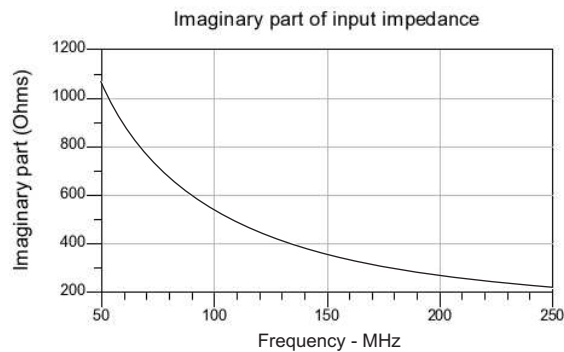
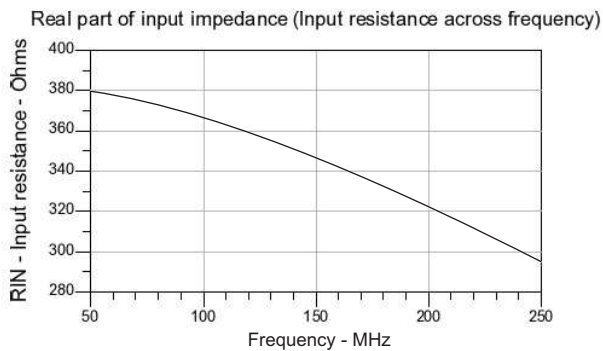
## DRIVE CIRCUIT REQUIREMENTS

For optimum performance, the analog inputs must be driven differentially. This technique improves the common-mode noise immunity and even-order harmonic rejection. A small resistor ( $5\Omega$ ) in series with each input pin is recommended to damp out ringing caused by package parasitics.

and show the differential impedance ( $Z_{IN} = R_{IN} \parallel C_{IN}$ ) seen by looking into the ADC input pins. The presence of the analog input buffer results in an almost constant input capacitance up to 1GHz.



At frequency F :  
 Real part of input impedance (input resistance) = RIN  
 Imaginary part of input impedance =  $1/(2 \cdot \pi \cdot F \cdot C_{IN})$   
 Input capacitance = CIN



## EXAMPLE DRIVING CIRCUITS

Two example driving circuit configurations are shown in Figure 46 and Figure 47—one optimized for low input frequencies and the other optimized for high input frequencies.

The presence of internal analog buffers makes the ADS61JB23 simple to drive by absorbing kick-back noise of ADC. The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch and good performance is obtained in input frequency range of interest.

The drive circuit for low input frequencies (<200MHz) in Figure 46 uses two back to back connected ADT1-1 transformers terminated by 50Ω near the ADC side.

An additional termination resistor pair may be required between the two transformers to improve even order harmonic performance as shown in drive circuit for high input frequencies (>200MHz) in Figure 47. The center point of this termination is connected to ground to improve the balance between the P (positive) and M (negative) sides. The example circuit uses two back to back connected ADTL2-18 transformers with 200Ω termination between them and 100Ω at secondary of second transformer to obtain an effective 50Ω (for a 50Ω source impedance). The ac-coupling capacitors allow the analog inputs to self-bias around the required common-mode voltage.

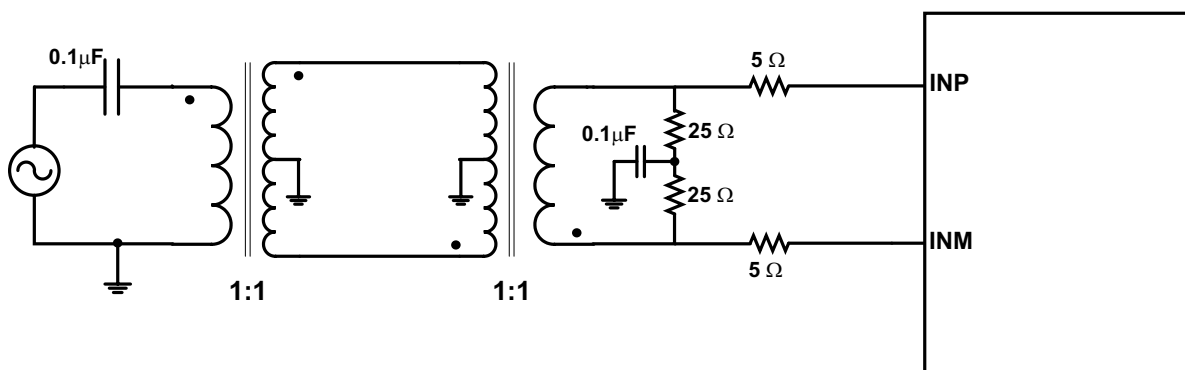


Figure 46. Drive Circuit with Low Bandwidth (for Low Input Frequencies)

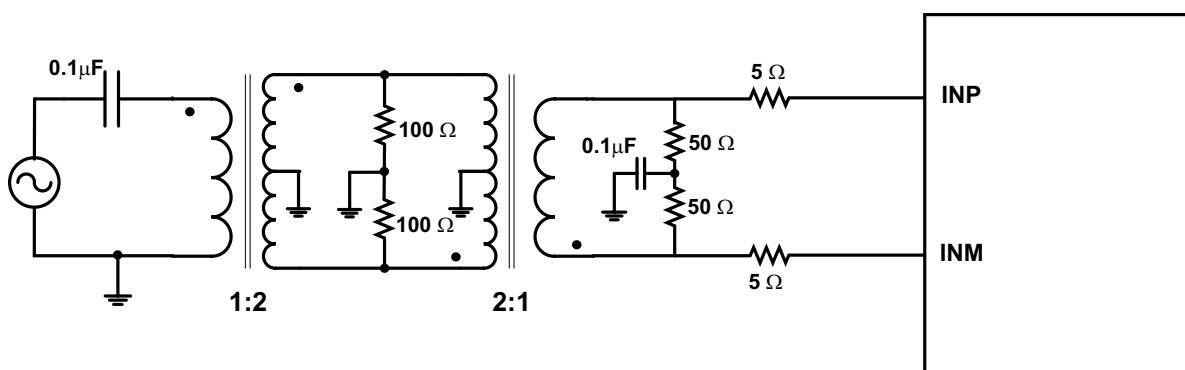
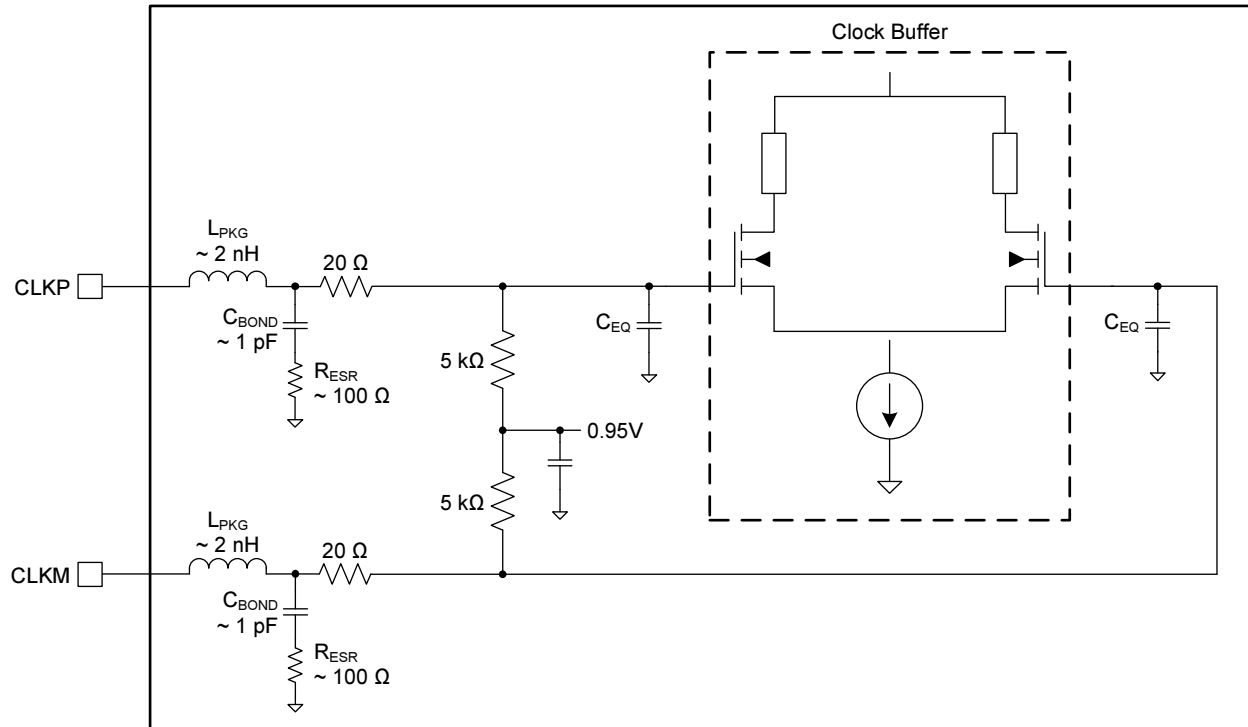


Figure 47. Drive Circuit with High Bandwidth (for High Input Frequencies)

## CLOCK INPUT

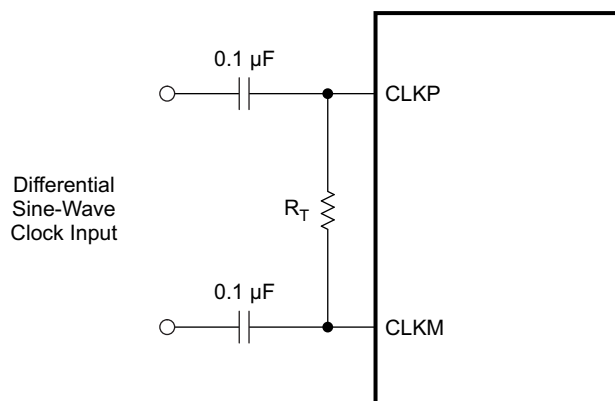
The ADS61JB23 clock inputs can be driven differentially by sine, LVPECL, or LVDS source with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to 0.95V using internal 5k $\Omega$  resistors as shown in Figure 48. This setting allows the use of transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL and LVDS clock sources (see Figure 49, Figure 50, and Figure 51).



Note:  $C_{EQ}$  is 1pF to 3pF and is the equivalent input capacitance of the clock buffer.

**Figure 48. Internal Clock Buffer**

For best performance, the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. It is recommended to keep differential voltage between clock inputs less than 1.8V<sub>PP</sub> to get best performance. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.



**Figure 49. Differential Sine-Wave Clock Driving Circuit**

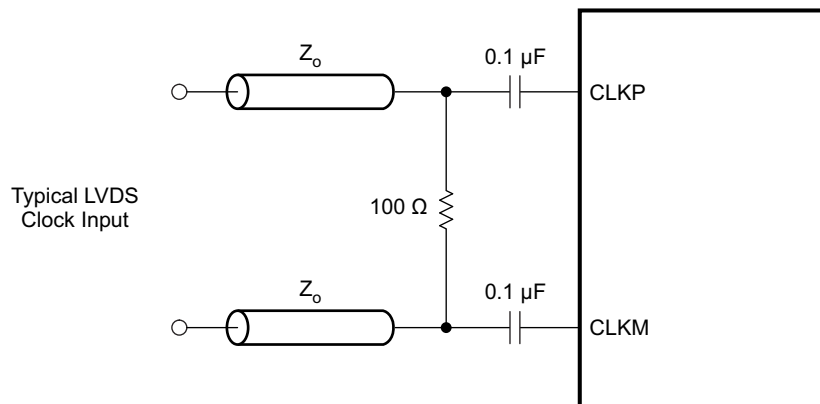


Figure 50. LVDS Clock Driving Circuit

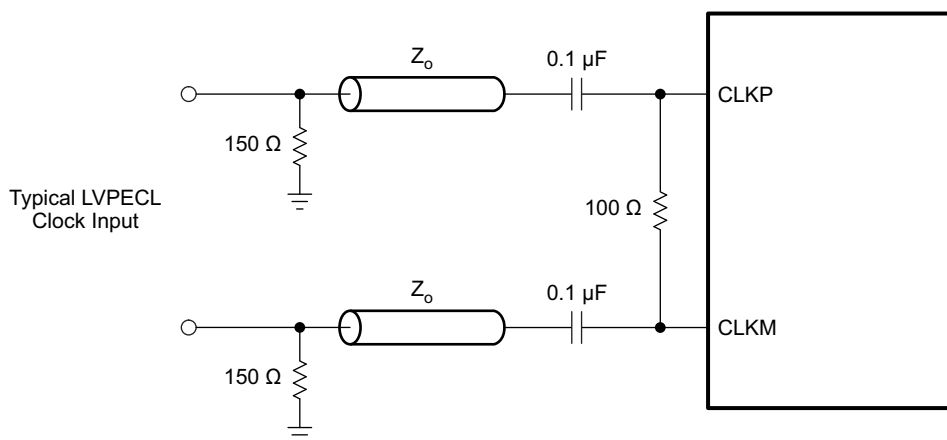


Figure 51. LVPECL Clock Driving Circuit

## FINE GAIN CONTROL

The ADS61JB23 includes gain settings that can be used to get improved SFDR performance (compared to no gain). The gain is programmable from 0dB to 6dB (in 0.5dB steps). For each gain setting, the analog input full-scale range scales proportionally, as shown in [Table 9](#).

The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades about 0.5dB. The SNR degradation is less at high input frequencies. As a result, the fine gain is very useful at high input frequencies as the SFDR improvement is significant with marginal degradation in SNR.

So, the fine gain can be used to trade-off between SFDR and SNR. Note that the default gain after reset is 0dB.

Table 9. Full-scale Range Across Gains

| FINE_GAIN<3:0> | GAIN, dB   | TYPE                                           | FULL-SCALE, Vpp |
|----------------|------------|------------------------------------------------|-----------------|
| 0000           | 0          | Fine gain, programmable<br>Default after reset | 2.00            |
| 0001           | 0.5        |                                                | 1.89            |
| 0010           | 1          |                                                | 1.78            |
| 0011           | 1.5        |                                                | 1.68            |
| 0100           | 2          |                                                | 1.59            |
| 0101           | 2.5        |                                                | 1.5             |
| 0110           | 3          |                                                | 1.42            |
| 0111           | 3.5        |                                                | 1.34            |
| 1000           | 4          |                                                | 1.26            |
| 1001           | 4.5        |                                                | 1.19            |
| 1010           | 5          |                                                | 1.12            |
| 1011           | 5.5        |                                                | 1.06            |
| 1100           | 6          |                                                | 1.00            |
| 1101           | Do not use |                                                |                 |
| 1110           |            |                                                |                 |
| 1111           |            |                                                |                 |

## SIGNAL POWER ESTIMATION

The ADS61JB23 includes a power estimation circuit that can be used to obtain a coarse power estimate (accurate to within a dB) of the input signal averaged over a programmable number of samples. The power estimate can be made available on pins DETECT<3:0> by enabling the bit EN\_PWR\_EST. The states of bits DETECT<3:0> maps to the input signal power is shown in Table 10.

Table 10. State of DETECT&lt;3:0&gt; Versus Input Signal Power

| INPUT SIGNAL POWER RANGE IN dBFs | DETECT<3:0> | INPUT SIGNAL POWER RANGE IN dBFs | DETECT<3:0> |
|----------------------------------|-------------|----------------------------------|-------------|
| –Inf to –12.5                    | 0001        | –6.5 to –5.5                     | 1000        |
| –12.5 to –11.5                   | 0010        | –5.5 to –4.5                     | 1001        |
| –11.5 to –10.5                   | 0011        | –4.5 to –3.5                     | 1010        |
| –10.5 to –9.5                    | 0100        | –3.5 to –2.5                     | 1011        |
| –9.5 to –8.5                     | 0101        | –2.5 to –1.5                     | 1100        |
| –8.5 to –7.5                     | 0110        | –1.5 to 0                        | 1101        |
| –7.5 to –6.5                     | 0111        | 0 to +1                          | 1110        |

The number of samples used for computing the average power is set by SAMPLES\_PWR\_EST<2:0> as shown in Table 11.

Table 11. Number of Samples Used for Power Estimation

| SAMPLES_PWR_EST<2:0> | NUMBER OF SAMPLES |
|----------------------|-------------------|
| 000                  | 1K                |
| 001                  | 2K                |
| 010                  | 4K                |
| 011                  | 8K                |
| 100                  | 16K               |

## DEFINITION OF SPECIFICATIONS

**Analog Bandwidth** – The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

**Aperture Delay** – The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay will be different across channels. The maximum variation is specified as aperture delay variation (channel-channel).

**Aperture Uncertainty (Jitter)** – The sample-to-sample variation in aperture delay.

**Clock Pulse Width/Duty Cycle** – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

**Maximum Conversion Rate** – The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

**Minimum Conversion Rate** – The minimum sampling rate at which the ADC functions.

**Differential Nonlinearity (DNL)** – An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

**Integral Nonlinearity (INL)** – The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

**Gain Error** – Gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error due to reference inaccuracy and error due to the channel. Both these errors are specified independently as  $E_{GREF}$  and  $E_{GCHAN}$ .

To a first order approximation, the total gain error will be  $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$ .

For example, if  $E_{TOTAL} = \pm 0.5\%$ , the full-scale input varies from  $(1 - 0.5/100) \times FS_{ideal}$  to  $(1 + 0.5/100) \times FS_{ideal}$ .

**Offset Error** – The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

**Temperature Drift** – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from  $T_{MIN}$  to  $T_{MAX}$ . It is calculated by dividing the maximum deviation of the parameter across the  $T_{MIN}$  to  $T_{MAX}$  range by the difference  $T_{MAX} - T_{MIN}$ .

**Signal-to-Noise Ratio** – SNR is the ratio of the power of the fundamental ( $P_S$ ) to the noise floor power ( $P_N$ ), excluding the power at DC and the first nine harmonics.

$$SNR = 10 \log_{10} \frac{P_S}{P_N} \quad (1)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

**Signal-to-Noise and Distortion (SINAD)** – SINAD is the ratio of the power of the fundamental ( $P_S$ ) to the power of all the other spectral components including noise ( $P_N$ ) and distortion ( $P_D$ ), but excluding dc.

$$SINAD = 10 \log_{10} \frac{P_S}{P_N + P_D} \quad (2)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

**Effective Number of Bits (ENOB)** – The ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \quad (3)$$

**Total Harmonic Distortion (THD)** – THD is the ratio of the power of the fundamental ( $P_S$ ) to the power of the first nine harmonics ( $P_N$ ).

$$\text{THD} = 10\text{Log}^{10} \frac{P_S}{P_N} \quad (4)$$

THD is typically given in units of dBc (dB to carrier).

**Spurious-Free Dynamic Range (SFDR)** – The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

**Two-Tone Intermodulation Distortion** – IMD3 is the ratio of the power of the fundamental (at frequencies  $f_1$  and  $f_2$ ) to the power of the worst spectral component at either frequency  $2f_1-f_2$  or  $2f_2-f_1$ . IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

**DC Power Supply Rejection Ratio (DC PSRR)** – The DC PSRR is the ratio of the change in offset error to a change in analog supply voltage. The DC PSRR is typically given in units of mV/V.

**AC Power Supply Rejection Ratio (AC PSRR)** – AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If  $\Delta V_{SUP}$  is the change in supply voltage and  $\Delta V_{OUT}$  is the resultant change of the ADC output code (referred to the input), then

$$\text{PSRR} = 20\text{Log}^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \quad (\text{Expressed in dBc}) \quad (5)$$

**Voltage Overload Recovery** – The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6dB positive and negative overload. The deviation of the first few samples after the overload (from their expected values) is noted.

**Common Mode Rejection Ratio (CMRR)** – CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If  $\Delta V_{cm\_in}$  is the change in the common-mode voltage of the input pins and  $\Delta V_{OUT}$  is the resultant change of the ADC output code (referred to the input), then

$$\text{CMRR} = 20\text{Log}^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \quad (\text{Expressed in dBc}) \quad (6)$$

**Cross-Talk (only for multi-channel ADC)** – This is a measure of the internal coupling of a signal from adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). It is usually measured by applying a full-scale signal in the adjacent channel. Cross-talk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| ADS61JB23IRHAR   | ACTIVE        | VQFN         | RHA                | 40   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAUAG             | Level-3-260C-168 HR  | -40 to 85    | 61JB23                  | <a href="#">Samples</a> |
| ADS61JB23IRHAT   | ACTIVE        | VQFN         | RHA                | 40   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAUAG             | Level-3-260C-168 HR  | -40 to 85    | 61JB23                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADS61JB23IRHAR | VQFN         | RHA             | 40   | 2500 | 330.0              | 16.4               | 6.3     | 6.3     | 1.5     | 12.0    | 16.0   | Q2            |
| ADS61JB23IRHAT | VQFN         | RHA             | 40   | 250  | 180.0              | 16.4               | 6.3     | 6.3     | 1.5     | 12.0    | 16.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS

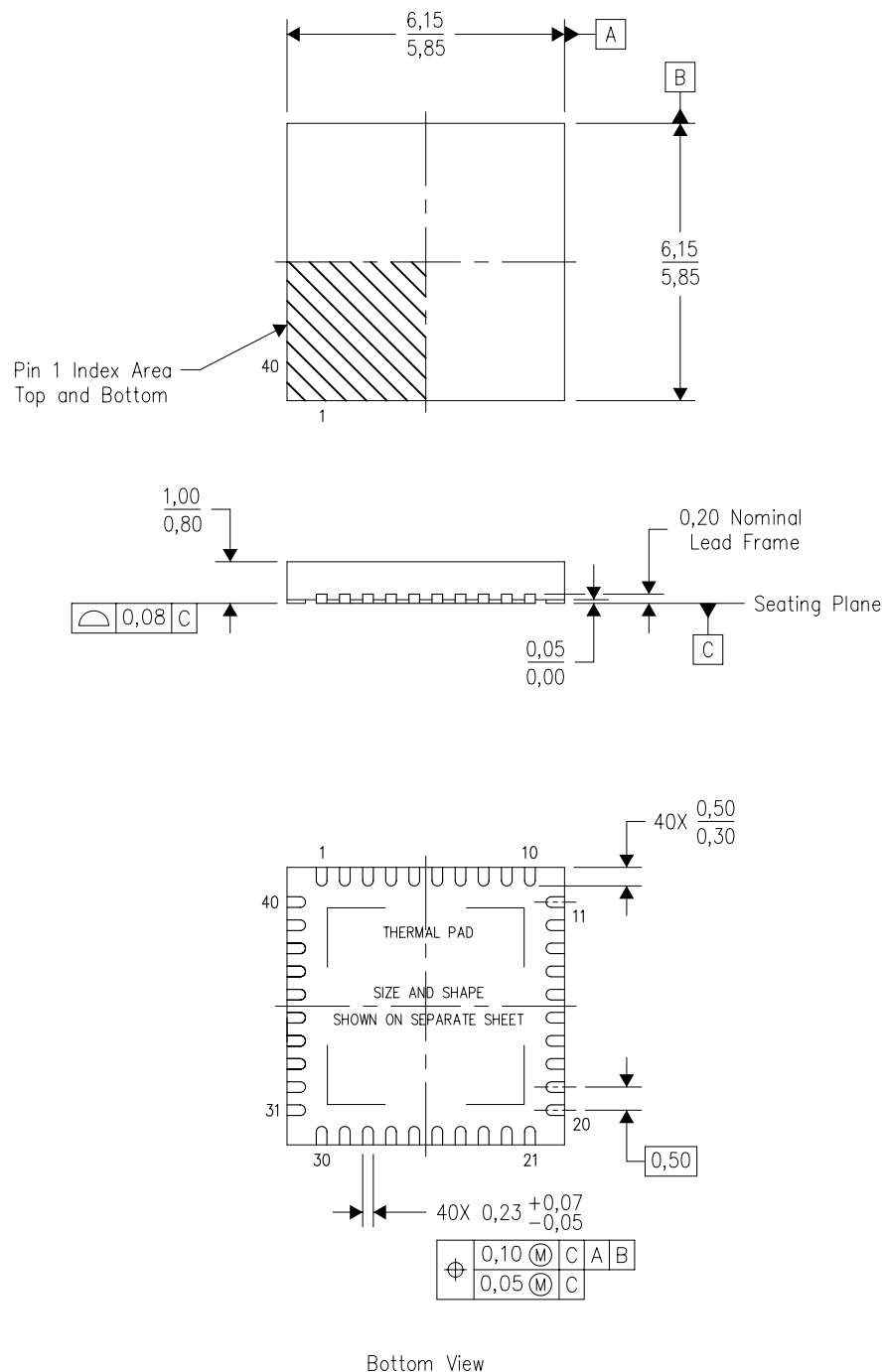


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADS61JB23IRHAR | VQFN         | RHA             | 40   | 2500 | 336.6       | 336.6      | 28.6        |
| ADS61JB23IRHAT | VQFN         | RHA             | 40   | 250  | 213.0       | 191.0      | 55.0        |

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



4204276/E 06/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) Package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Package complies to JEDEC MO-220 variation VJJD-2.

## THERMAL PAD MECHANICAL DATA

RHA (S-PVQFN-N40)

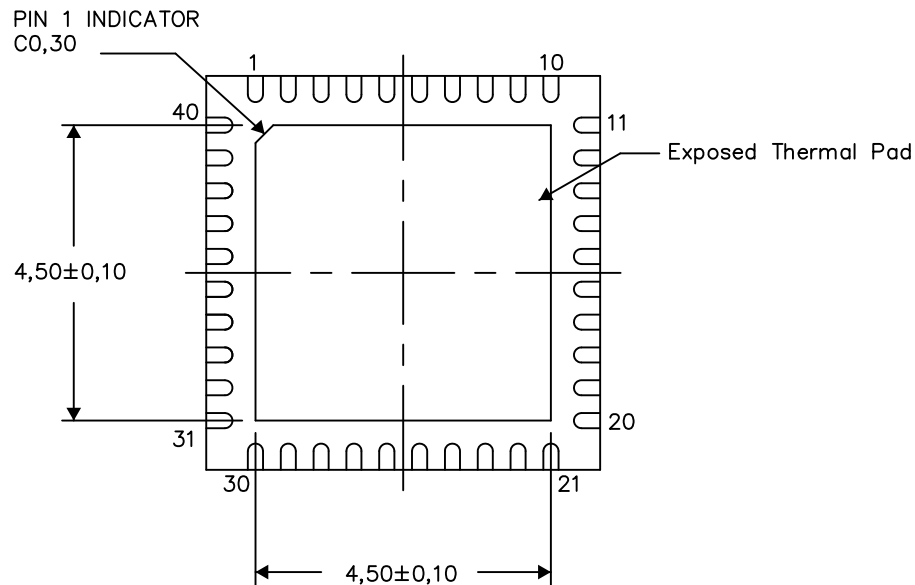
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

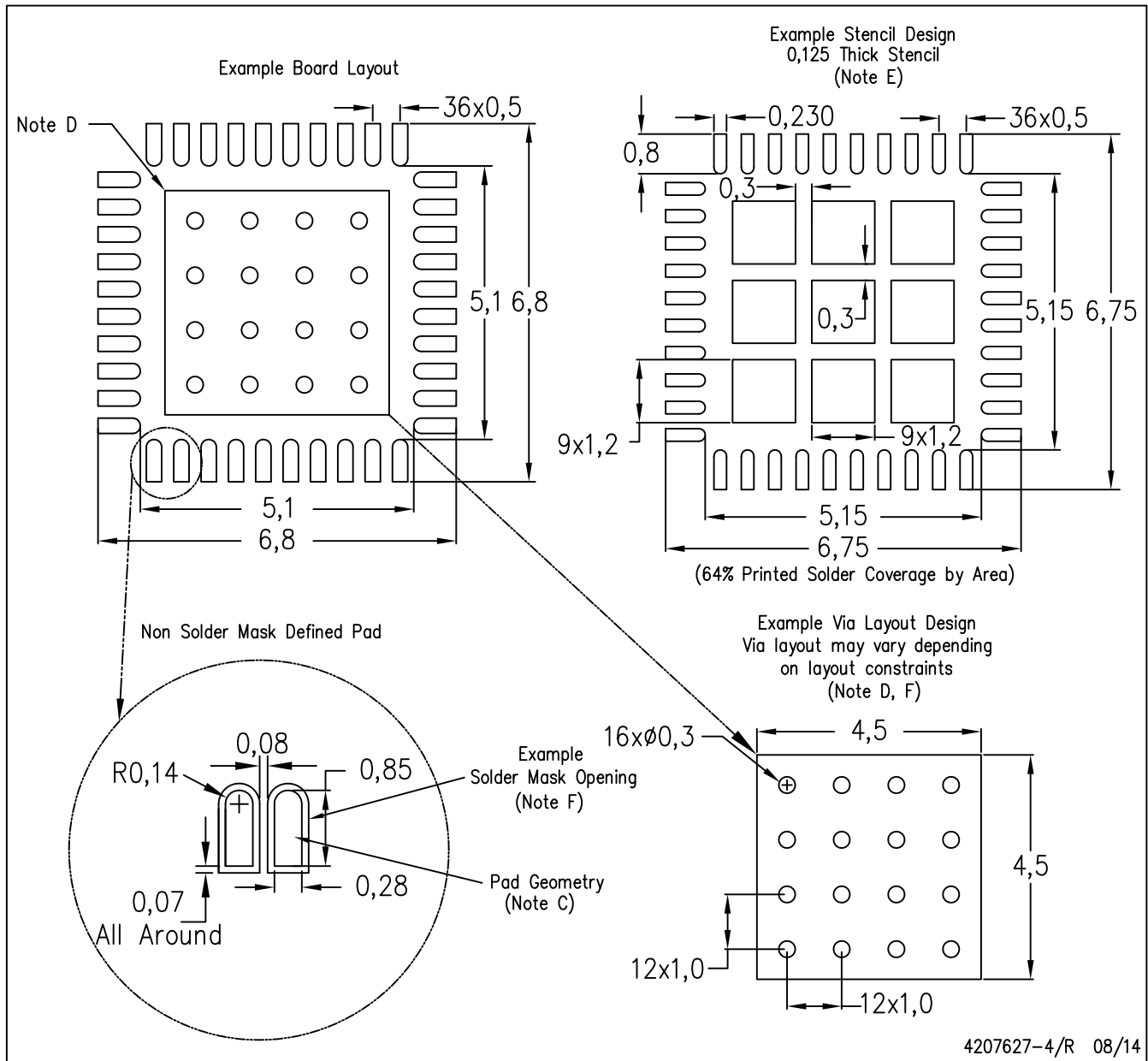
Exposed Thermal Pad Dimensions

4206355-4/X 08/14

NOTES: A. All linear dimensions are in millimeters

RHA (S-PVQFN-N40)

PLASTIC QUAD FLATPACK NO-LEAD



4207627-4/R 08/14

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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