

DS25BR150 3.125 Gbps LVDS Buffer

Check for Samples: [DS25BR150](#)

FEATURES

- DC - 3.125 Gbps Low Jitter, High Noise Immunity, Low Power Operation
- On-Chip 100 Ω Input and Output Termination Minimizes Insertion and Return Losses, Reduces Component Count and Minimizes Board Space
- 7 kV ESD on LVDS I/O Pins Protects Adjoining Components
- Small 3 mm x 3 mm WSON-8 Space Saving Package

APPLICATIONS

- Clock or Data Buffering / Repeating
- OC-48 / STM-16 Clock or Data Buffering / Repeating
- InfiniBand
- FireWire

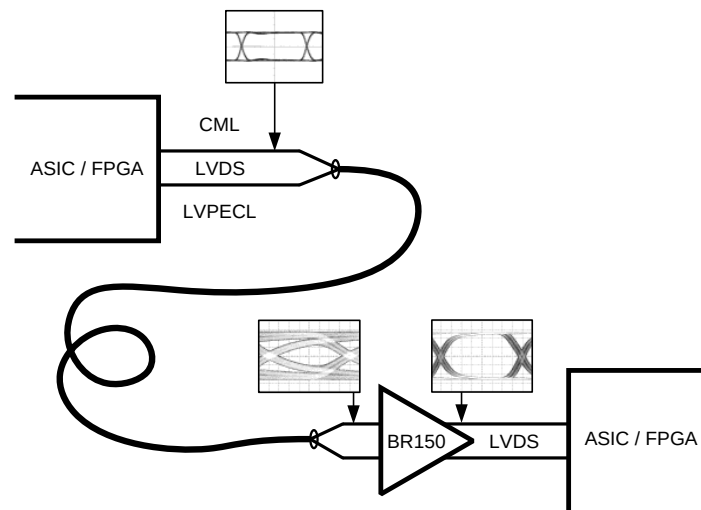
DESCRIPTION

The DS25BR150 is a single channel 3.125 Gbps LVDS buffer optimized for high-speed signal transmission over printed circuit boards and balanced cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity.

The DS25BR150 is a buffer/repeater with very low power consumption. Other LVDS devices with similar IO characteristics and with signal conditioning features include the following products. The DS25BR110 features four levels of equalization for use as an optimized receiver device, the DS25BR120 features four levels of pre-emphasis for use as an optimized driver device, and the DS25BR100 features both pre-emphasis and equalization for use as an optimized repeater device.

Wide input common mode range allows the receiver to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires a minimal space on the board while the flow-through pinout allows easy board layout. The differential inputs and outputs are internally terminated with a 100 Ω resistor to lower device input and output return losses, reduce component count, and further minimize board space.

Typical Application



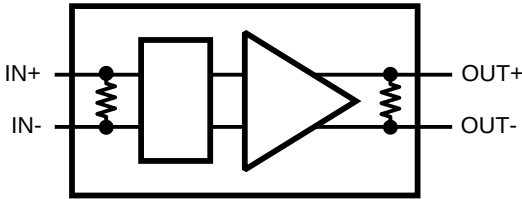
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

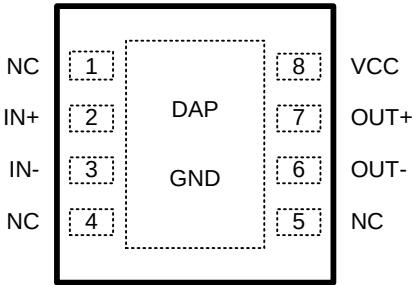
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2007–2013, Texas Instruments Incorporated

Block Diagram



Pin Diagram



WSON Package

PIN DESCRIPTION

Pin Name	Pin Name	Pin Type	Pin Description
NC	1	NA	"NO CONNECT" pin.
IN+	2	Input	Non-inverting LVDS input pin.
IN-	3	Input	Inverting LVDS input pin.
NC	4	NA	"NO CONNECT" pin.
NC	5	NA	"NO CONNECT" pin.
OUT-	6	Output	Inverting LVDS output pin.
OUT+	7	Output	Non-inverting LVDS Output pin.
VCC	8	Power	Power supply pin.
GND	DAP	Power	Ground pad (DAP - die attach pad)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

Supply Voltage (V_{CC})		-0.3V to +4V
LVDS Input Voltage (IN+, IN-)		-0.3V to +4V
Differential Input Voltage VID		1V
LVDS Output Voltage (OUT+, OUT-)		-0.3V to ($V_{CC} + 0.3V$)
LVDS Differential Output Voltage ((OUT+) - (OUT-))		0V to 1V
LVDS Output Short Circuit Current Duration		5 ms
Junction Temperature		+150°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature Range	Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	NGQ Package	2.08W
	Derate NGQ Package	16.7 mW/°C above +25°C
Package Thermal Resistance	θ_{JA}	+60.0°C/W
	θ_{JC}	+12.3°C/W
ESD Susceptibility	HBM ⁽³⁾	≥7 kV
	MM ⁽⁴⁾	≥250V
	CDM ⁽⁵⁾	≥1250V

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) Human Body Model, applicable std. JESD22-A114C
- (4) Machine Model, applicable std. JESD22-A115-A
- (5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Receiver Differential Input Voltage (V_{ID})	0		1	V
Operating Free Air Temperature (T_A)	-40	+25	+85	°C

DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS OUTPUT DC SPECIFICATIONS (OUT+, OUT-)						
V_{OD}	Differential Output Voltage	$R_L = 100\Omega$	250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States		-35		35	mV
V_{OS}	Offset Voltage	$R_L = 100\Omega$	1.05	1.2	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States		-35		35	mV
I_{OS}	Output Short Circuit Current ⁽⁴⁾	OUT to GND		-25	-50	mA
		OUT to V_{CC}		7.5	50	mA
C_{OUT}	Output Capacitance	Any LVDS Output Pin to GND		1.2		pF
R_{OUT}	Output Termination Resistor	Between OUT+ and OUT-		100		Ω

- (1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD} .
- (3) Typical values represent most likely parametric norms for $V_{CC} = +3.3V$ and $T_A = +25^\circ C$, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
- (4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS INPUT DC SPECIFICATIONS (IN+, IN-)						
V _{ID}	Input Differential Voltage		0		1	V
V _{TH}	Differential Input High Threshold	V _{CM} = +0.05V or V _{CC} -0.05V		0	+100	mV
V _{TL}	Differential Input Low Threshold		-100	0		mV
V _{CMR}	Common Mode Voltage Range	V _{ID} = 100 mV	0.05		V _{CC} - 0.05	V
I _{IN}	Input Current	V _{IN} = 3.6V or 0V V _{CC} = 3.6V or 0V		±1	±10	μA
C _{IN}	Input Capacitance	Any LVDS Input Pin to GND		1.7		pF
R _{IN}	Input Termination Resistor	Between IN+ and IN-		100		Ω
SUPPLY CURRENT						
I _{CC}	Supply Current			27	35	mA

AC Electrical Characteristics⁽¹⁾

Over recommended operating supply and temperature ranges unless otherwise specified.⁽²⁾⁽³⁾

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVDS OUTPUT AC SPECIFICATIONS (OUT+, OUT-)							
t _{PHLD}	Differential Propagation Delay High to Low	R _L = 100Ω		370	520	ps	
t _{PLHD}	Differential Propagation Delay Low to High			355	520	ps	
t _{SKD1}	Pulse Skew t _{PLHD} - t _{PHLD} ⁽⁴⁾			15	100	ps	
t _{SKD2}	Part to Part Skew ⁽⁵⁾			45	160	ps	
t _{LHT}	Rise Time	R _L = 100Ω		80	150	ps	
t _{HLT}	Fall Time			80	150	ps	
JITTER PERFORMANCE (Figure 5)							
t _{DJ1}	Deterministic Jitter (Peak-to-Peak Value) ⁽⁶⁾	V _{ID} = 350 mV V _{CM} = 1.2V K28.5 (NRZ)	2.5 Gbps		11	33	ps
t _{DJ2}			3.125 Gbps		15	41	ps
t _{RJ1}	Random Jitter (RMS Value) ⁽⁷⁾	V _{ID} = 350 mV V _{CM} = 1.2V Clock (RZ)	1.25 GHz		0.5	1	ps
t _{RJ2}			1.5625 GHz		0.5	1	ps
t _{TJ1}	Total Jitter (Peak to Peak Value) ⁽⁸⁾	V _{ID} = 350 mV V _{CM} = 1.2V PRBS-23 (NRZ)	2.5 Gbps		0.04	0.11	UI _{P-P}
t _{TJ2}			3.125 Gbps		0.07	0.15	UI _{P-P}

- (1) Specification is ensured by characterization and is not tested in production.
- (2) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
- (4) t_{SKD1}, |t_{PLHD} - t_{PHLD}|, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
- (5) t_{SKD2}, Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
- (6) Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.
- (7) Measured on a clock edge with a histogram and an accumulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.
- (8) Measured on an eye diagram with a histogram and an accumulation of 3500 histogram hits. Input stimulus jitter is subtracted.

DC TEST CIRCUITS

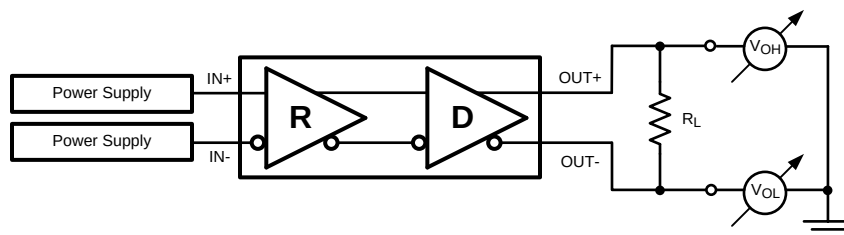


Figure 1. Differential Driver DC Test Circuit

AC Test Circuits and Timing Diagrams

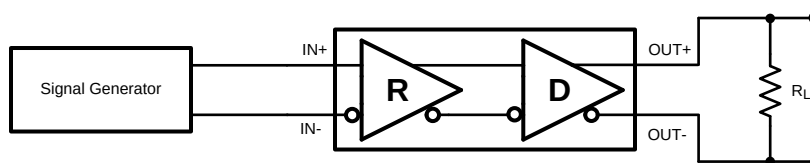


Figure 2. Differential Driver AC Test Circuit

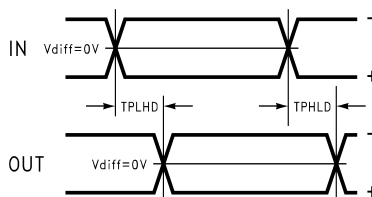


Figure 3. Propagation Delay Timing Diagram

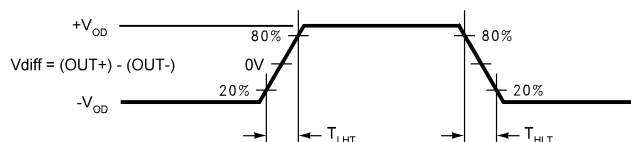


Figure 4. LVDS Output Transition Times

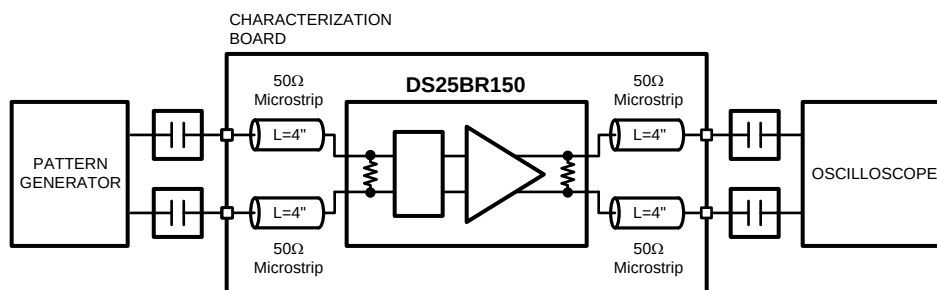


Figure 5. Jitter Measurements Test Circuit

Device Operation

INPUT INTERFACING

The DS25BR150 accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS25BR150 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the DS25BR150 inputs are internally terminated with a 100Ω resistor.

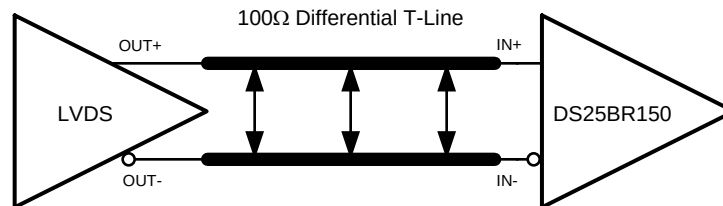


Figure 6. Typical LVDS Driver DC-Coupled Interface to DS25BR150 Input

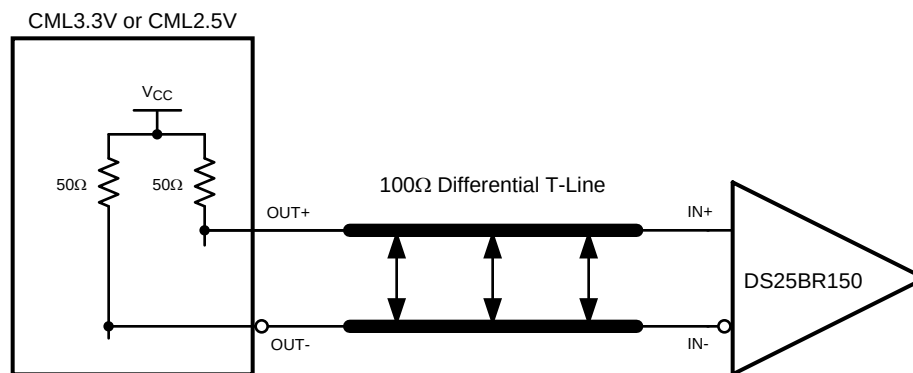


Figure 7. Typical CML Driver DC-Coupled Interface to DS25BR150 Input

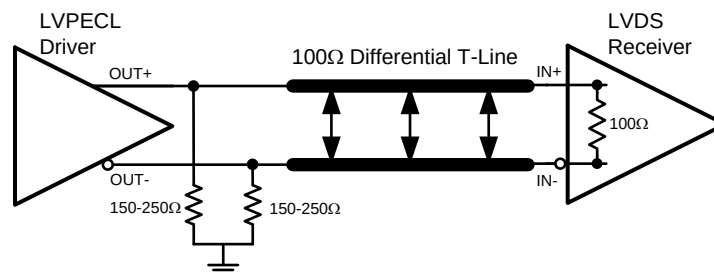


Figure 8. Typical LVPECL Driver DC-Coupled Interface to DS25BR150 Input

OUTPUT INTERFACING

The DS25BR150 outputs signals are compliant to the LVDS standard. It can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check the respective receiver's data sheet prior to implementing the suggested interface implementation.

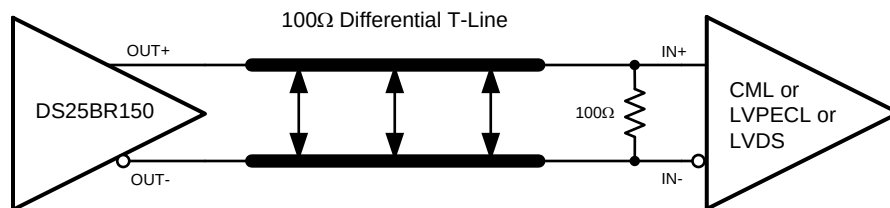


Figure 9. Typical DS25BR150 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

Typical Performance Characteristics

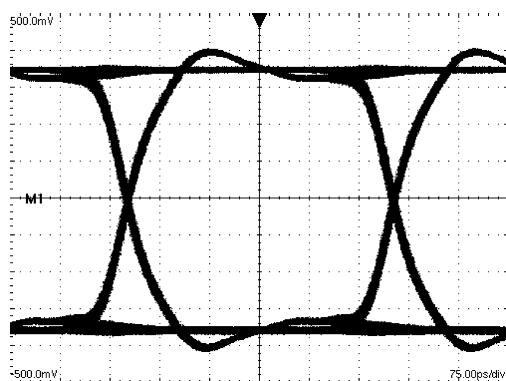


Figure 10. A 2.5 Gbps NRZ PRBS-7 Output Eye Diagram
V:100 mV / DIV, H:75 ps / DIV

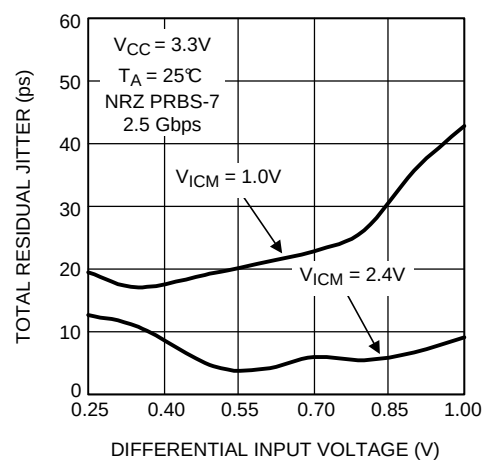


Figure 11. Total Jitter as a Function of Input Amplitude

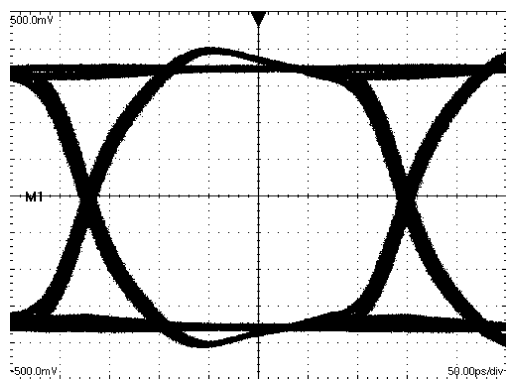


Figure 12. A 3.125 Gbps NRZ PRBS-7 Output Eye Diagram
V:100 mV / DIV, H:50 ps / DIV

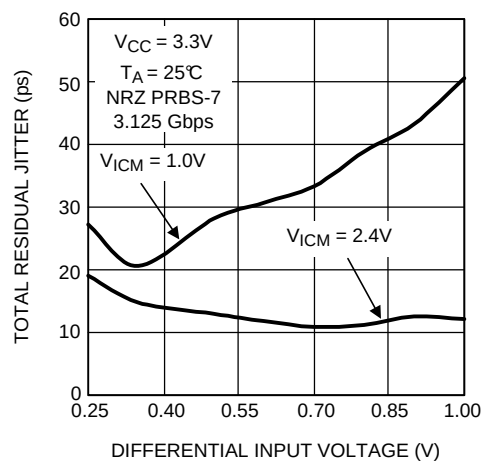


Figure 13. Total Jitter as a Function of Input Amplitude

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS25BR150TSD/NOPB	ACTIVE	WSO	NGQ	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	2R150	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

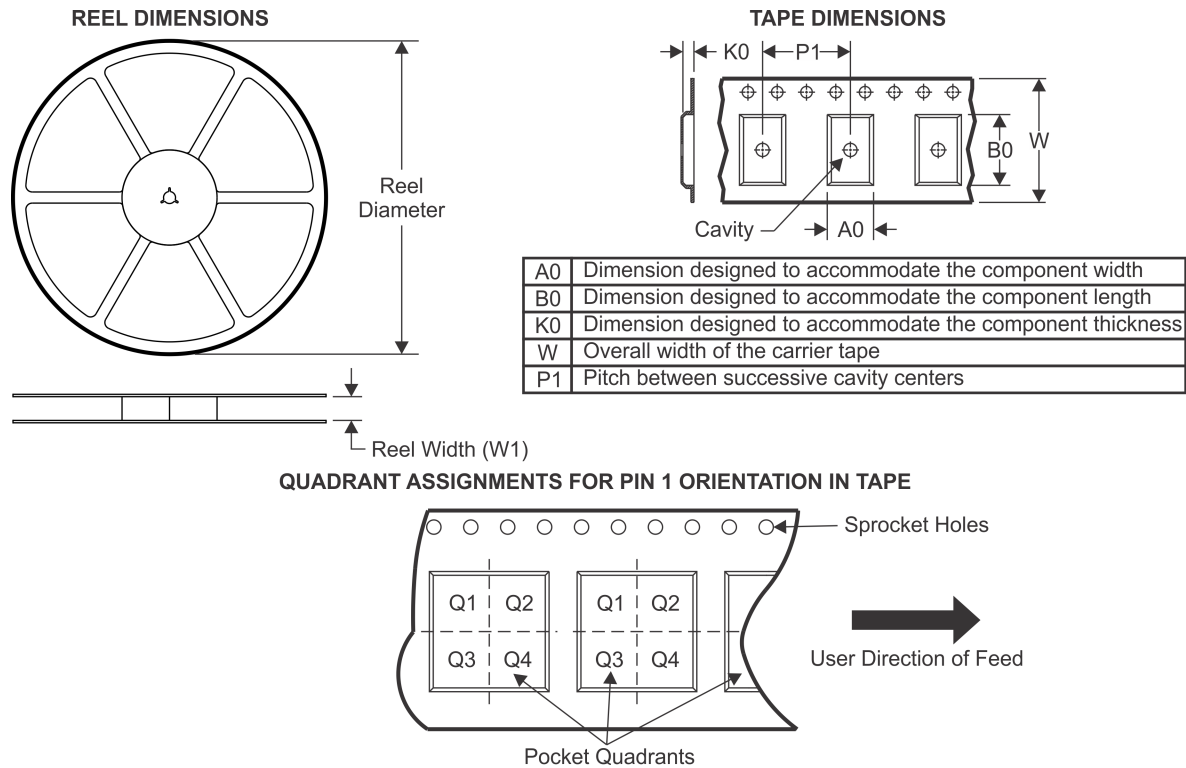
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

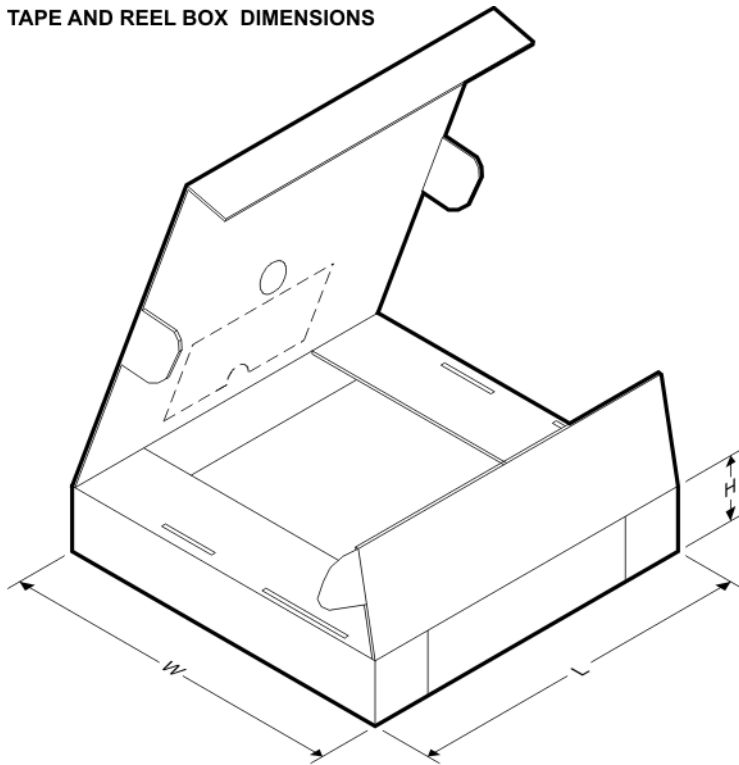
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS25BR150TSD/NOPB	WSO	NGQ	8	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

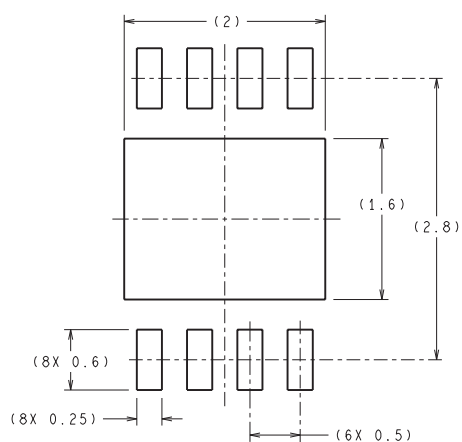
TAPE AND REEL BOX DIMENSIONS



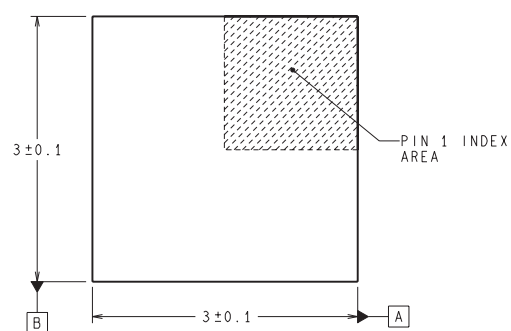
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS25BR150TSD/NOPB	WS0N	NGQ	8	1000	210.0	185.0	35.0

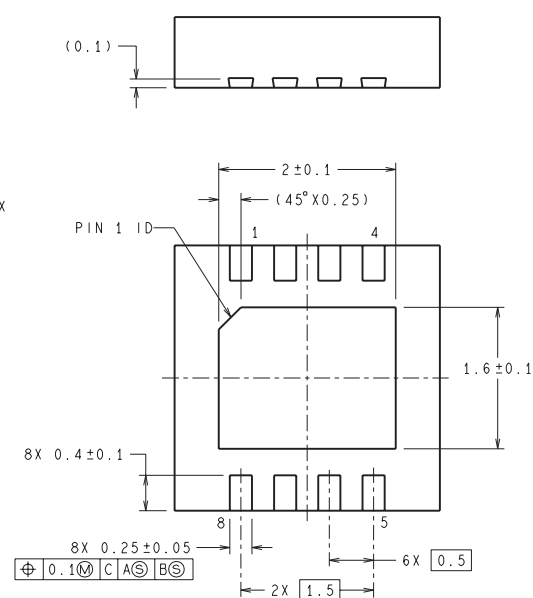
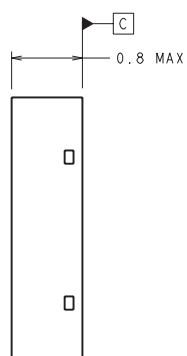
NGQ0008A



RECOMMENDED LAND PATTERN



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY



SDA08A (Rev A)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com