

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

## DESCRIPTION/ORDERING INFORMATION

This 12-bit to 24-bit bus exchanger is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74ALVCH16271 is intended for applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. This device is particularly suitable as an interface between conventional DRAMs and high-speed microprocessors.

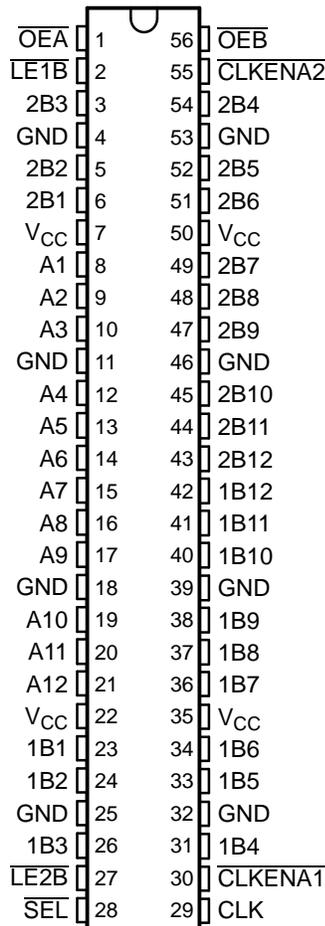
A data is stored in the internal A-to-B registers on the low-to-high transition of the clock (CLK) input, provided that the clock-enable ( $\overline{CLKENA}$ ) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port.

Transparent latches in the B-to-A path allow asynchronous operation to maximize memory access throughput. These latches transfer data when the latch-enable ( $\overline{LE}$ ) inputs are low. The select ( $\overline{SEL}$ ) line selects 1B or 2B data for the A outputs. Data flow is controlled by the active-low output enables ( $\overline{OEA}$ ,  $\overline{OEB}$ ).

To ensure the high-impedance state during power up or power down, the output enables should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

DGG OR DL PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP - DL	Tube	SN74ALVCH16271DL	ALVCH16271
		Tape and reel	SN74ALVCH16271DLR	
	TSSOP - DGG	Tape and reel	SN74ALVCH16271DGGR	ALVCH16271

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

**SN74ALVCH16271**  
**12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER**  
**WITH 3-STATE OUTPUTS**

SCES017G—JULY 1995—REVISED SEPTEMBER 2004

**FUNCTION TABLES**

**OUTPUT ENABLE**

INPUTS		OUTPUTS	
$\overline{OE\bar{A}}$	$\overline{OE\bar{B}}$	A	1B, 2B
H	H	Z	Z
H	L	Z	Active
L	H	Active	Z
L	L	Active	Active

**A-TO-B STORAGE ( $\overline{OE\bar{B}} = L$ )**

INPUTS				OUTPUTS	
$\overline{CLKEN\bar{A}1}$	$\overline{CLKEN\bar{A}2}$	CLK	A	1B	2B
H	H	X	X	1B <sub>0</sub> <sup>(1)</sup>	2B <sub>0</sub> <sup>(1)</sup>
L	X	↑	L	L	X
L	X	↑	H	H	X
X	L	↑	L	X	L
X	L	↑	H	A <sub>0</sub>	H

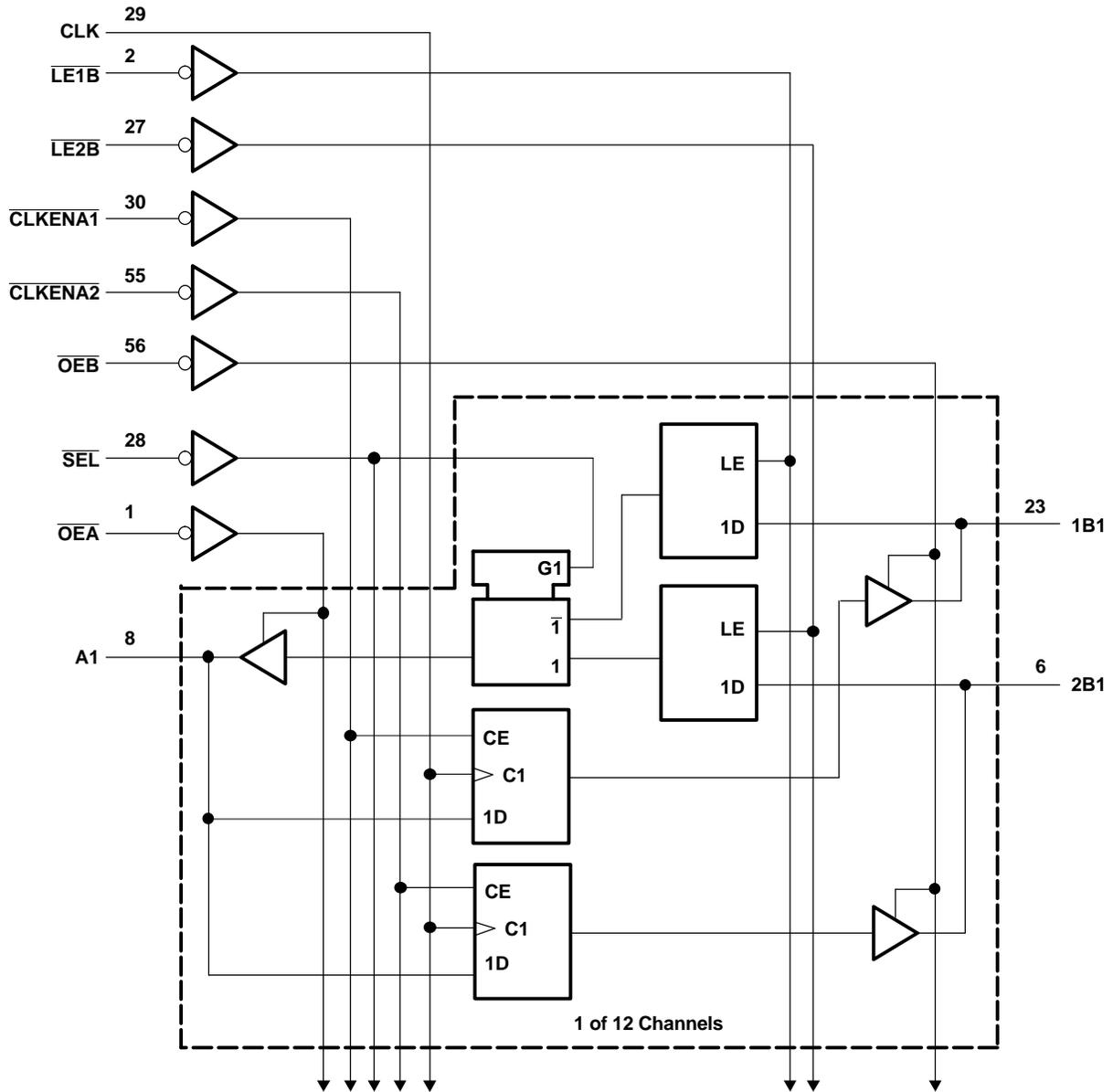
(1) Output level before the indicated steady-state input conditions were established

**B-TO-A STORAGE ( $\overline{OE\bar{A}} = L$ )**

INPUTS				OUTPUT A
$\overline{LE}$	$\overline{SEL}$	1B	2B	
H	X	X	X	A <sub>0</sub> <sup>(1)</sup>
H	X	X	X	A <sub>0</sub> <sup>(1)</sup>
L	H	L	X	L
L	H	H	X	H
L	L	X	L	L
L	L	X	H	H

(1) Output level before the indicated steady-state input conditions were established

**LOGIC DIAGRAM (POSITIVE LOGIC)**



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**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	4.6	V
V <sub>I</sub>	Input voltage range	Except I/O ports <sup>(2)</sup>		V
		I/O ports <sup>(2)(3)</sup>		
V <sub>O</sub>	Output voltage range <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50 mA
I <sub>O</sub>	Continuous output current			±50 mA
	Continuous current through each V <sub>CC</sub> or GND			±100 mA
θ <sub>JA</sub>	Package thermal impedance <sup>(4)</sup>	DGG package		64 °C/W
		DL package		56
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	1.65	3.6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		V
		V <sub>CC</sub> = 2.3 V to 2.7 V		
		V <sub>CC</sub> = 2.7 V to 3.6 V		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		V
		V <sub>CC</sub> = 2.3 V to 2.7 V		
		V <sub>CC</sub> = 2.7 V to 3.6 V		
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V		mA
		V <sub>CC</sub> = 2.3 V		
		V <sub>CC</sub> = 2.7 V		
		V <sub>CC</sub> = 3 V		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		mA
		V <sub>CC</sub> = 2.3 V		
		V <sub>CC</sub> = 2.7 V		
		V <sub>CC</sub> = 3 V		
Δt/Δv	Input transition rise or fall rate			10 ns/V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> - 0.2			V
	I <sub>OH</sub> = -4 mA	1.65 V	1.2			
	I <sub>OH</sub> = -6 mA	2.3 V	2			
	I <sub>OH</sub> = -12 mA	2.3 V	1.7			
		2.7 V	2.2			
		3 V	2.4			
I <sub>OH</sub> = -24 mA	3 V	2				
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.2	V
	I <sub>OL</sub> = 4 mA	1.65 V			0.45	
	I <sub>OL</sub> = 6 mA	2.3 V			0.4	
	I <sub>OL</sub> = 12 mA	2.3 V			0.7	
		2.7 V			0.4	
	I <sub>OL</sub> = 24 mA	3 V			0.55	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V			±5	μA
I <sub>I(hold)</sub>	V <sub>I</sub> = 0.58 V	1.65 V	25			μA
	V <sub>I</sub> = 1.07 V	1.65 V	-25			
	V <sub>I</sub> = 0.7 V	2.3 V	45			
	V <sub>I</sub> = 1.7 V	2.3 V	-45			
	V <sub>I</sub> = 0.8 V	3 V	75			
	V <sub>I</sub> = 2 V	3 V	-75			
	V <sub>I</sub> = 0 to 3.6 V <sup>(2)</sup>	3.6 V			±500	
I <sub>OZ</sub> <sup>(3)</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V			±10	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			40	μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	3.5		pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	9		pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

## TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	130		130		130		MHz
t <sub>w</sub>	Pulse duration, CLK high or low	3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time	A before CLK↑	2.6	2.1	1.7			ns
		B before $\overline{\text{LE}}$	1.7	1.5	1.3			
		$\overline{\text{CLKEN}}$ before CLK↑	1.6	1.3	1			
t <sub>h</sub>	Hold time	A after CLK↑	0.6	0.6	0.7			ns
		B after $\overline{\text{LE}}$	0.9	0.9	1.1			
		$\overline{\text{CLKEN}}$ after CLK↑	1	0.9	0.9			

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**SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>				130		130		130		MHz
t <sub>pd</sub>	CLK	B	8	1	6.2	5	1	4.3	ns	
	B	A	7	1	5.3	4.7	1.4	4		
	$\overline{LE}$		7	1	6	5.9	1.4	4.8		
	$\overline{SEL}$		7	1.1	6.4	6.2	1.3	5.2		
t <sub>en</sub>	$\overline{OE}B$ or $\overline{OE}A$	B or A	8	1	6	6.1	1	5.1	ns	
t <sub>dis</sub>	$\overline{OE}B$ or $\overline{OE}A$	B or A	7	1.4	5.4	4.6	1.7	4.2	ns	

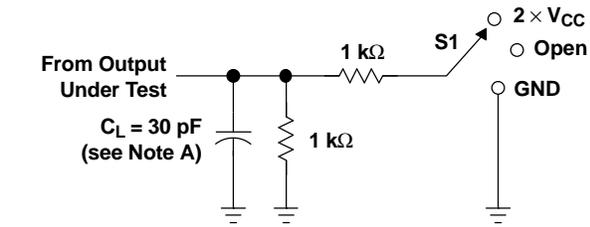
**OPERATING CHARACTERISTICS**

T<sub>A</sub> = 25°C

PARAMETER			TEST CONDITIONS	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
				TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance	A to B	Outputs enabled	92	105	pF
			Outputs disabled	61	76	
		B to A	Outputs enabled	39	43	
			Outputs disabled	11	13	

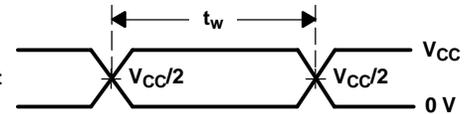
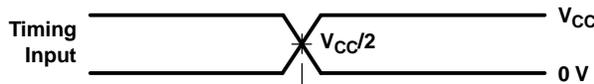
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8\text{ V}$

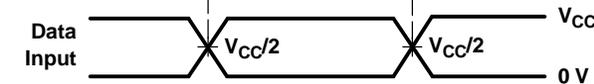


LOAD CIRCUIT

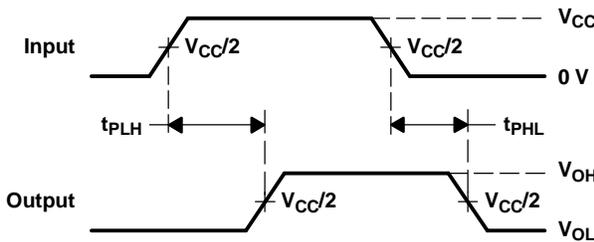
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



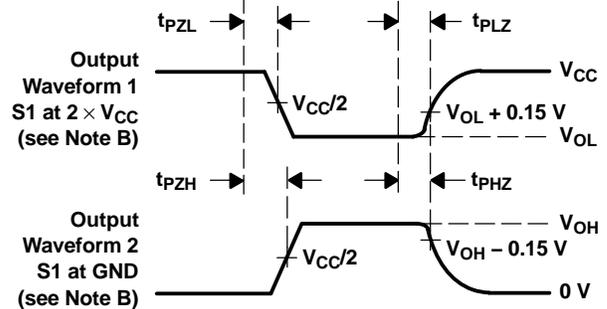
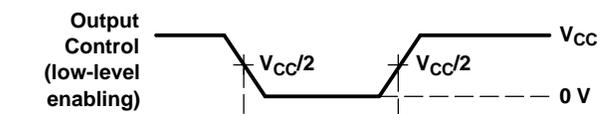
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



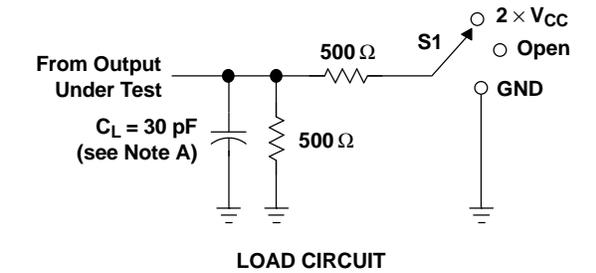
VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

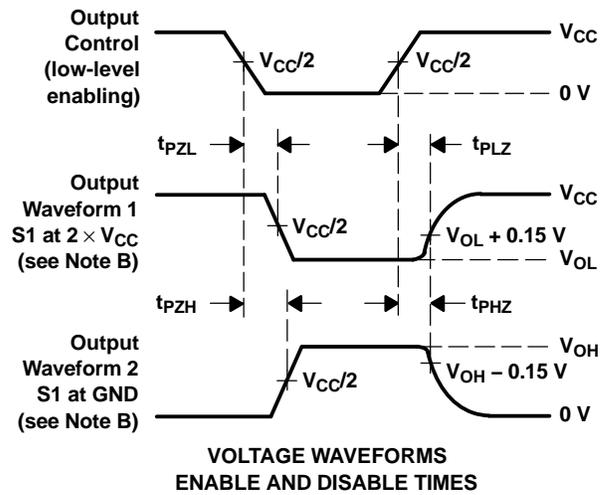
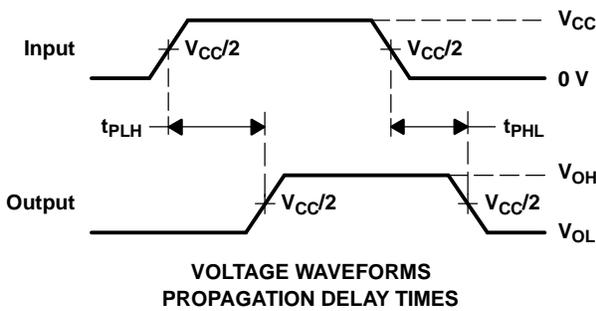
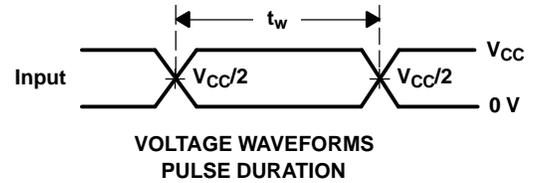
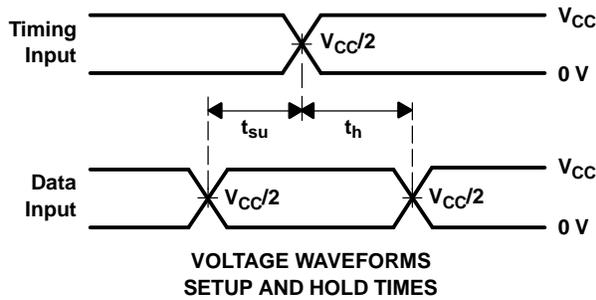
Figure 1. Load Circuit and Voltage Waveforms

**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

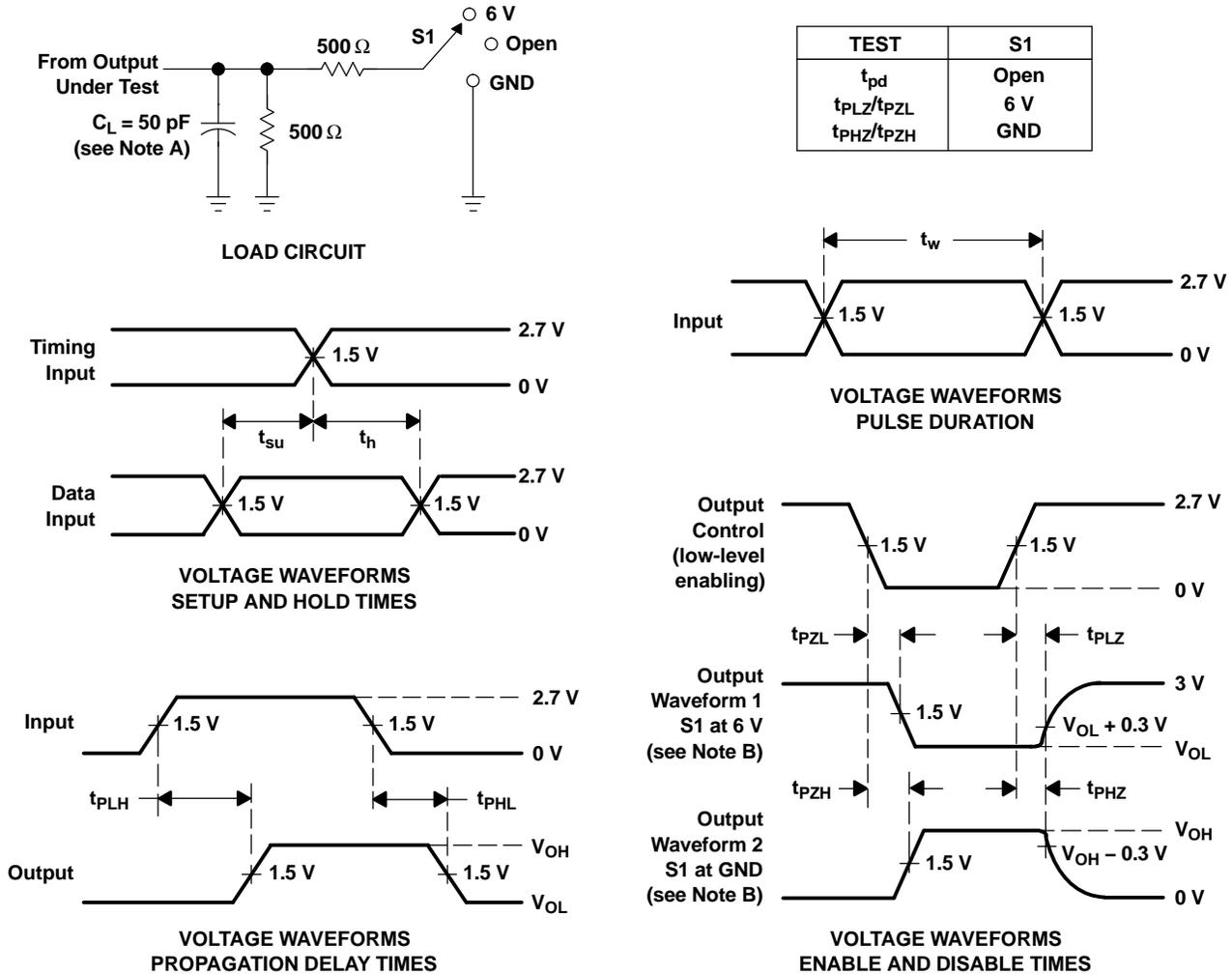


- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
D. The outputs are measured one at a time, with one transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 2. Load Circuit and Voltage Waveforms**

PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V}$  AND  $3.3\text{ V} \pm 0.3\text{ V}$



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 3. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74ALVCH16271DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16271	<a href="#">Samples</a>
SN74ALVCH16271DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCH16271	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

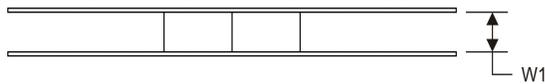
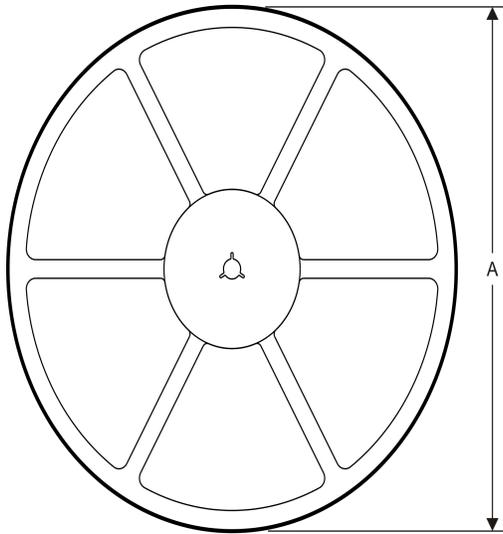
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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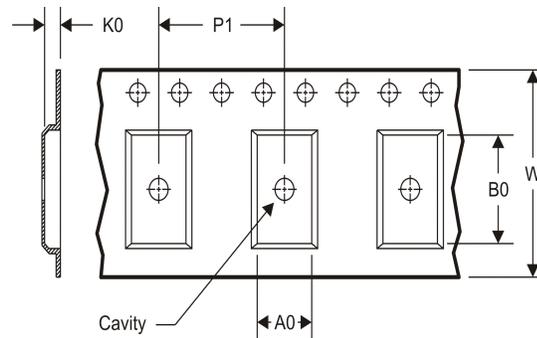
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



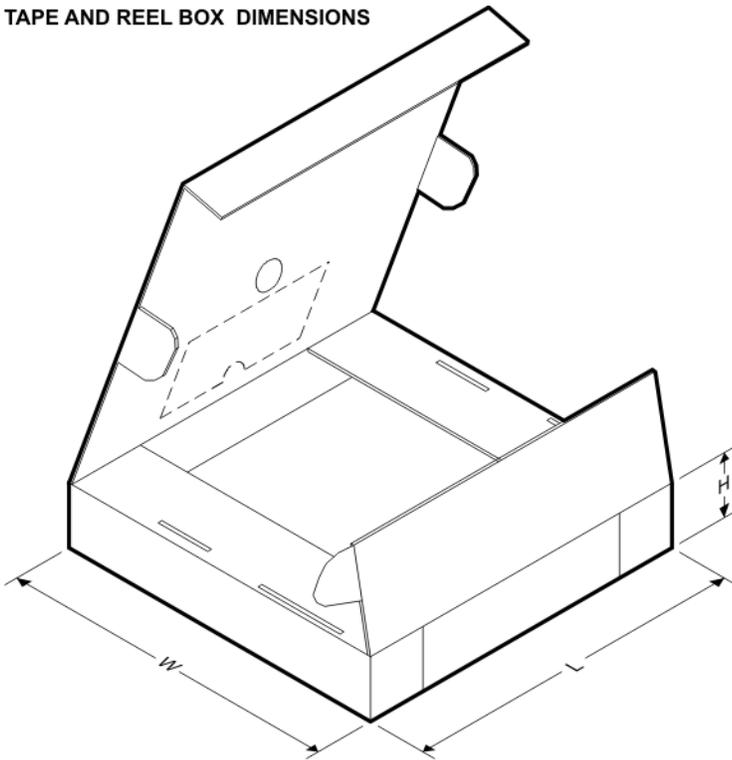
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH16271DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH16271DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0

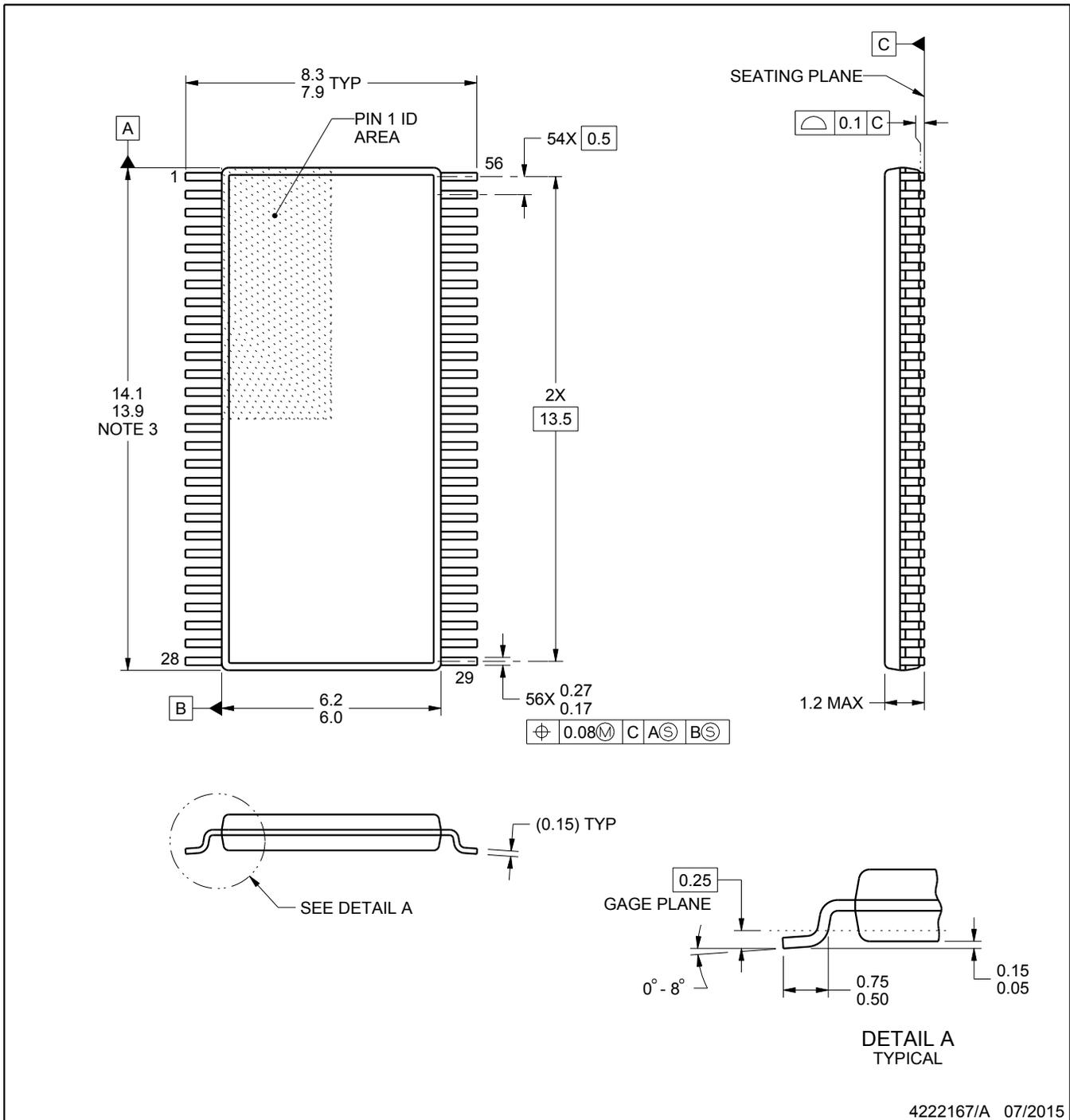
# DGG0056A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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### NOTES:

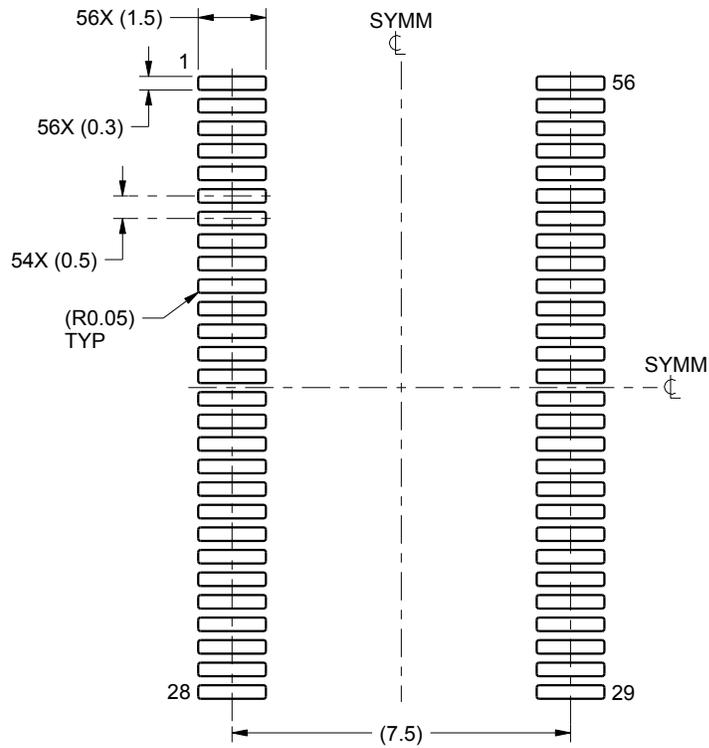
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

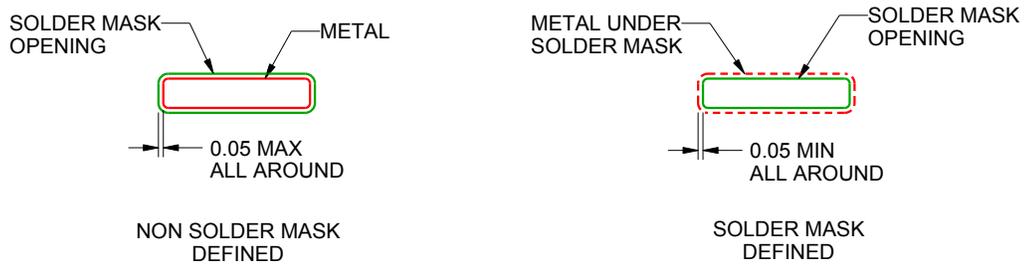
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

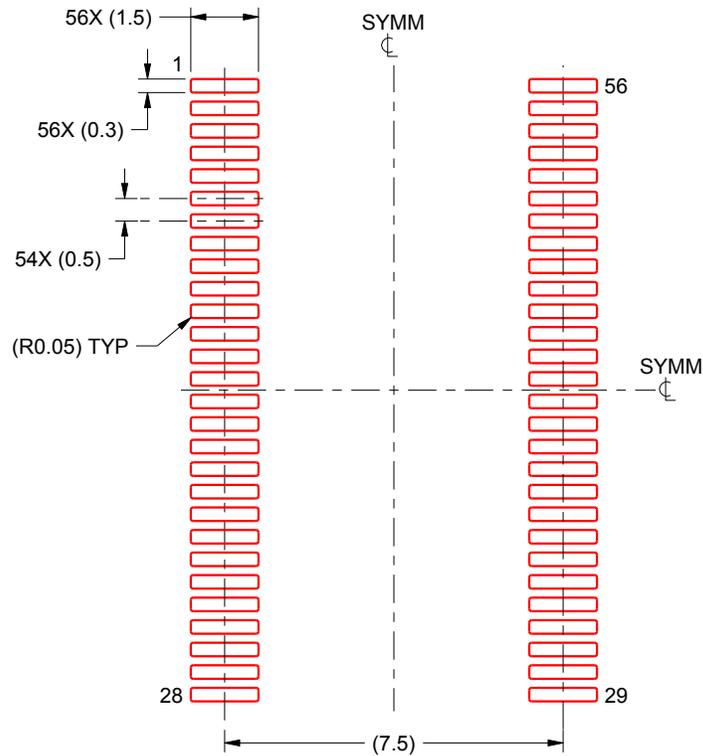
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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