155 Mbps to 4.25 Gbps Limiting Amplifier With LOS and RSSI

FEATURES

- **Multi-Rate Operation from 155 Mbps up to 4.25 Gbps**
- **89 mW Power Consumption**
- **Input Offset Cancellation**
- **High Input Dynamic Range**
- **Output Disable**
- **CML Data Outputs**
- **Receive Signal Strength Indicator (RSSI)**
- **Loss of Signal Detection**
- **Polarity Select**
- **Single 3.3-V Supply**
- **Surface Mount Small Footprint 3-mm × 3-mm 16-Pin QFN Package**
- **Pin-Compatible with the ONET2501PA and ONET3301PA**

APPLICATIONS

- **Multi-Rate OC3 to OC-48 FEC SONET/SDH Transmission Systems**
- **1.0625 Gbps, 2.125 Gbps, and 4.25 Gbps Fibre Channel Receivers**
- **Gigabit Ethernet Receivers**

DESCRIPTION

The ONET4201PA is a versatile high-speed, 3.3-V limiting amplifier for multiple fiber optic applications with data rates up to 4.25 Gbps.

This device provides a gain of about 50 dB, which ensures a fully differential output swing for input signals as low as 3 mV_{p-p}.

The high input signal dynamic range ensures low jitter output signals even when overdriven with input signal swings as high as 1200 mV_{p-p}.

The ONET4201PA provides a loss of signal detection as well as a received signal strength indicator.

The part is available in a small footprint 3-mm × 3-mm 16-pin QFN package and is pin-compatible with the ONET2501PA and ONET3301PA.

This power efficient limiting amplifier typically dissipates less than 89 mW and it is characterized for operation from –40°C to 85°C.

BLOCK DIAGRAM

A simplified block diagram of the ONET4201PA is shown in Figure 1.

This compact, low power 4.25 Gbps limiting amplifier consists of a high-speed data path with offset cancellation block, a loss of signal and RSSI detection block, and a bandgap voltage reference and bias current generation block.

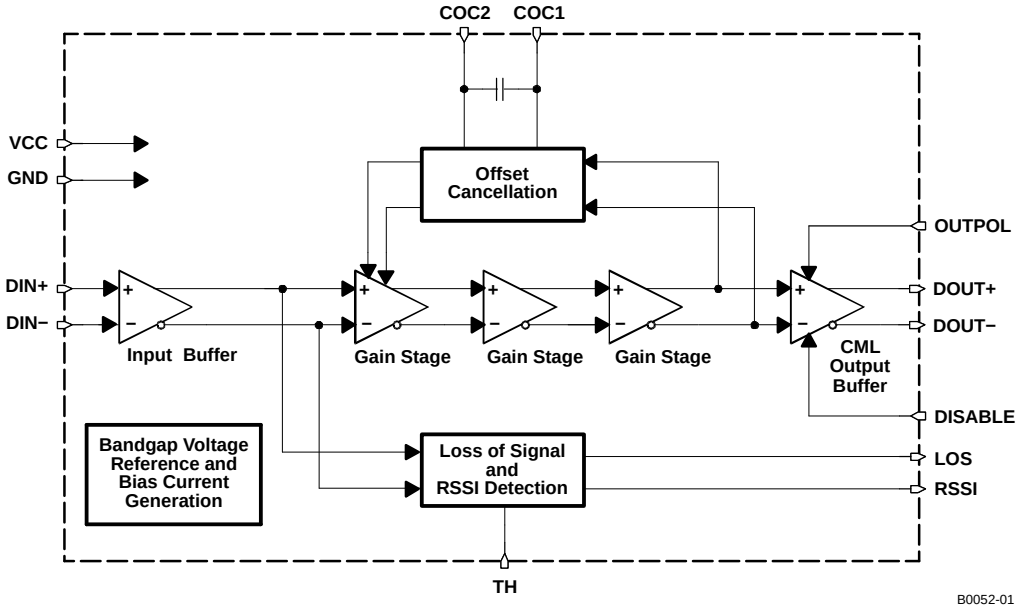

Figure 1. Simplified Block Diagram of the ONET4201PA

HIGH SPEED DATA PATH

The high-speed data signal is applied to the data path by means of the input signal pins DIN+/DIN–. The data path consists of the input stage with 2 × 50-Ω on-chip line termination to VCC, three gain stages, which provide the required typical gain of about 50 dB, and a CML output stage. The amplified data output signal is available at the output pins DOUT+/DOUT–, which provide 2 × 50-Ω back-termination to VCC. The output stage also includes a data polarity switching function, which is controlled by the OUTPOL input, and a disable function, controlled by the signal applied to the DISABLE input pin.

Offset cancellation compensates for internal offset voltages and thus ensures proper operation even for very small input data signals.

The low frequency cutoff is typically as low as 25 kHz with the built-in filter capacitor.

For applications which require even lower cutoff frequencies, an additional external filter capacitor may be connected to the COC1/COC2 pins.

LOSS OF SIGNAL AND RSSI DETECTION

The output signal of the input buffer is monitored by the loss of signal and RSSI detection circuitry. In this block a signal is generated that is linearly proportional to the input amplitude over a wide input voltage range. This signal is available at the RSSI output pin.

Furthermore, this circuit block compares the input signal to a threshold which can be programmed by means of an external resistor connected to the TH pin. If the input signal falls below the specified threshold, a loss of signal is indicated at the LOS pin.

The relation between the LOS assert voltage V_{AST} (in mV_{p-p}) and the external resistor R_{TH} (in kΩ) connected to the TH pin can be approximated as given below:

$$R_{TH} \approx \frac{20.8\ k\Omega}{\left(V_{AST}/mV_{p-p} - 1\right)} + 300\ \Omega \quad (1)$$

$$V_{AST} \approx \frac{20.8\ mV_{p-p}}{R_{TH}/k\Omega - 0.3} + 1\ mV_{p-p} \quad (2)$$

BANDGAP VOLTAGE AND BIAS GENERATION

The ONET4201PA limiting amplifier is supplied by a single 3.3-V±10% supply voltage connected to the VCC pins. This voltage is referred to ground (GND).

An on-chip bandgap voltage circuit generates a supply voltage independent reference from which all other internally required voltages and bias currents are derived.

PACKAGE

For the ONET4201PA a small footprint 3-mm × 3-mm 16-pin QFN package, with a lead pitch of 0,5 mm, is used. The pin out is shown in Figure 2.

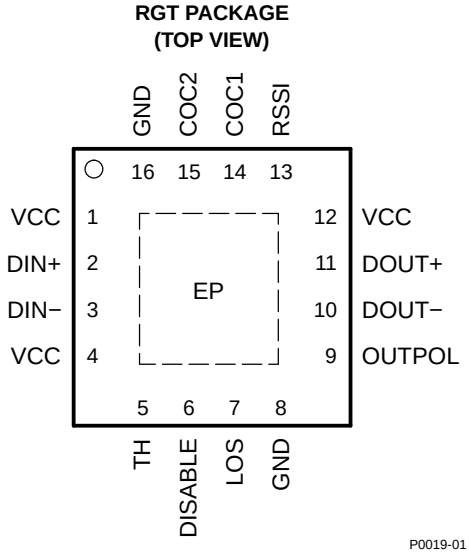

Figure 2. Pinout of ONET4201PA in a 3mm x 3mm 16 Pin QFN Package (Top View)

TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NO.	NAME		
1, 4, 12	VCC	supply	3.3-V ± 10% supply voltage
2	DIN+	analog-in	Non-inverted data input. On-chip 50-Ω terminated to VCC.
3	DIN–	analog-in	Inverted data input. On-chip 50-Ω terminated to VCC.
5	TH	analog-in	LOS threshold adjustment with resistor to GND.
6	DISABLE	CMOS-in	Disables CML output stage when set to high level.
7	LOS	CMOS-out	High level indicates that the input signal amplitude is below the programmed threshold level.
8, 16, EP	GND	supply	Circuit ground. Exposed die pad (EP) must be grounded.
9	OUTPOL	CMOS-in	Output data signal polarity select (internally pulled high). Setting to a high level or leaving the pin open selects normal polarity. Low level selects inverted polarity.
10	DOUT–	CML-out	Inverted data output. On-chip 50-Ω back-terminated toVCC.
11	DOUT+	CML-out	Non-inverted data output. On-chip 50-Ω back-terminated to VCC.

TERMINAL FUNCTIONS (continued)

TERMINAL		TYPE	DESCRIPTION
NO.	NAME		
13	RSSI	analog-out	Analog output voltage proportional to the input data amplitude. Indicates the strength of the received signal (RSSI).
14	COC1	analog	Offset cancellation filter capacitor terminal 1. Connect an additional filter capacitor between this pin and COC2 (pin 15). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15).
15	COC2	analog	Offset cancellation filter capacitor terminal 2. Connect an additional filter capacitor between this pin and COC1 (pin 14). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE/UNIT
V_{CC}	Supply voltage (2)	–0.3 V to 4.0 V
V_{DIN+}, V_{DIN-}	Voltage at DIN+, DIN–(2)	0.5 V to 4.0 V
V_{TH}, $V_{DISABLE}$, V_{LOS}, V_{OUTPOL}, V_{DOUT+}, $V_{DOUT–}$, V_{RSSI}, V_{COC1}, V_{COC2}	Voltage at TH, DISABLE, LOS, OUTPOL, DOUT+, DOUT-, RSSI, COC1, COC2 (2)	–0.3 V to 4.0 V
$V_{COC,DIFF}$	Differential voltage between COC1 and COC2	±1 V
$V_{DIN,DIFF}$	Differential voltage between DIN+ and DIN–	±2.5 V
I_{LOS}	Current into LOS	-1 to 9 mA
I_{DIN+}, $I_{DIN–}$, I_{DOUT+}, $I_{DOUT–}$	Continuous current at inputs and outputs	–25 mA to 25 mA
ESD	ESD rating at all pins	2 kV (HBM)
$T_{J(max)}$	Maximum junction temperature	125°C
T_{STG}	Storage temperature range	–65 to 85°C
T_A	Characterized free-air operating temperature range	–40 to 85°C
T_{LEAD}	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	–40		85	°C
V_{IH}	CMOS input high voltage	2.1			V
V_{IL}	CMOS input low voltage			0.6	V

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
I_{VCC}	Supply current	DISABLE = low (includes CML output current)		35	45	mA
		DISABLE = low (excludes CML output current)		27	35	
V_{OD}	Differential data output voltage swing	DISABLE = high		0.25	10	mV_{p-p}
		DISABLE = low, 5 $mV_{p-p} \le V_{IN} \le$ 1200 mV_{p-p}	520	760	1200	
R_{IN}, R_{OUT}	Data input/output resistance	Single-ended		50		Ω
	RSSI output voltage	Input = 8 mV_{p-p}, $R_{RSSI} \ge 10$ kΩ		200		mV
		Input = 80 mV_{p-p}, $R_{RSSI} \ge 10$ kΩ		1900		
	RSSI linearity	8 $mV_{p-p} \le V_{IN} \le 80$ mV_{p-p}		±3%		
$V_{IN(MIN)}$	Data input sensitivity	BER < 10^{-10}		3	5	mV_{p-p}
$V_{IN(MAX)}$	Data input overload		1200			mV_{p-p}
	LOS high voltage	I_{SOURCE} = 30 µA	2.4			V
	LOS low voltage	I_{SINK} = 1 mA			0.4	V

AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions, typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Low frequency –3 dB bandwidth	C_{OC} = open		25		kHz
		C_{OC} = 0.54 µF		0.8		
	Data rate		4.25			Gb/s
v_{NI}	Input referred noise			230		$µV_{RMS}$
DJ	Deterministic jitter	K28.5 pattern at 4.25 Gbps		3	19	ps_{p-p}
		K28.5 pattern at 2.125 Gbps		4	35	
		K28.5 pattern at 1.0625 Gbps		4	72	
RJ	Random jitter	Input = 5 mVpp		9		ps_{RMS}
		Input = 10 mVpp		4		
t_R	Output rise time	20% to 80%		45	85	ps
t_F	Output fall time	20% to 80%		45	85	ps
	LOS hysteresis	K28.5 pattern at 4.25 Gbps, 20log (V_{DEA}/V_{AST})	2.5	4.5		dB
R_{TH}	LOS threshold adjustment resistor range	See (1)	1.2		6.8	kΩ
V_{AST}	LOS assert voltage	R_{TH} = 2.5 kΩ, K28.5 pattern at 4.25 Gbps(1)		10		mV_{p-p}
		R_{TH} = 6.8 kΩ, K28.5 pattern at 4.25 Gbps(1)	2	5		
V_{DEA}	LOS de-assert voltage	R_{TH} = 2.5 kΩ, K28.5 pattern at 4.25 Gbps(1)		17		mV_{p-p}
		R_{TH} = 6.8 kΩ, K28.5 pattern at 4.25 Gbps(1)		8	20	
T_{LOS}	LOS assert/deassert time		2		100	µs
T_{DIS}	Disable response time			20		ns

(1) For a given external resistor connected to the TH pin the LOS assert voltage value may vary due to part-to-part variations. If high precision is required, adjustment of this resistor for each device is mandatory.

TYPICAL CHARACTERISTICS

Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted).

TRANSFER FUNCTION

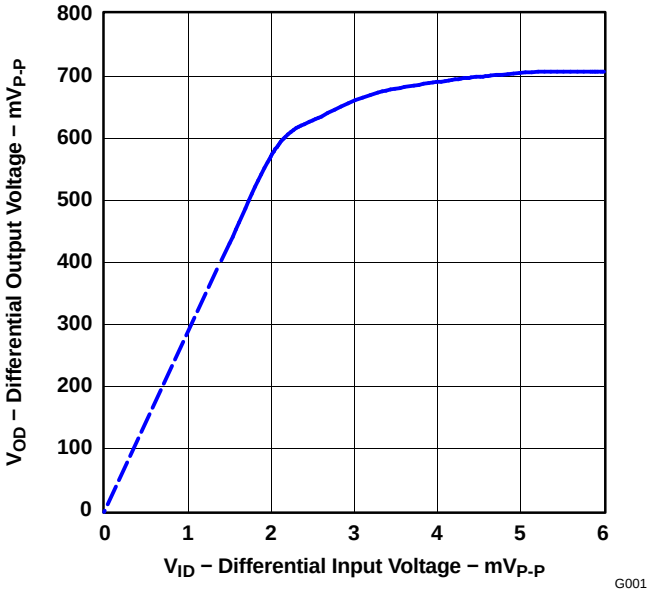

Figure 3.

RANDOM JITTER vs INPUT AMPLITUDE

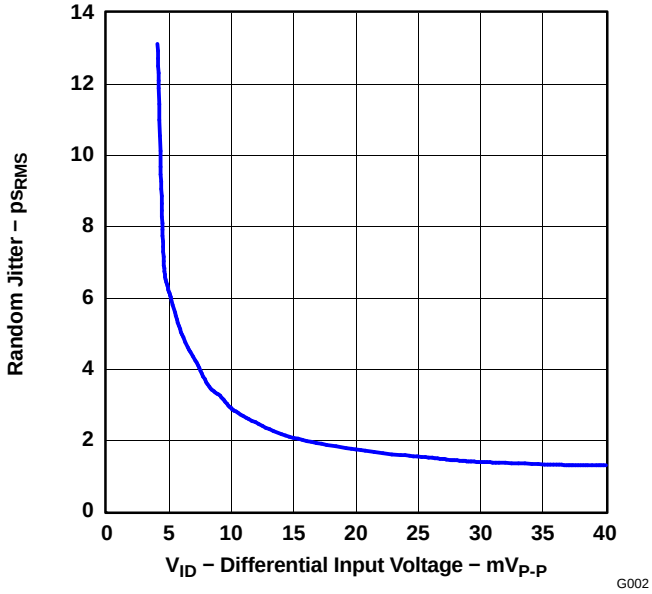

Figure 4.

BIT-ERROR RATIO INPUT AMPLITUDE

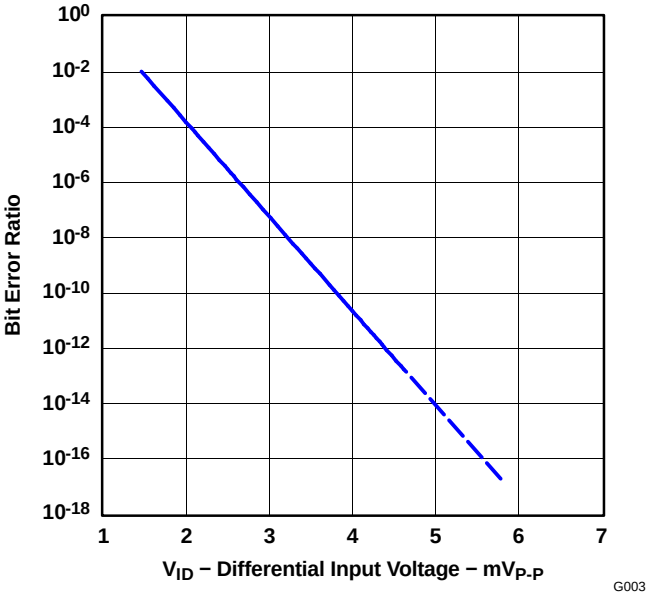

Figure 5.

FREQUENCY RESPONSE

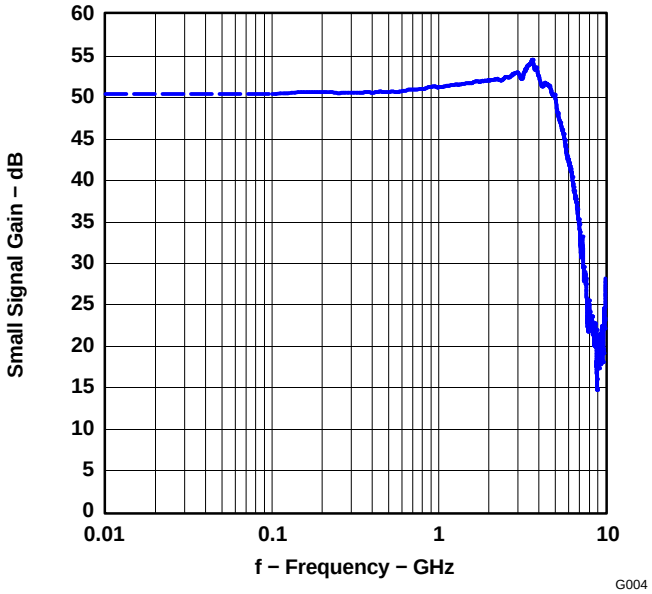

Figure 6.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted).

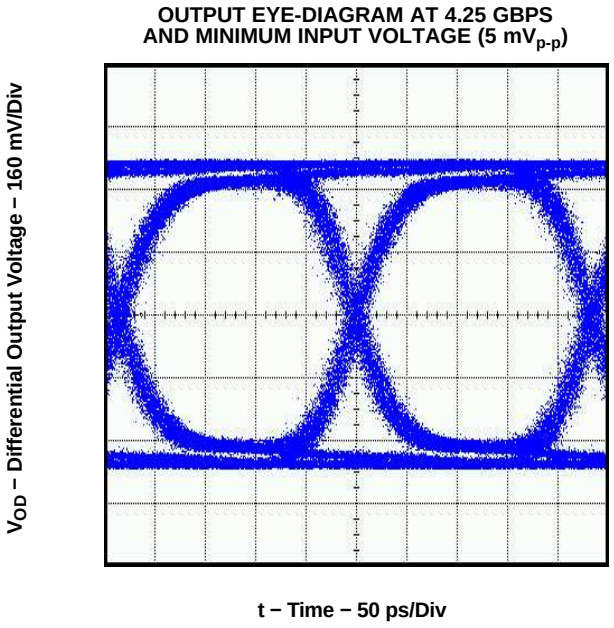

Figure 7.

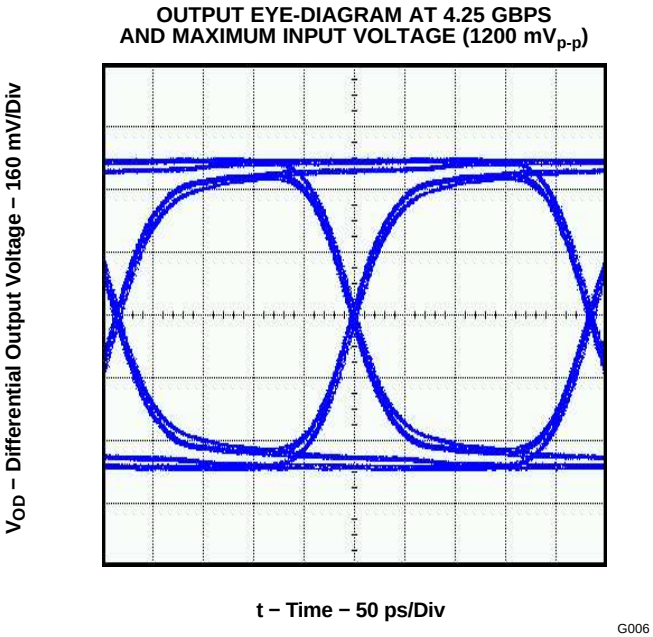

Figure 8.

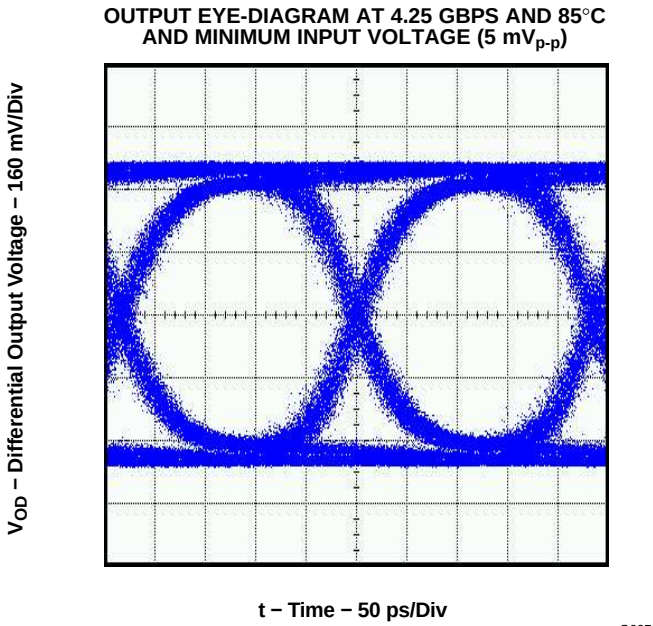

Figure 9.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted).

OUTPUT EYE-DIAGRAM AT 2.125 GBPS AND MINIMUM INPUT VOLTAGE (5 mV_{p-p})

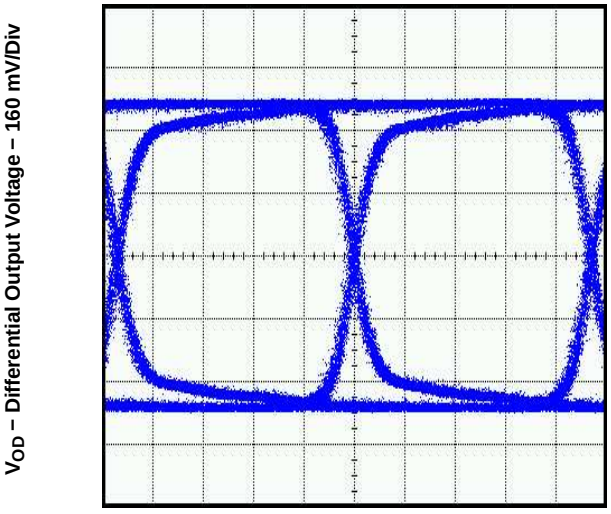

Figure 10.

OUTPUT EYE-DIAGRAM AT 2.125 GBPS AND MAXIMUM INPUT VOLTAGE (1200 mV_{p-p})

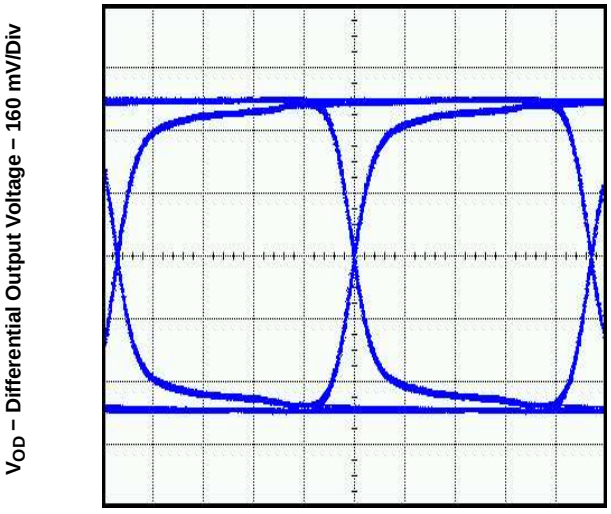

Figure 11.

OUTPUT EYE-DIAGRAM AT 1.0625 GBPS AND MINIMUM INPUT VOLTAGE (5 mV_{p-p})

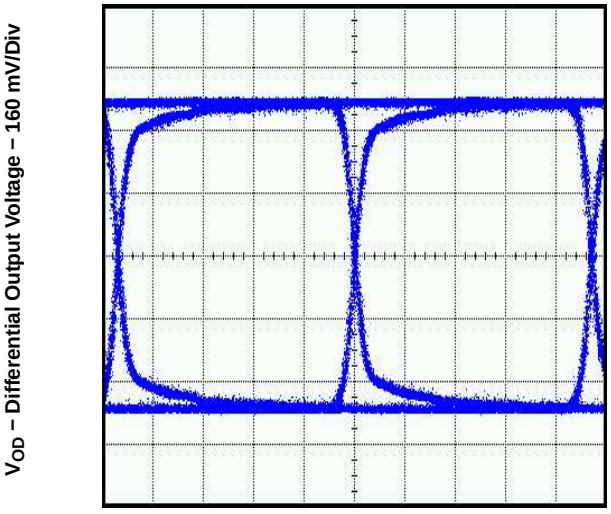

Figure 12.

OUTPUT EYE-DIAGRAM AT 1.0625 GBPS AND MAXIMUM INPUT VOLTAGE (1200 mV_{p-p})

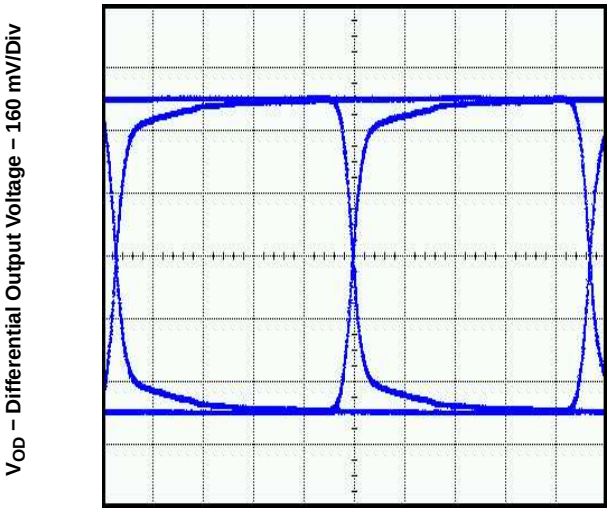

Figure 13.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted).

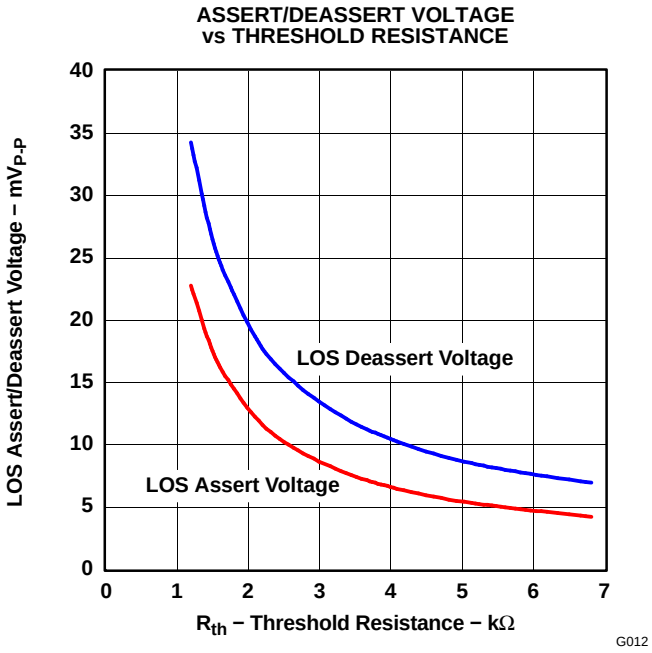

Figure 14.

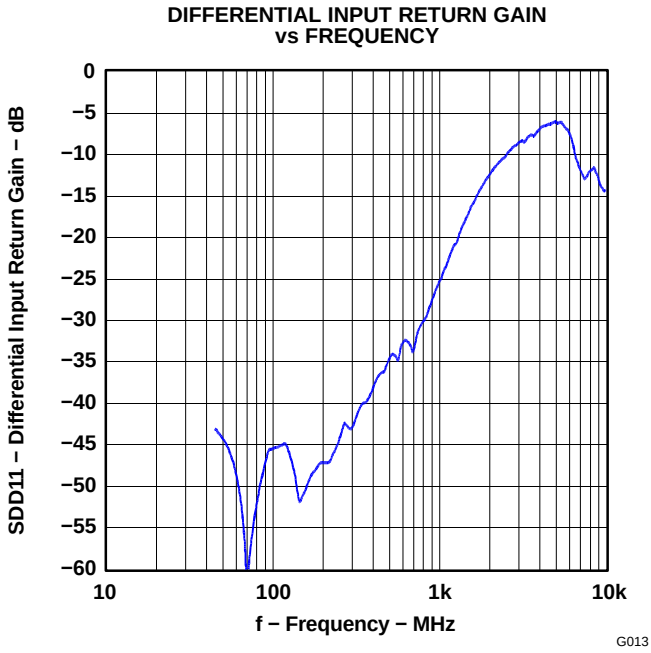

Figure 15.

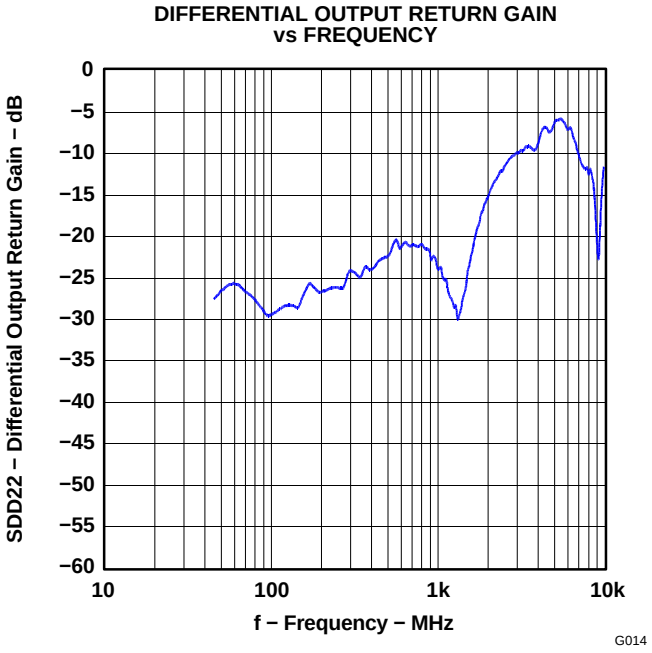

Figure 16.

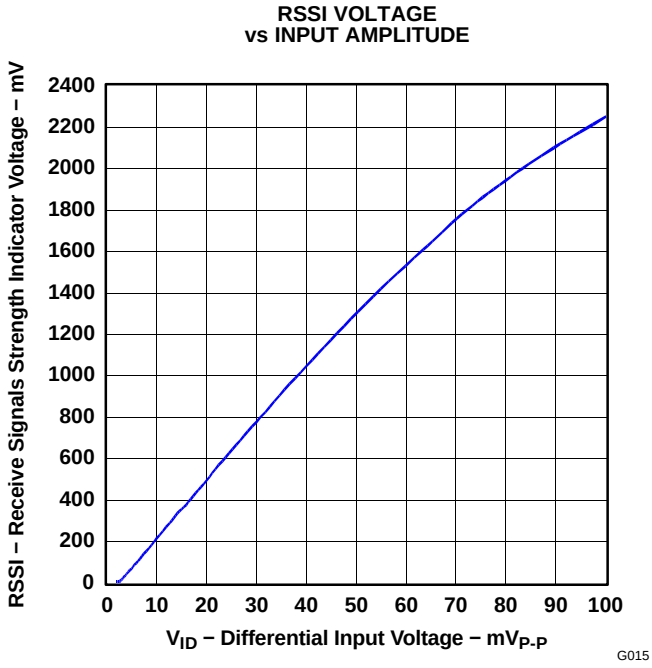

Figure 17.

APPLICATION INFORMATION

Figure 18 shows the ONET4201PA connected with an ac-coupled interface to the data signal source as well as to the output load.

Besides the ac-coupling capacitors C_1 through C_4 in the input and output data signal lines, the only required external component is the LOS threshold setting resistor R_{th}. In addition, an optional external filter capacitor (C_{OC}) may be used if a lower cutoff frequency is desired.

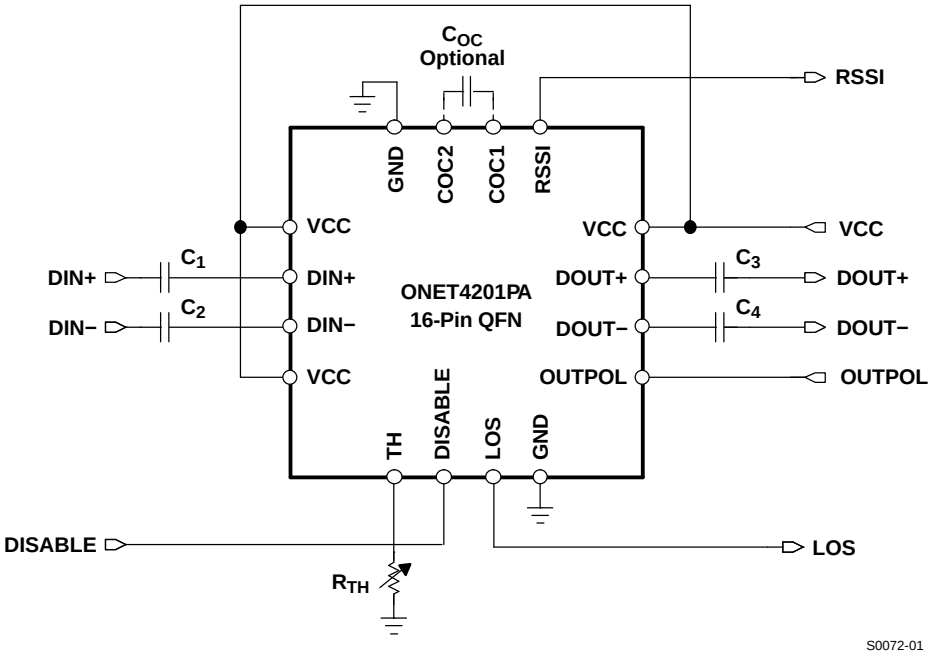

Figure 18. Basic Application Circuit With AC-Coupled I/Os

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ONET4201PARGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	401P	Samples
ONET4201PARGTRG4	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	401P	Samples
ONET4201PARGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	401P	Samples
ONET4201PARGTTG4	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	401P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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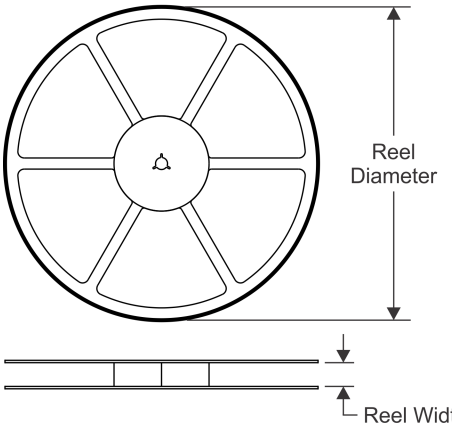
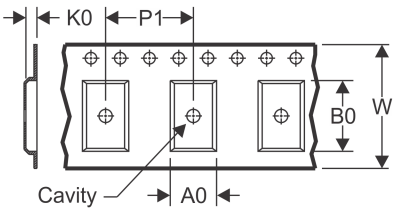
TAPE AND REEL INFORMATION

REEL DIMENSIONS

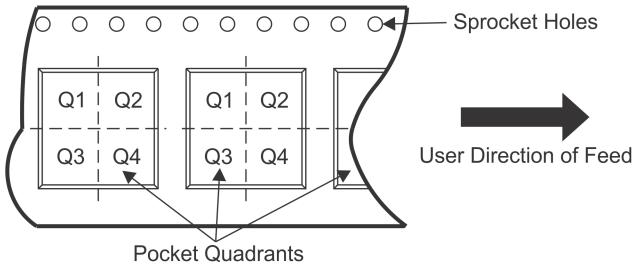


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

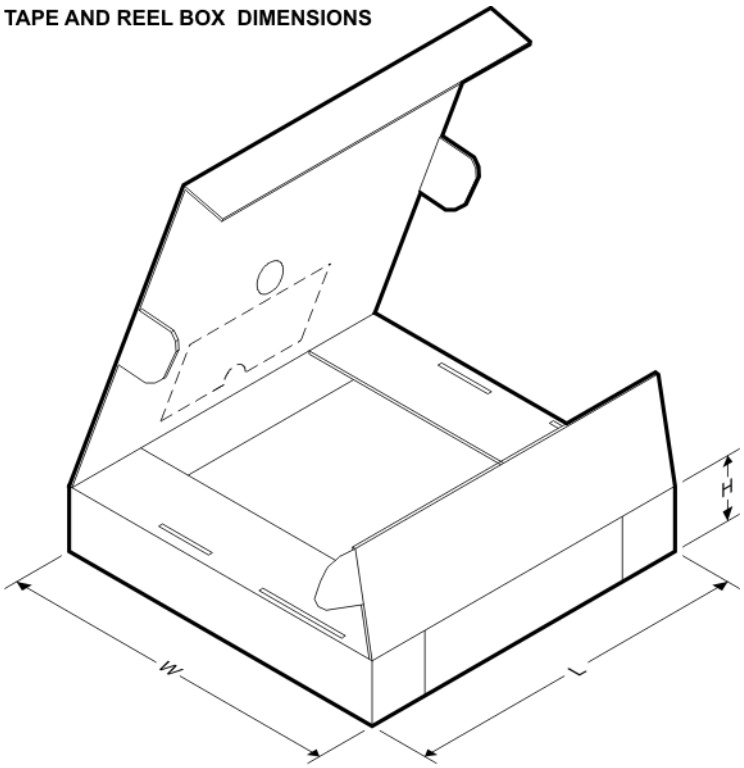
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ONET4201PARGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ONET4201PARGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

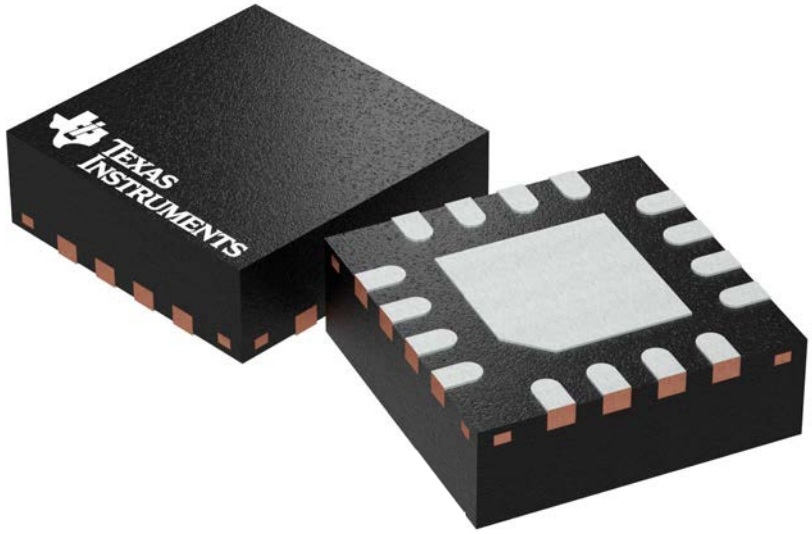


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ONET4201PARGTR	VQFN	RGT	16	3000	336.6	336.6	28.6
ONET4201PARGTT	VQFN	RGT	16	250	210.0	185.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



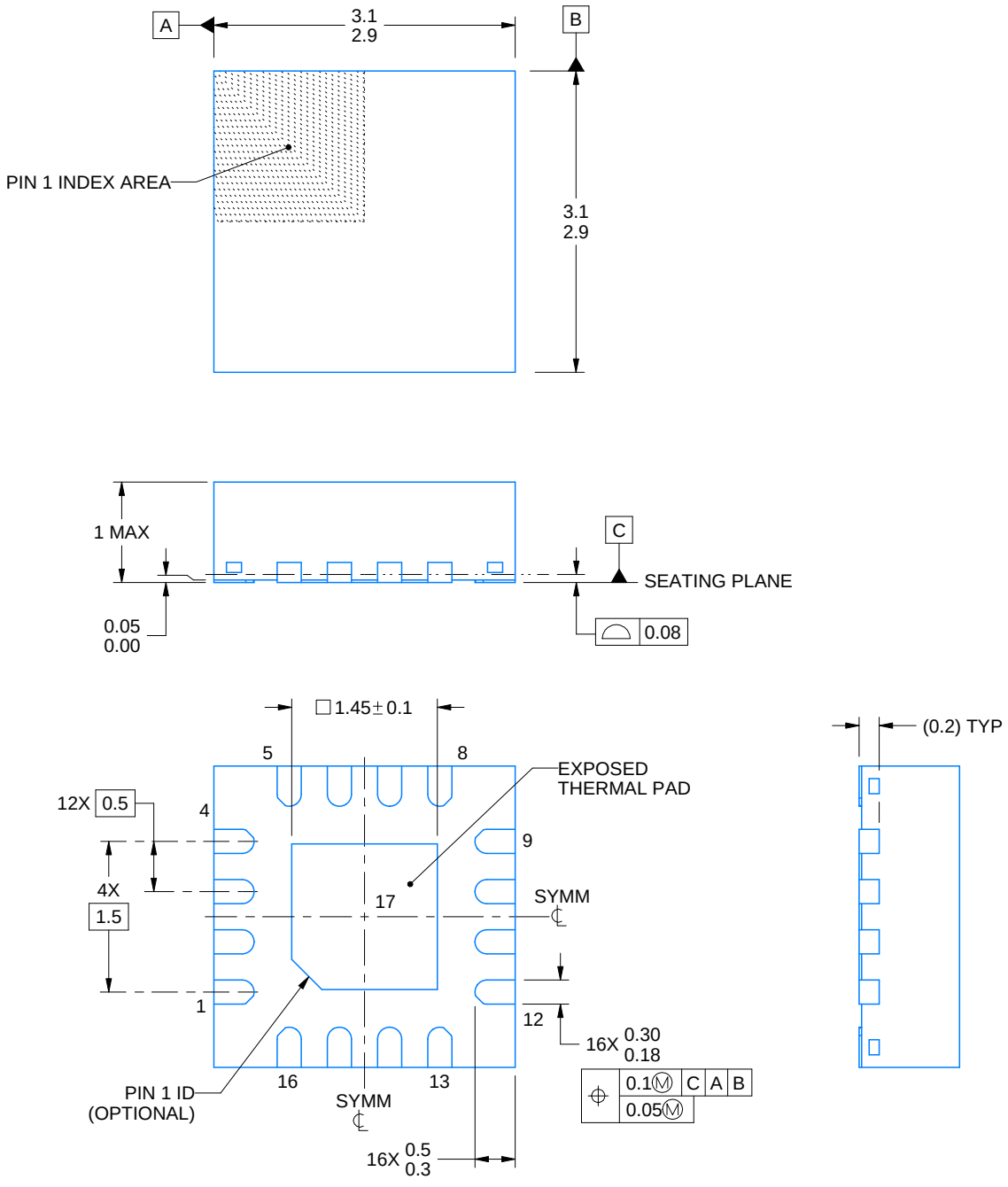
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT0016A

PACKAGE OUTLINE

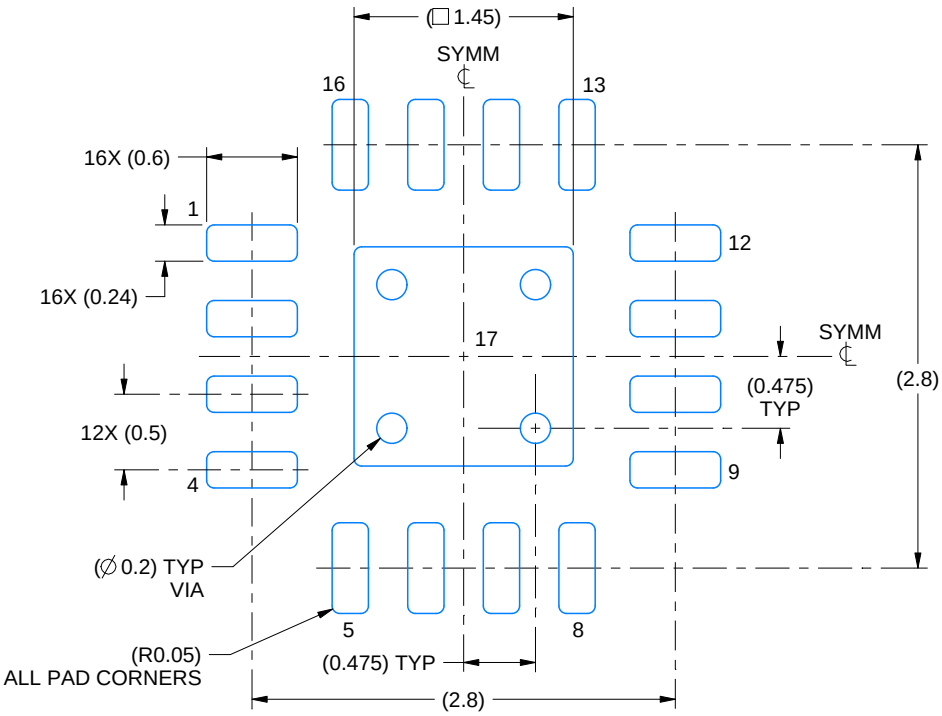
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

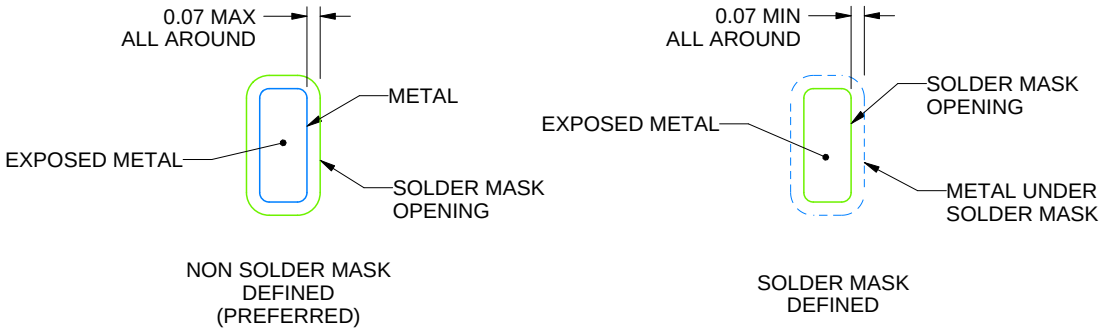


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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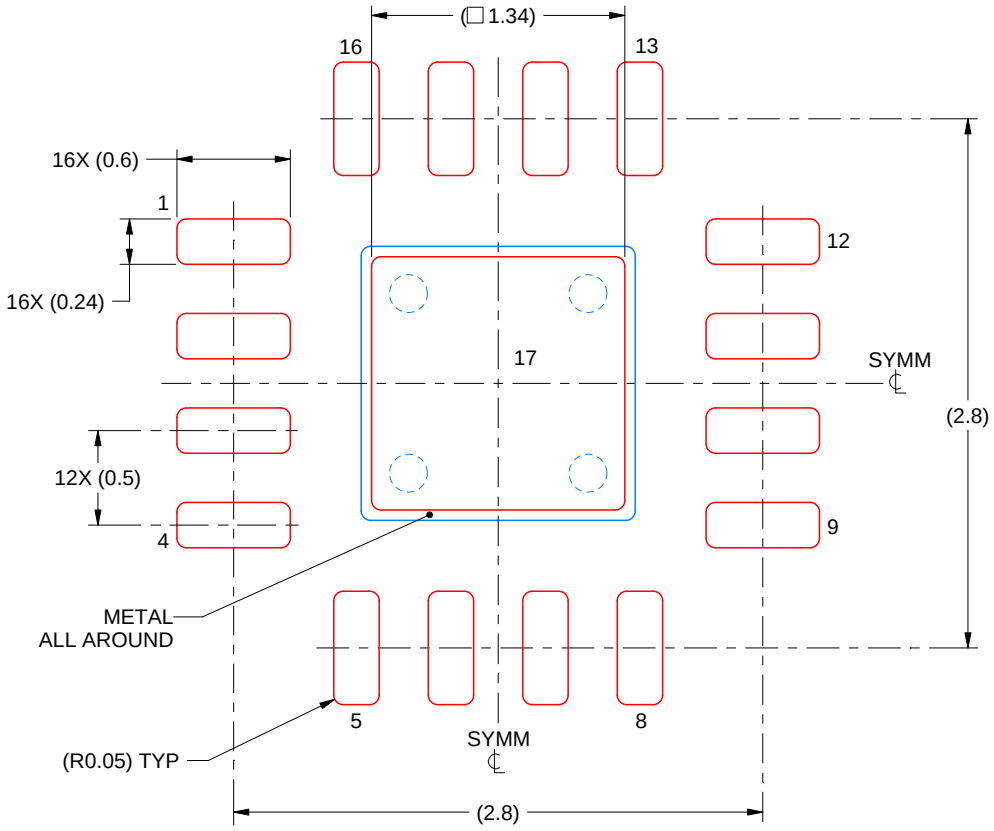
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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