TLV703x and TLV704x Small-Size, Nanopower, Low-Voltage Comparators

1 Features

- Ultra-small X2SON package (0.8 mm × 0.8 mm × 0.4 mm)
- Tiny 5-pin SOT-23, SC70, and VSSOP packages
- Wide supply voltage range of 1.6 V to 6.5 V
- Quiescent supply current of 315 nA
- Low propagation delay of 3 µs
- Rail-to-rail common-mode input voltage
- Internal hysteresis
- Push-pull output (TLV703x)
- Open-drain output (TLV704x)
- No phase reversal for overdriven inputs
- –40°C to 125°C Operating temperature

2 Applications

- Mobile phones and tablets
- Portable and battery-powered devices
- IR receivers
- Level translators
- Threshold detectors and discriminators
- Window comparators
- Rotary position encoders
- Zero-crossing detectors

3 Description

The TLV7031/TLV7041 (single-channel) and TLV7032/42 (dual-channel) are low-voltage, nanoPower comparators. These devices are available in an ultra-small, leadless package measuring 0.8 mm × 0.8 mm as well as standard 5-pin SC70 and SOT-23 packages, making them applicable for space-critical designs like smartphones, smart meters, and other portable or battery-powered applications.

The TLV703x and TLV704x offer an excellent combination of speed and power, with a propagation delay of 3 µs and a quiescent supply current of 315 nA. The benefit of fast response time at nanoPower enables power-conscious systems to monitor and respond quickly to fault conditions. With an operating voltage range of 1.6 V to 6.5 V, these comparators are compatible with 3-V and 5-V systems.

The TLV703x and TLV704x also ensure no output phase inversion with overdriven inputs and internal hysteresis, so engineers can use this family of comparators for precision voltage monitoring in harsh, noisy environments where slow-moving input signals must be converted into clean digital outputs.

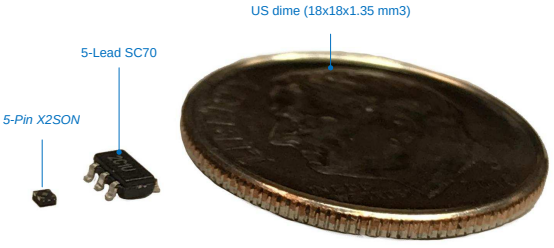
The TLV703x has a push-pull output stage capable of sinking and sourcing milliamps of current when controlling an LED or driving a capacitive load. The TLV704x has an open-drain output stage that can be pulled beyond V_{CC}, making it appropriate for level translators and bipolar to single-ended converters.

Device Information(1)

PART NUMBERS	PACKAGE (PINS)	BODY SIZE (NOM)
TLV7031, TLV7041	X2SON (5)	0.80 mm × 0.80 mm
	SC70 (5)	2.00 mm × 1.25 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
TLV7032, TLV7042	VSSOP (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

X2SON Package vs SC70 and US Dime



I_{CC} vs. Supply Voltage

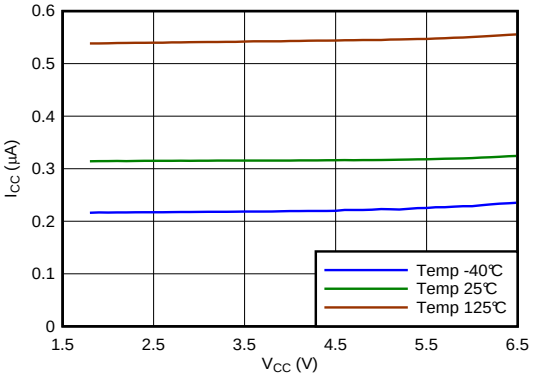


Table of Contents

4 Revision History

Changes from Revision D (April 2019) to Revision E — **Page**

- Changed VOH min from 4.7V to 4.65V for all package options in EC Table (Single) ... 6
- Changed VOL max from 300mV to 350mV for all package options in EC Table (Single) ... 6
- Deleted separate rows for VOH & VOL for DBV package options only in EC Table (Single) ... 6

Changes from Revision C (March 2019) to Revision D — **Page**

- Added separate rows for VOH & VOL for DBV package options in EC Table (Single) ... 6

Changes from Revision B (May 2018) to Revision C — **Page**

- Added dual channel versions in VSSOP package ... 1
- Changed TLV7031 to TLV703x and TLV7041 to TLV704x throughout the document ... 1
- Added dual channel versions ... 1
- Added Device Information dual channel versions in VSSOP package ... 1
- Deleted The SOT-23 package is in preview only ... 1

Changes from Revision A (January 2018) to Revision B — **Page**

- Changed the preview SC70 package to production data ... 1

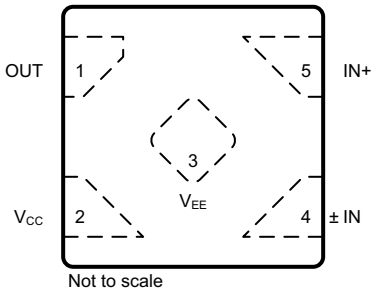
Changes from Original (September 2017) to Revision A — **Page**

- Changed data sheet title from: TLV7031/TLV7041 Small-Size, nanoPower, Low-Voltage Comparators to: TLV7031 and TLV7041 Small Size, nanopower, Low-Voltage Comparators ... 1
- Added Internal Hysteresis bullet to *Features* ... 1

- Specified which device has push-pull output and open-drain output options in *Features* 1
- Removed (TLV7031) from key graphic title because the graph covers both the TLV7031 and TLV7041 devices 1
- Added X2SON tablenote to *Pin Functions* table 4
- Changed Figure 2 10
- Added note to the *Timing Diagrams* section 10
- Smoothed Propagation Delay plots in Figure 31 through 11
- Changed vertical labels on Figure 20, Figure 21, Figure 17, and Figure 30 13
- Changed *Functional Block Diagram* 16
- Changed text 'the TLV7041 features an open-drain output stage enabling the output logic levels to be pulled up to an external source up to 7 V' to 'the TLV7041 features an open-drain output stage enabling the output logic levels to be pulled up to an external source up to 6.5 V' 17
- Changed Figure 36 20
- Added note to the *Layout Example* section 27
- Added *Documentation Support* section 28

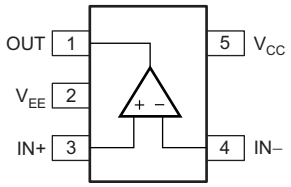
5 Pin Configuration and Functions

DPW Package
5-Pin X2SON
Top View



Not to scale

DBV and DCK Package
5-Pin SOT-23 and SC70
Top View

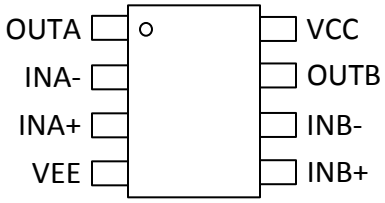


Pin Functions

PIN			I/O(1)	DESCRIPTION
X2SON(2)	SOT-23, SC70	NAME		
1	1	OUT	O	Output
2	5	V_{CC}	P	Positive (highest) power supply
3	2	V_{EE}	P	Negative (lowest) power supply
4	4	IN–	I	Inverting input
5	3	IN+	I	Noninverting input

(1) I = Input, O = Output, P = Power
(2) The application report *Designing and Manufacturing With TI's X2SON Packages* (SCEA055) provides more details on the optimal PCB designs.

DGK Package
8-Pin VSSOP
Top View



Pin Functions: TLV7032/42

PIN		I/O	DESCRIPTION
NAME	NO.		
INA–	2	I	Inverting input, channel A
INA+	3	I	Noninverting input, channel A
INB–	6	I	Inverting input, channel B
INB+	5	I	Noninverting input, channel B
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
VEE	4	—	Negative (lowest) supply or ground (for single-supply operation)
VCC	8	—	Positive (highest) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage $V_S = V_{CC} - V_{EE}$	–0.3	7	V
Input pins (IN+, IN-)(2)	V_{EE} – 0.3	7	V
Current into Input pins (IN+, IN-)		±10	mA
Output (OUT) (TLV703x)(3)	V_{EE} – 0.3	V_{CC} + 0.3	V
Output (OUT) (TLV704x)	V_{EE} – 0.3	7	V
Output short-circuit duration(4)		10	s
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to V_{EE}. Input signals that can swing 0.3V below V_{EE} must be current-limited to 10mA or less
(3) Output maximum is (V_{CC} + 0.3 V) or 7 V, whichever is less.
(4) Short-circuit to ground, one comparator per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage $V_S = V_{CC} – V_{EE}$	1.6	6.5	V
Input voltage range	V_{EE} – 0.1	V_{CC} + 0.1	V
Ambient temperature, T_A	–40	125	°C

6.4 Thermal Information (Dual)

THERMAL METRIC(1)		TLV7032/TLV7042 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	211.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	133.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	28.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	131.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Thermal Information (Single)

THERMAL METRIC[1]		TLV7031/TLV7041			UNIT
		DPW (X2SON)	DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	533.2	297.2	278.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	302.7	224.7	186.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	408.3	200.1	113.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	71.5	141.2	82.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	405.9	198.9	112.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	188.3	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics (Dual)

V_S = 1.8 V to 5 V, V_{CM} = V_S / 2; minimum and maximum values are at T_A = –40°C to +125°C (unless otherwise noted). Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input Offset Voltage	V_S = 1.8 V and 5 V, V_{CM} = VS / 2		±0.1	±8	mV
V_{HYS}	Hysteresis	V_S = 1.8 V and 5 V, V_{CM} = VS / 2	3	10	25	mV
V_{CM}	Common-mode voltage range		V_{EE}		V_{CC} + 0.1	V
I_B	Input bias current			2		pA
I_{OS}	Input offset current			1		pA
V_{OH}	Output voltage high (for TLV7032 only)	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA	4.65	4.8		V
V_{OL}	Output voltage low	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA		250	350	mV
I_{LKG}	Open-drain output leakage current (TLV7042 only)	V_S = 5 V, V_{ID} = +0.1 V (output high), V_{PULLUP} = V_{CC}		100		pA
CMRR	Common-mode rejection ratio	V_{EE} < V_{CM} < V_{CC}, V_S = 5 V		73		dB
PSRR	Power supply rejection ratio	V_S = 1.8 V to 5 V, V_{CM} = V_S / 2		77		dB
I_{SC}	Short-circuit current	VS = 5 V, sourcing (for TLV7032 only)		29		mA
		VS = 5 V, sinking		33		
I_{CC}	Supply current / Channel	V_S = 1.8 V, no load, V_{ID} = –0.1 V (Output Low)		315	750	nA

6.7 Switching Characteristics (Dual)

Typical values are at T_A = 25°C, V_S = 5 V, V_{CM} = V_S / 2; CL = 15 pF, input overdrive = 100 mV (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low (RP = 4.99 kΩ TLV7042 only) (1)	Midpoint of input to midpoint of output, V_{OD} = 100 mV		3		µs
t_{PLH}	Propagation delay time, low-to high (RP = 4.99 kΩ TLV7042 only) (1)	Midpoint of input to midpoint of output, V_{OD} = 100 mV		3		µs
t_R	Rise time (TLV7032 only)	Measured from 20% to 80%		4.5		ns
t_F	Fall time	Measured from 20% to 80%		4.5		ns
t_{ON}	Power-up time	During power on, V_{CC} must exceed 1.6V for 200 µs before the output will reflect the input..		200		µs

(1) The lower limit for RP is 650 Ω

6.8 Electrical Characteristics (Single)

V_S = 1.8 V to 5 V, V_{CM} = V_S / 2; minimum and maximum values are at T_A = –40°C to +125°C (unless otherwise noted). Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input Offset Voltage	V_S = 1.8 V and 5 V, V_{CM} = VS / 2		±0.1	±8	mV
V_{HYS}	Hysteresis	V_S = 1.8 V and 5 V, V_{CM} = VS / 2, T_A = 25°C	2	7	17	mV
V_{CM}	Common-mode voltage range		V_{EE}		V_{CC} + 0.1	V
I_B	Input bias current			2		pA
I_{OS}	Input offset current			1		pA
V_{OH}	Output voltage high (for TLV7031 only)	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA	4.65	4.8		V
V_{OL}	Output voltage low	V_S = 5 V, V_{EE} = 0 V, I_O = 3 mA		250	350	mV
I_{LKG}	Open-drain output leakage current (TLV7041 only)	V_S = 5 V, V_{ID} = +0.1 V (output high), V_{PULLUP} = V_{CC}		100		pA
CMRR	Common-mode rejection ratio	V_{EE} < V_{CM} < V_{CC}, V_S = 5 V		73		dB
PSRR	Power supply rejection ratio	V_S = 1.8 V to 5 V, V_{CM} = V_S / 2		77		dB
I_{SC}	Short-circuit current	VS = 5 V, sourcing		29		mA
		VS = 5 V, sinking		33		
I_{CC}	Supply current	V_S = 1.8 V, no load, V_{ID} = –0.1 V (Output Low)		335	900	nA

6.9 Switching Characteristics (Single)

Typical values are at T_A = 25°C, V_S = 5 V, V_{CM} = V_S / 2; CL = 15 pF, input overdrive = 100 mV (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low (RP = 2.5 kΩ TLV7041 only)	Midpoint of input to midpoint of output, V_{OD} = 100 mV		3		µs
t_{PLH}	Propagation delay time, low-to high (RP = 2.5 kΩ TLV7041 only)	Midpoint of input to midpoint of output, V_{OD} = 100 mV		3		µs
t_R	Rise time (TLV7031 only)	Measured from 10% to 90%		4.5		ns
t_F	Fall time	Measured from 10% to 90%		4.5		ns
t_{ON}	Power-up time	During power on, V_{CC} must exceed 1.6V for 200 µs before the output will reflect the input.		200		µs

6.10 Timing Diagrams

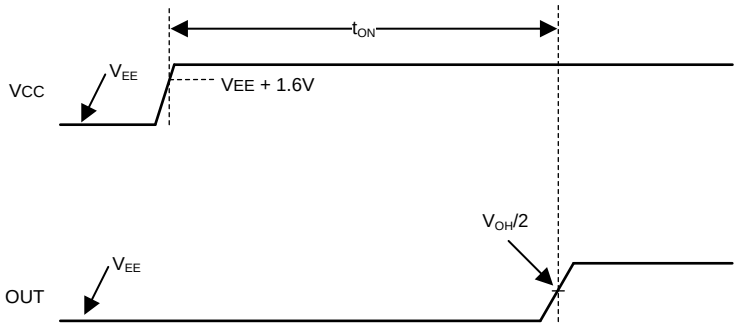


Figure 1. Start-Up Time Timing Diagram (IN+ > IN–)

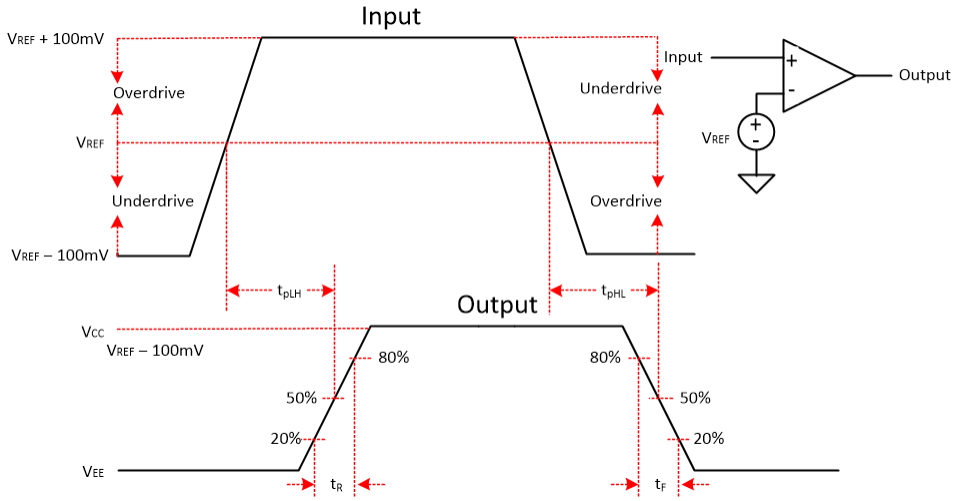


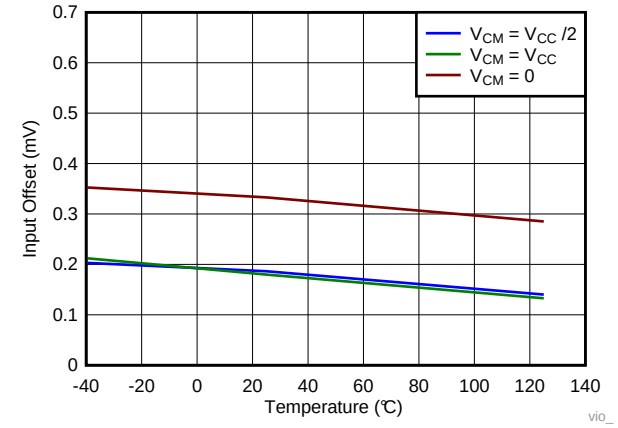
Figure 2. Propagation Delay Timing Diagram

NOTE

The propagation delays t_{pLH} and t_{pHL} include the contribution of input offset and hysteresis.

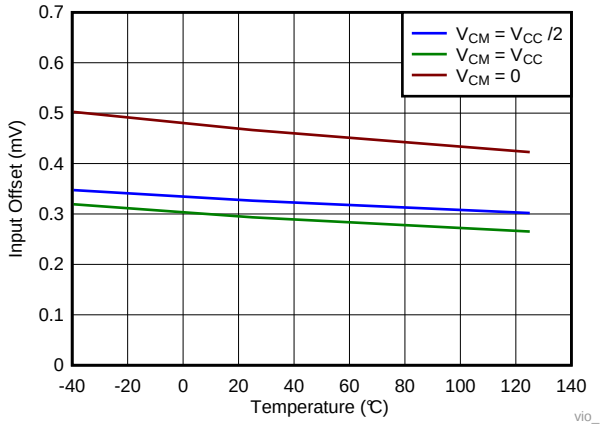
6.11 Typical Characteristics

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF



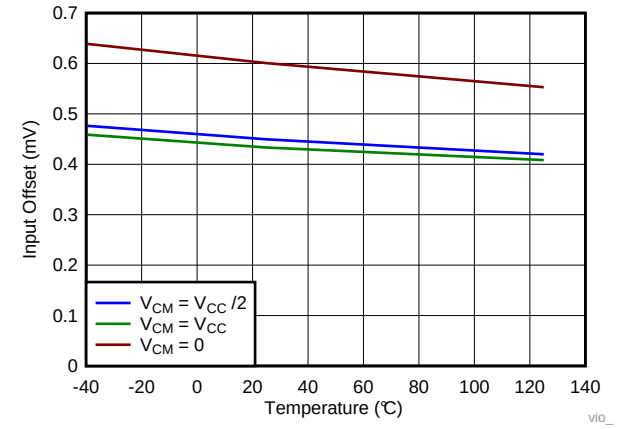
V_{CC} = 1.8 V

Figure 3. Input Offset vs Temperature



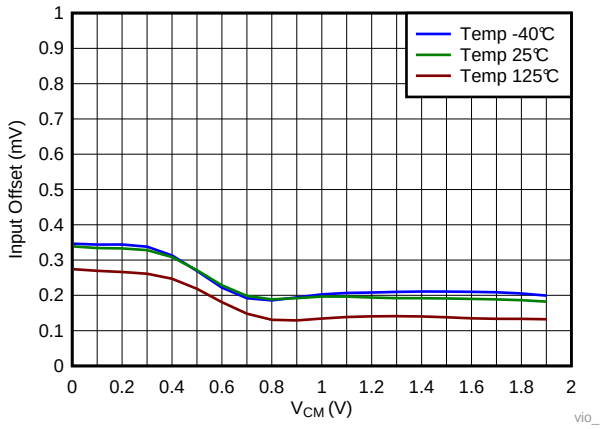
V_{CC} = 3.3 V

Figure 4. Input Offset vs Temperature



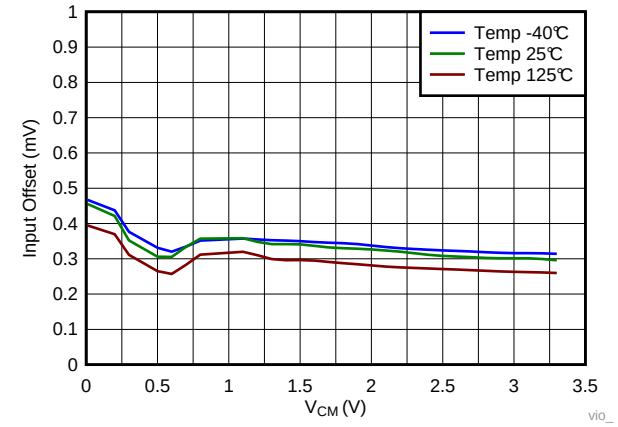
V_{CC} = 5 V

Figure 5. Input Offset vs Temperature



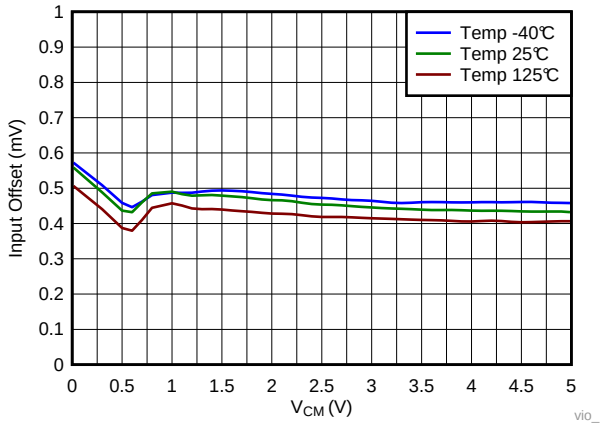
V_{CC} = 1.8 V

Figure 6. Input Offset Voltage vs V_{CM}



V_{CC} = 3.3 V

Figure 7. Input Offset Voltage vs V_{CM}

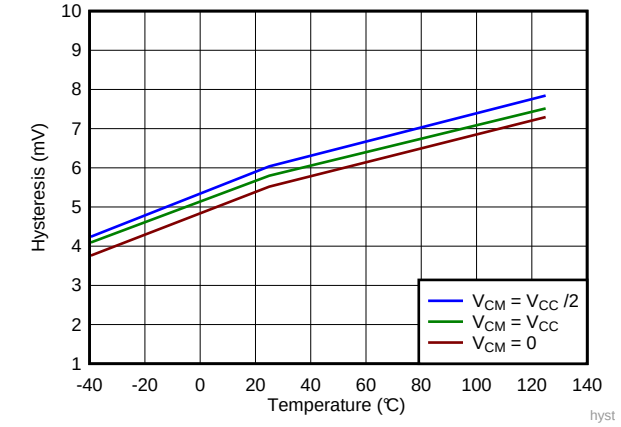


V_{CC} = 5 V

Figure 8. Input Offset Voltage vs V_{CM}

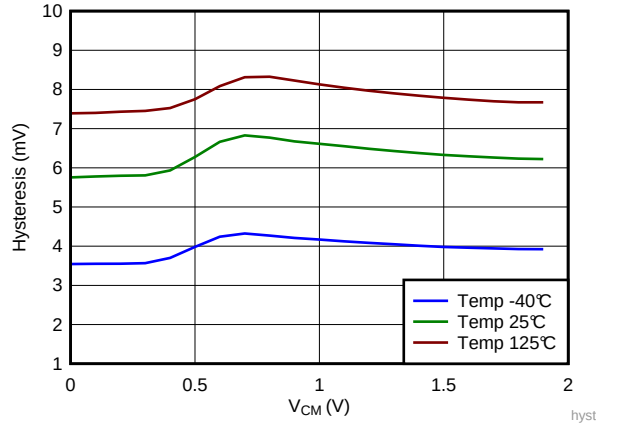
Typical Characteristics (continued)

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF



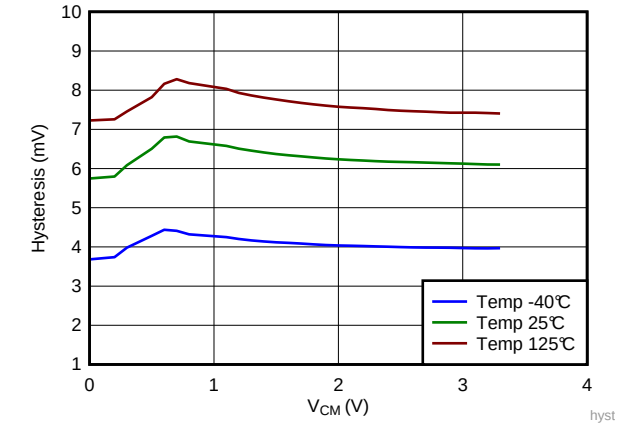
V_{CC} = 1.8 V to 5 V TLV70x1

Figure 9. Hysteresis vs Temperature



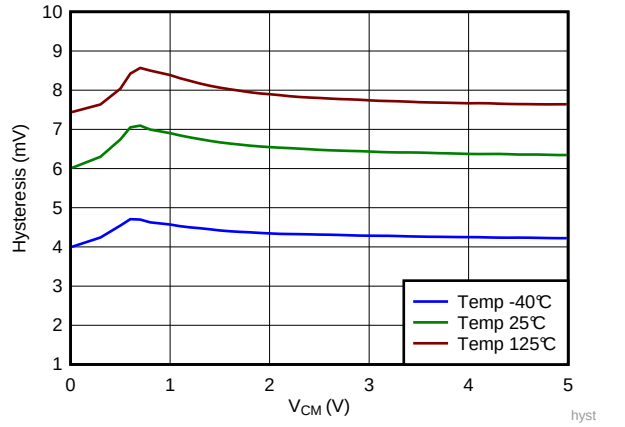
V_{CC} = 1.8 V TLV70x1

Figure 10. Hysteresis vs V_{CM}



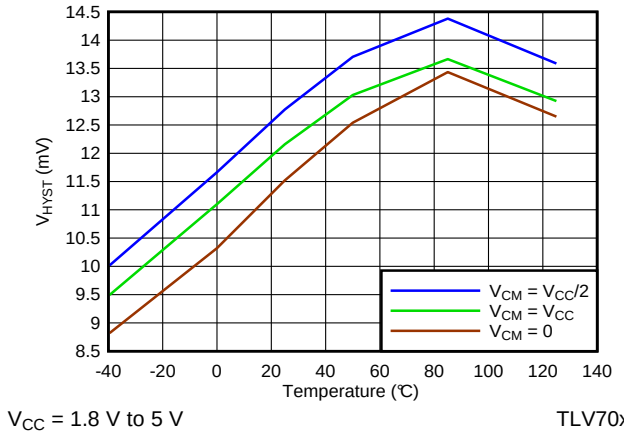
V_{CC} = 3.3 V TLV70x1

Figure 11. Hysteresis vs V_{CM}



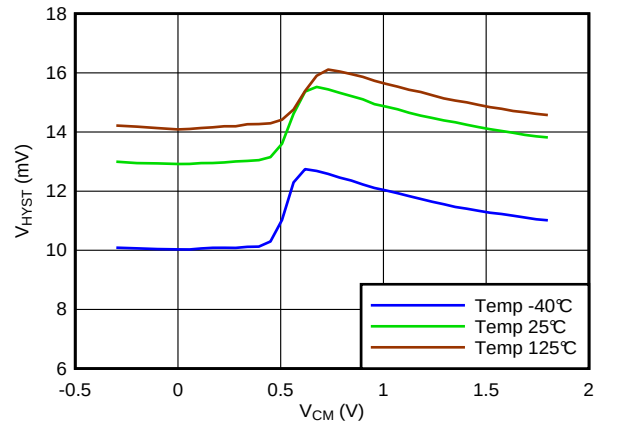
V_{CC} = 5 V TLV70x1

Figure 12. Hysteresis vs V_{CM}



V_{CC} = 1.8 V to 5 V TLV70x2

Figure 13. Hysteresis vs Temperature

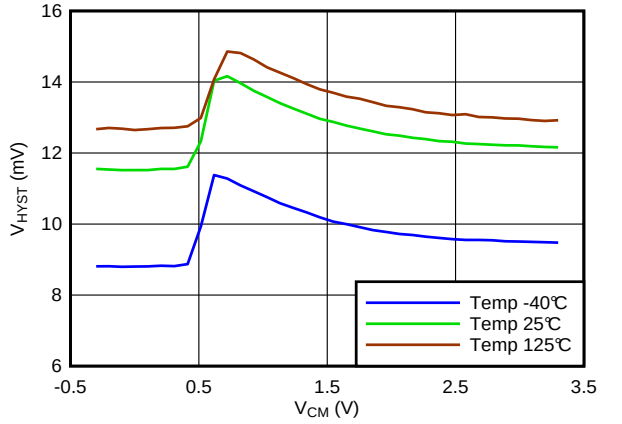


V_{CC} = 1.8 V TLV70x2

Figure 14. Hysteresis vs V_{CM}

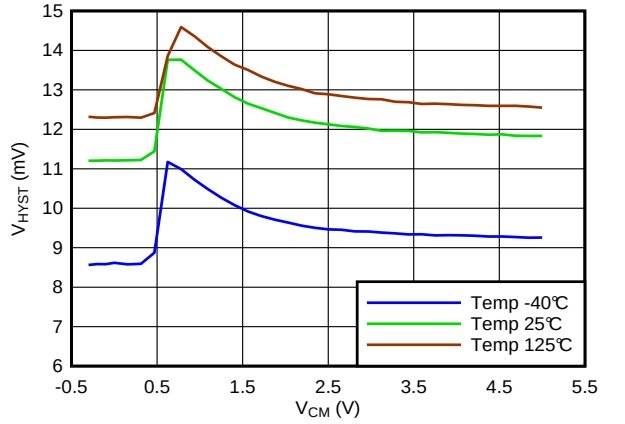
Typical Characteristics (continued)

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF



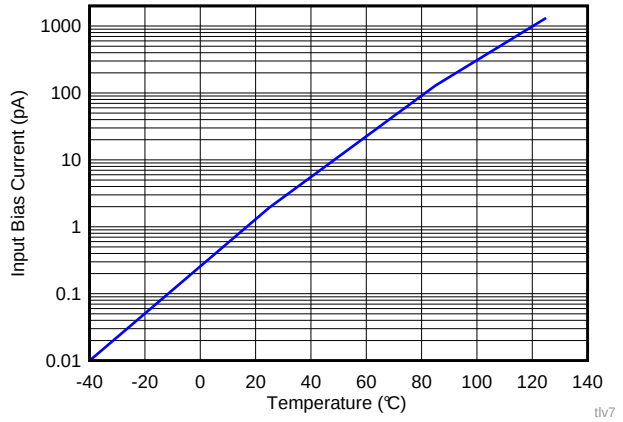
V_{CC} = 3.3 V TLV70x2

Figure 15. Hysteresis vs V_{CM}



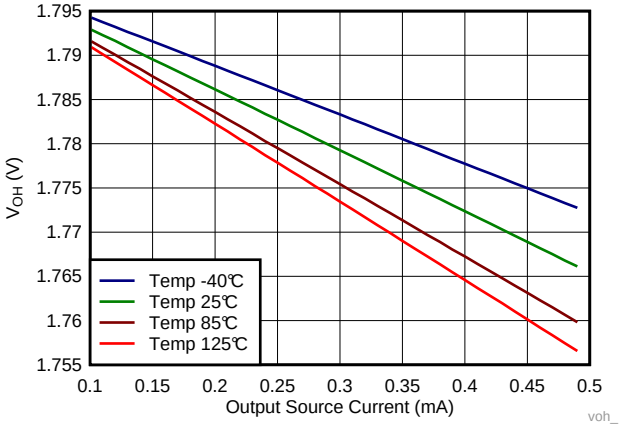
V_{CC} = 5 V TLV70x2

Figure 16. Hysteresis vs V_{CM}



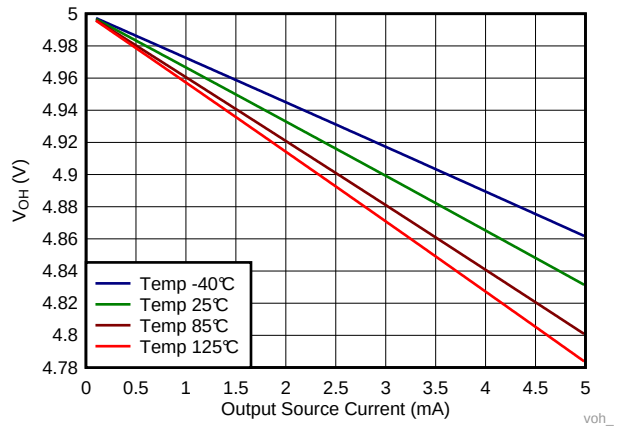
V_{CC} = 5 V

Figure 17. Input Bias Current vs Temperature



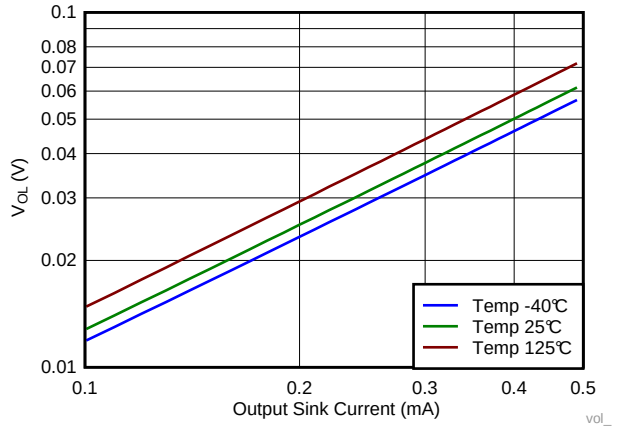
V_{CC} = 1.8 V TLV703x

Figure 18. Output Voltage High vs Output Source Current



V_{CC} = 5 V TLV703x

Figure 19. Output Voltage High vs Output Source Current

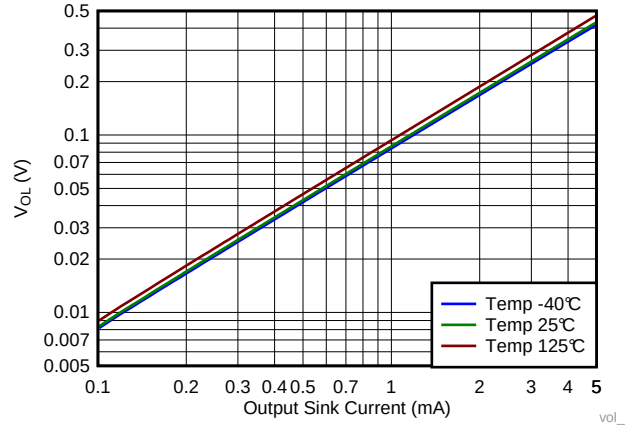


V_{CC} = 1.8 V

Figure 20. Output Voltage Low vs Output Sink Current

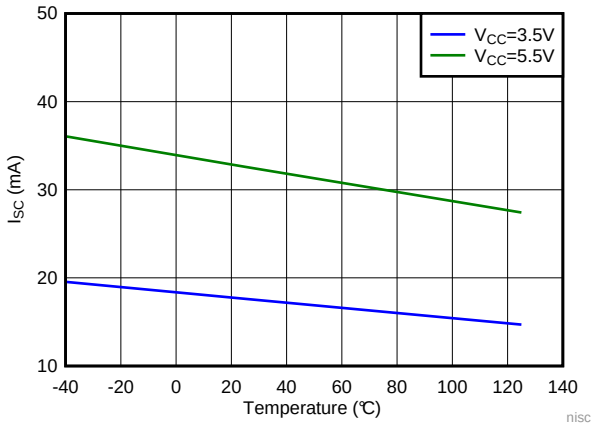
Typical Characteristics (continued)

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF



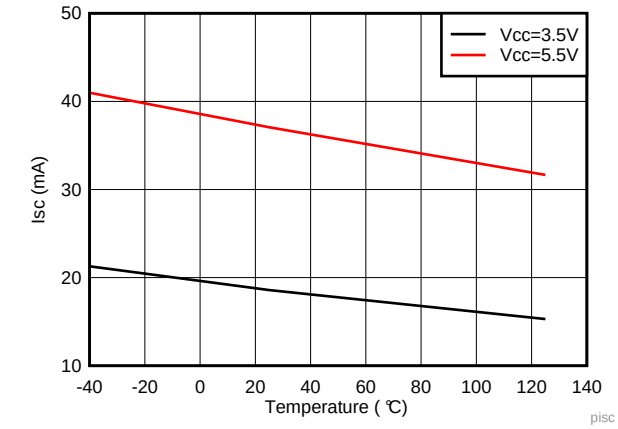
V_{CC} = 5 V

Figure 21. Output Voltage Low vs Output Sink Current



V_{CM} = V_{CC} / 2

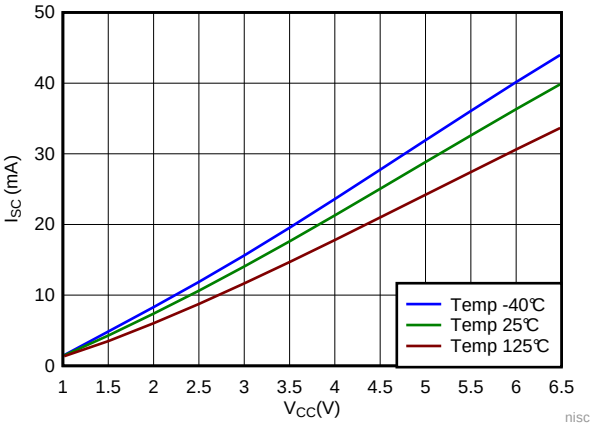
Figure 22. Output Short-Circuit (Sink) Current vs Temperature



V_{CM} = V_{CC} / 2

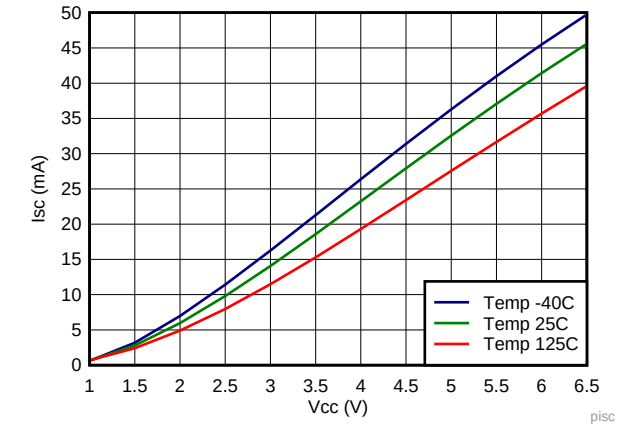
TLV703x

Figure 23. Output Short-Circuit (Source) Current vs Temperature



V_{CM} = V_{CC} / 2

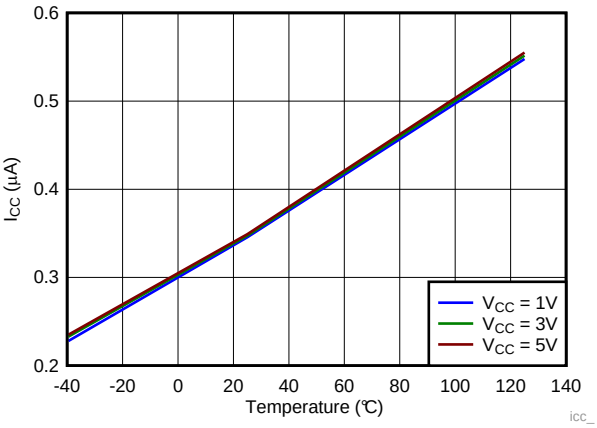
Figure 24. Output Short Circuit (Sink) vs V_{CC}



V_{CM} = V_{CC} / 2

TLV703x

Figure 25. Output Short Circuit (Source) vs V_{CC}



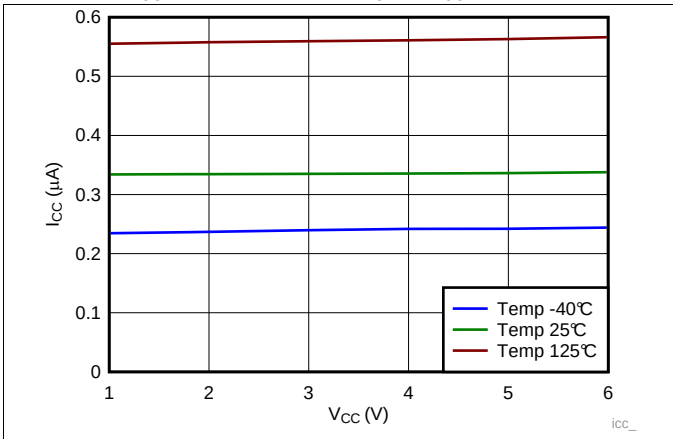
V_{CM} = V_{CC} / 2

TLV70x1

Figure 26. I_{CC} vs Temperature

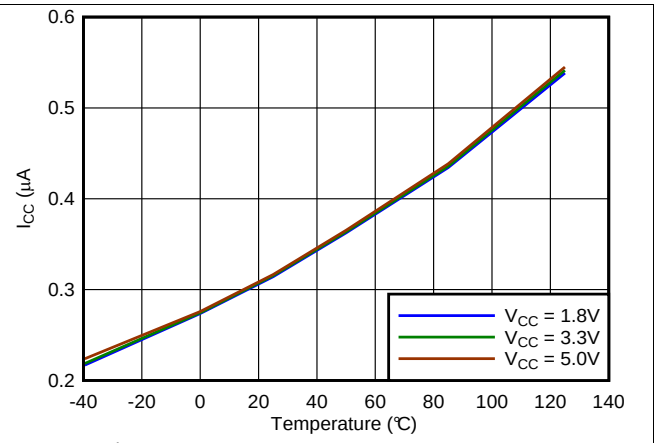
Typical Characteristics (continued)

T_A = 25°C, V_{CC} = 5 V, V_{EE} = 0 V, V_{CM} = V_{CC}/2, C_L = 15 pF



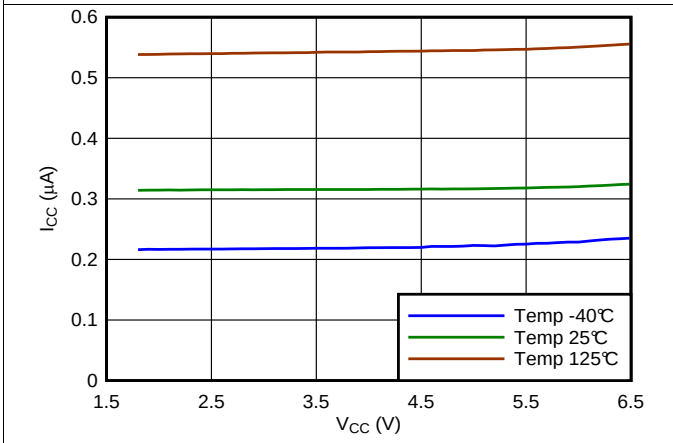
V_{CM} = V_{CC} / 2 TLV70x1

Figure 27. I_{CC} vs V_{CC}



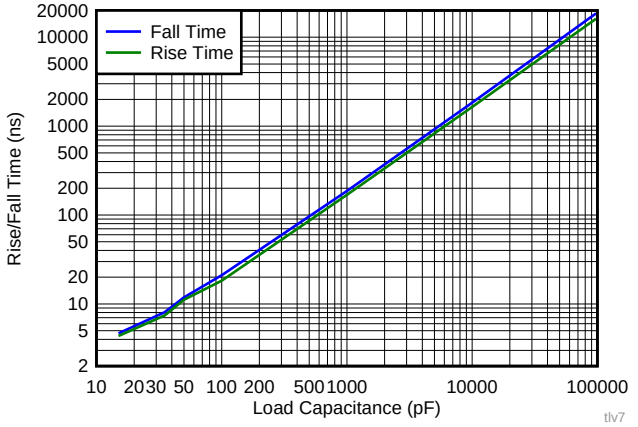
V_{CM} = V_{CC} / 2 TLV70x2

Figure 28. I_{CC} vs Temperature



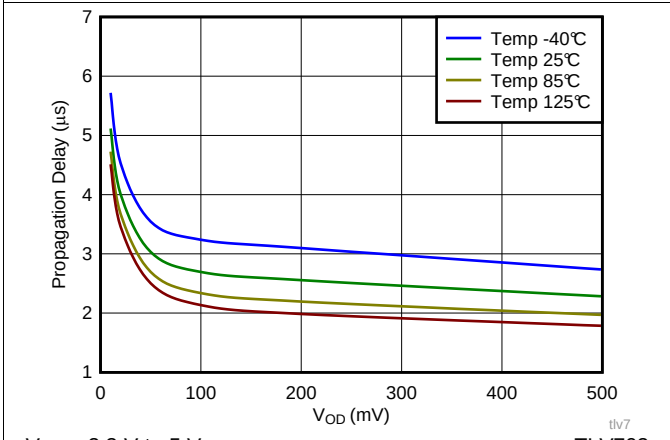
V_{CM} = V_{CC} / 2 TLV70x2

Figure 29. I_{CC} vs V_{CC}



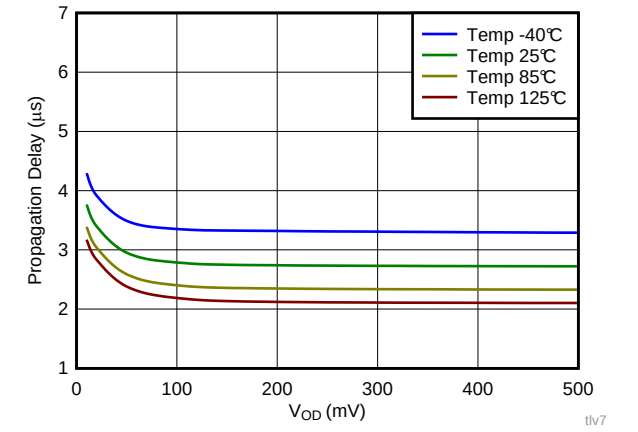
V_{OD} = 100 mV TLV703x Rise only

Figure 30. Rise/Fall Time vs Load Capacitance



V_{CC} = 3.3 V to 5 V TLV703x

Figure 31. Propagation Delay (L-H) vs Input Overdrive



V_{CC} = 3.3 V to 5 V

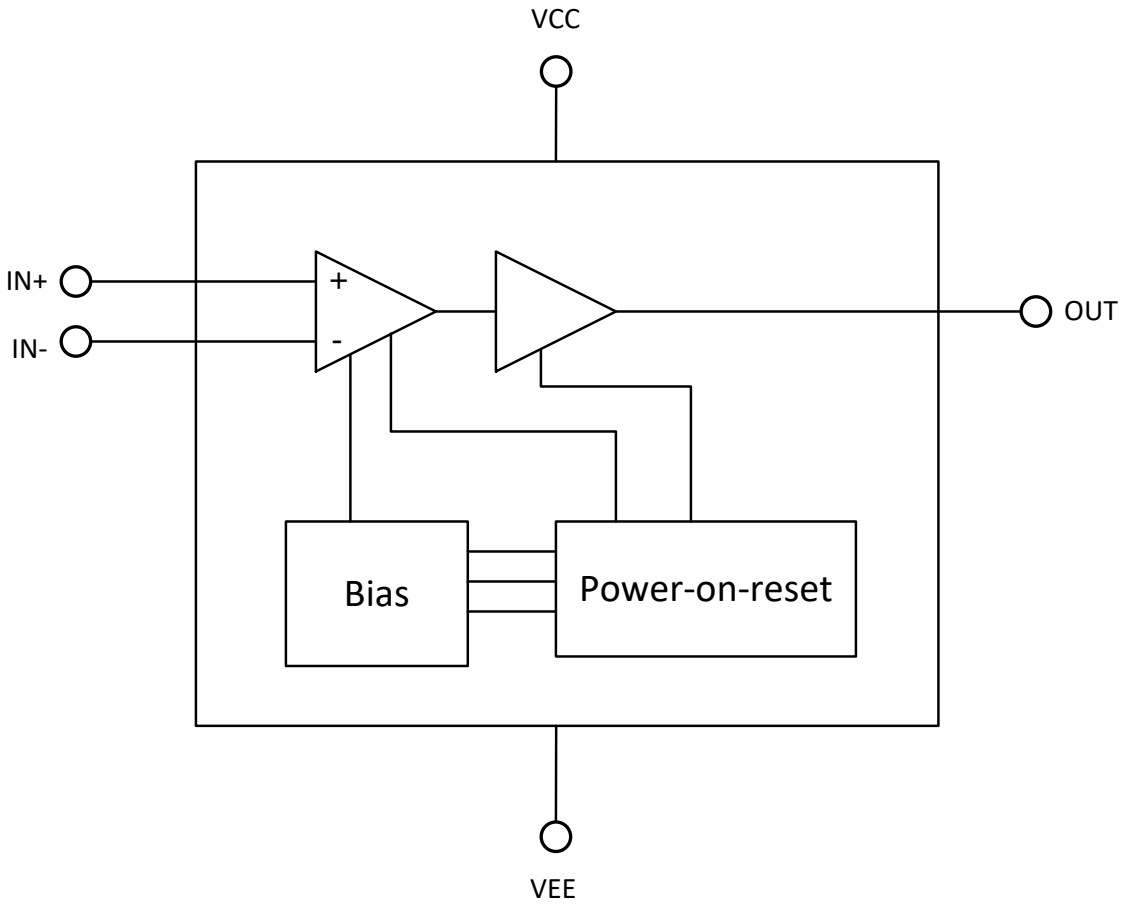
Figure 32. Propagation Delay (H-L) vs Input Overdrive

7 Detailed Description

7.1 Overview

The TLV703x and TLV704x devices are single-channel, nano-power comparators with push-pull and open-drain outputs. Operating from 1.6 V to 6.5 V and consuming only 315 nA, the TLV703x and TLV704x are designed for portable and industrial applications. The TLV703x and TLV704x are available in an ultra-small X2SON package (0.8 × 0.8 mm) to offer significant board space saving in space-challenged designs.

7.2 Functional Block Diagram



7.3 Feature Description

The TLV703x and TLV704x devices are nanoPower comparators that are capable of operating at low voltages. The TLV703x and TLV704x feature a rail-to-rail input stage capable of operating up to 100 mV beyond the VCC power supply rail. The TLV703x (push-pull) and TLV704x (open-drain) also feature internal hysteresis.

7.4 Device Functional Modes

The TLV703x and TLV704x have a power-on-reset (POR) circuit. While the power supply (V_S) is less than the minimum supply voltage, either upon ramp-up or ramp-down, the POR circuitry is activated.

For the TLV703x, the POR circuit holds the output low (at V_{EE}) while activated.

For the TLV704x, the POR circuit keeps the output high impedance (logical high) while activated.

When the supply voltage is greater than, or equal to, the minimum supply voltage, the comparator output reflects the state of the differential input (V_{ID}).

Device Functional Modes (continued)

7.4.1 Inputs

The TLV703x and TLV704x input common-mode extends from V_{EE} to 100 mV above V_{CC}. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase inversion of the comparator output occurs when the input pins exceed V_{CC} and V_{EE}.

The input of TLV703x and TLV704x is fault tolerant. It maintains the same high input impedance when V_{CC} is unpowered or ramping up. The input can be safely driven up to the specified maximum voltage (7 V) with V_{CC} = 0 V or any value up to the maximum specified. The V_{CC} is isolated from the input such that it maintains its value even when a higher voltage is applied to the input.

The input bias current is typically 1 pA for input voltages between V_{CC} and V_{EE}. The comparator inputs are protected from voltages below V_{EE} by internal diodes connected to V_{EE}. As the input voltage goes under V_{EE}, the protection diodes become forward biased and begin to conduct causing the input bias current to increase exponentially. Input bias current typically doubles every 10°C temperature increases.

7.4.2 Internal Hysteresis

The device hysteresis transfer curve is shown in Figure 33. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise (7 mV for both TLV703x and TLV704x).

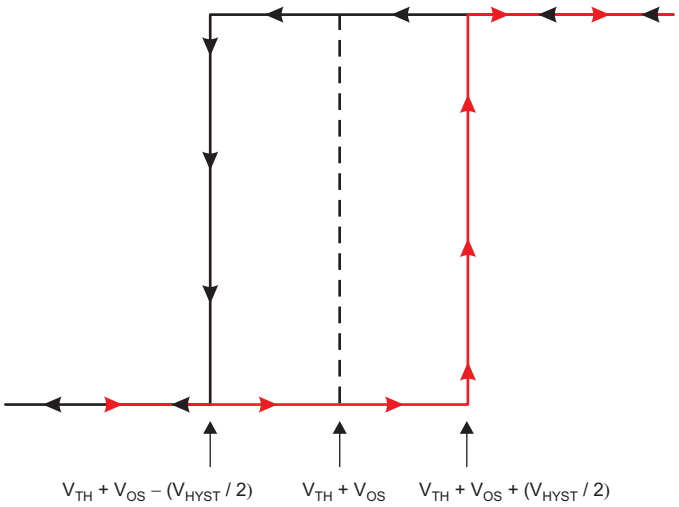


Figure 33. Hysteresis Transfer Curve

7.4.3 Output

The TLV703x features a push-pull output stage eliminating the need for an external pullup resistor. On the other hand, the TLV704x features an open-drain output stage enabling the output logic levels to be pulled up to an external source up to 6.5 V independent of the supply voltage.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV703x and TLV704x are nano-power comparators with reasonable response time. The comparators have a rail-to-rail input stage that can monitor signals beyond the positive supply rail with integrated hysteresis. When higher levels of hysteresis are required, positive feedback can be externally added. The push-pull output stage of the TLV703x is optimal for reduced power budget applications and features no shoot-through current. When level shifting or wire-ORing of the comparator outputs is needed, the TLV704x with its open-drain output stage is well suited to meet the system needs. In either case, the wide operating voltage range, low quiescent current, and small size of the TLV703x and TLV704x make these comparators excellent candidates for battery-operated and portable, handheld designs.

8.1.1 Inverting Comparator With Hysteresis for TLV703x

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in Figure 34. When V_{IN} at the inverting input is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2. Equation 1 defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than V_A, the output voltage is low, very close to ground. In this case, the three network resistors can be presented as R2 || R3 in series with R1. Use Equation 2 to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

Equation 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

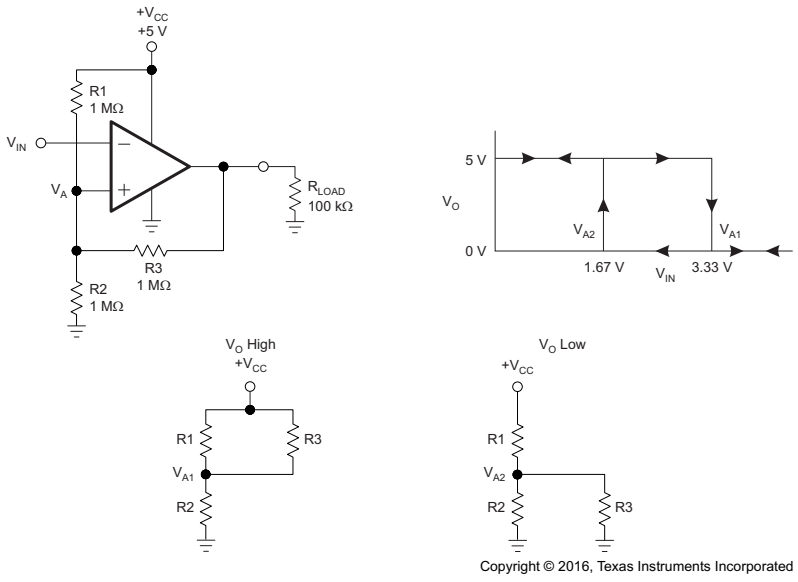


Figure 34. TLV703x in an Inverting Configuration With Hysteresis

Application Information (continued)

8.1.2 Noninverting Comparator With Hysteresis for TLV703x

A noninverting comparator with hysteresis requires a two-resistor network, as shown in Figure 35, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise to V_{IN1}. Use Equation 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is high, the output is also high. For the comparator to switch back to a low state, V_{IN} must drop to V_{IN2} such that V_A is equal to V_{REF}. Use Equation 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

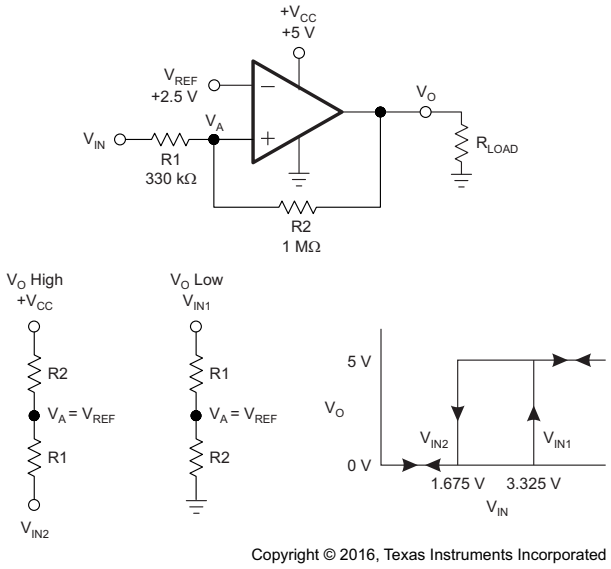


Figure 35. TLV703x in a Noninverting Configuration With Hysteresis

8.2 Typical Applications

8.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. Figure 36 shows a simple window comparator circuit.

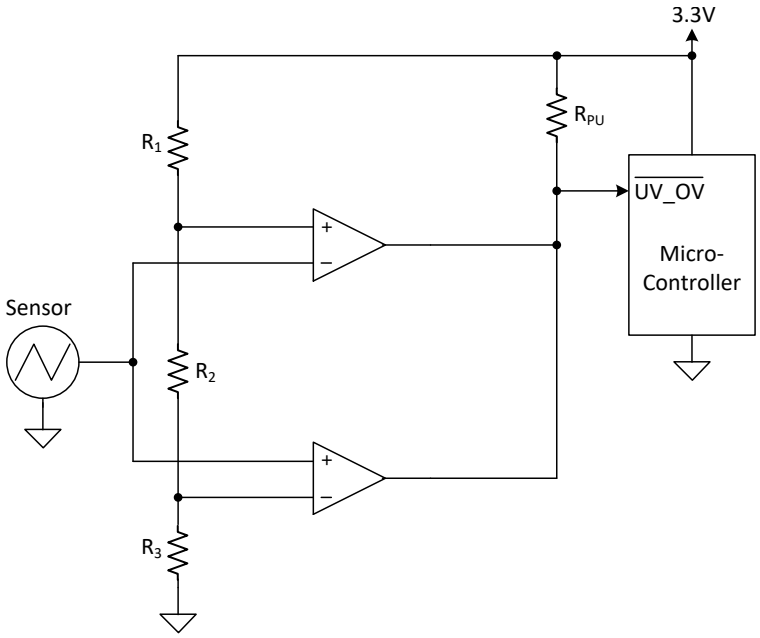


Figure 36. TLV704x-Based Window Comparator

8.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (logic low output) when an input signal is less than 1.1 V
- Alert (logic low output) when an input signal is greater than 2.2 V
- Alert signal is active low
- Operate from a 3.3-V power supply

8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in Figure 36. Connect V_{CC} to a 3.3-V power supply and V_{EE} to ground. Make R1, R2, and R3 each 10-MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and $V_{TH–}$). With each resistor being equal, V_{TH+} is 2.2 V and V_{TH-} is 1.1 V. Large resistor values such as 10 MΩ are used to minimize power consumption. The sensor output voltage is applied to the inverting and noninverting inputs of the two TLV704x devices. The TLV704x is used for its open-drain output configuration. Using the TLV704x allows the two comparator outputs to be wire-ored together. The respective comparator outputs are low when the sensor is less than 1.1 V or greater than 2.2 V. V_{OUT} is high when the sensor is in the range of 1.1 V to 2.2 V.

Typical Applications (continued)

8.2.1.3 Application Curve

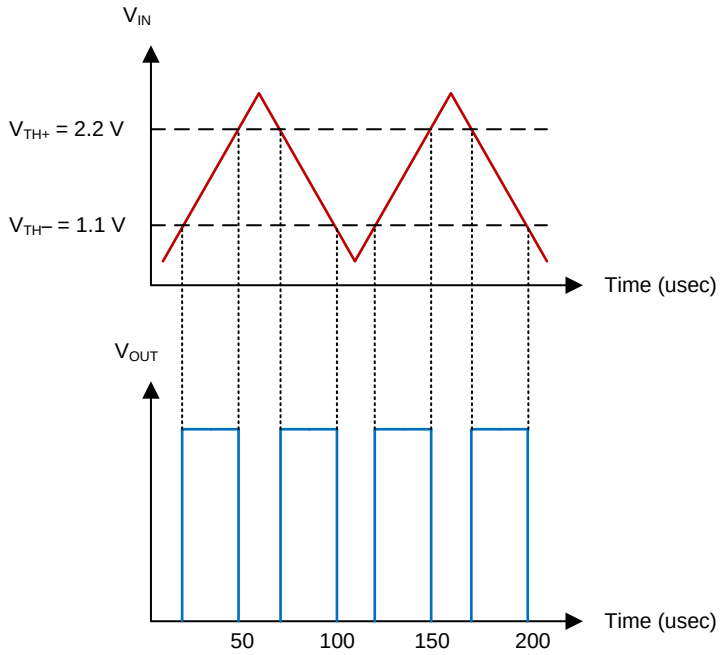


Figure 37. Window Comparator Results

8.2.2 IR Receiver Analog Front End

A single TLV703x device can be used to build a complete IR receiver analog front end (AFE). The nanoamp quiescent current and low input bias current make it possible to be powered with a coin cell battery, which could last for years.

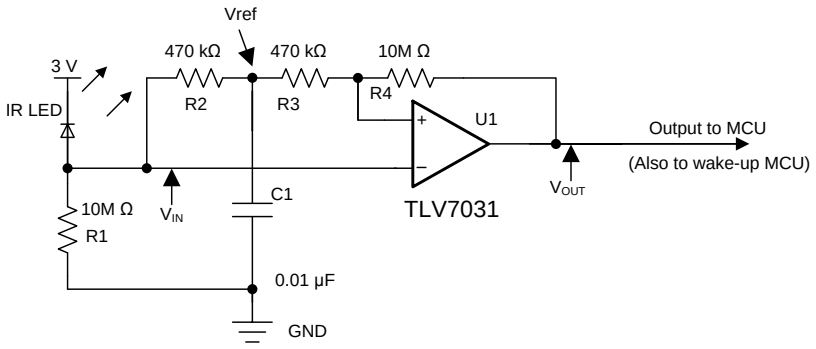


Figure 38. IR Receiver Analog Front End Using TLV703x

8.2.2.1 Design Requirements

For this design, follow these design requirements:

- Use a proper resistor (R_1) value to generate an adequate signal amplitude applied to the inverting input of the comparator.
- The low input bias current I_B (2 pA typical) ensures that a greater value of R1 to be used.
- The RC constant value (R_2 and C_1) must support the targeted data rate (that is, 9,600 bauds) in order to maintain a valid tripping threshold.
- The hysteresis introduced with R_3 and R_4 helps to avoid spurious output toggles.

Typical Applications (continued)

8.2.2.2 Detailed Design Procedure

The IR receiver AFE design is highly streamlined and optimized. R_1 converts the IR light energy induced current into voltage and applies to the inverting input of the comparator. The RC network of R_2 and C_1 establishes a reference voltage V_{ref}, which tracks the mean amplitude of the IR signal. The noninverting input is directly connected to V_{ref} through R3. R3 and R4 are used to produce a hysteresis to keep transitions free of spurious toggles. To reduce the current drain from the coin cell battery, data transmission must be short and infrequent.

More technical details are provided in the TI TechNote *Low Power Comparator for Signal Processing and Wake-Up Circuit in Smart Meters* (SNVA808).

8.2.2.3 Application Curve

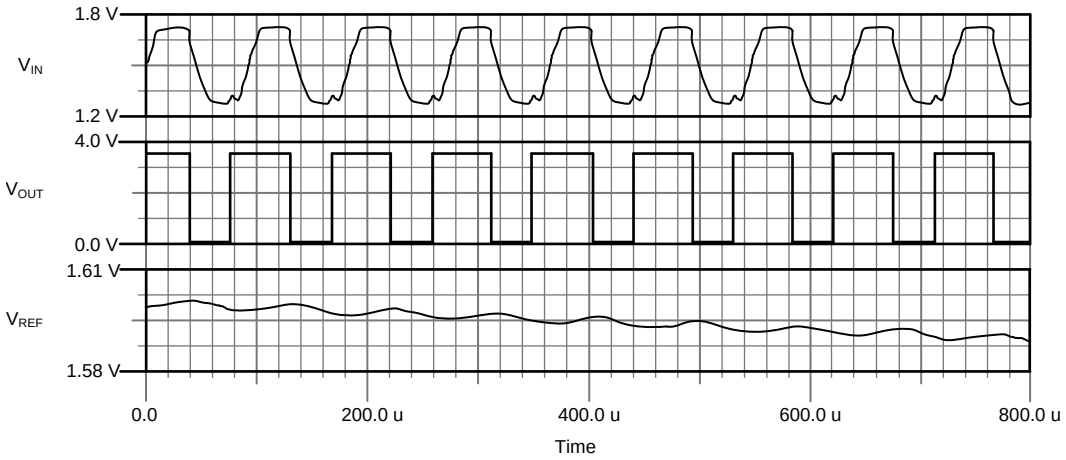


Figure 39. IR Receiver AFE Waveforms

Typical Applications (continued)

8.2.3 Square-Wave Oscillator

A square-wave oscillator can be used as low-cost timing reference or system supervisory clock source.

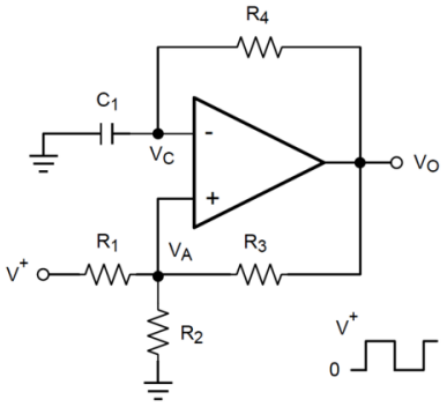


Figure 40. Square-Wave Oscillator

8.2.3.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor and resistor. The maximum frequency is limited by the propagation delay of the device and the capacitance load at the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which may help reduce BOM cost and board space.

8.2.3.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following section provides details to calculate these component values.

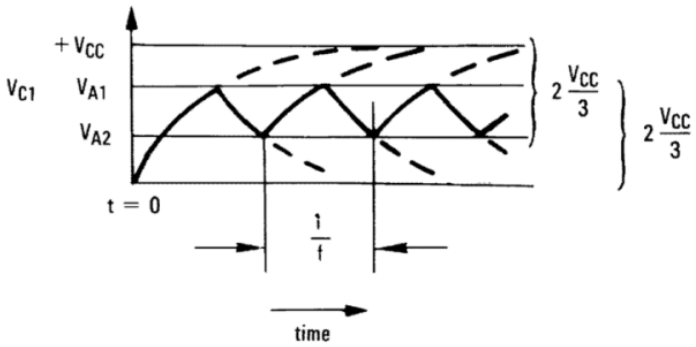


Figure 41. Square-Wave Oscillator Timing Thresholds

First consider the output of figure Figure 40 is high, which indicates the inverted input V_C is lower than the noninverting input (V_A). This causes the C_1 to be charged through R_4, and the voltage V_C increases until it is equal to the noninverting input. The value of V_A at the point is calculated by Equation 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 \text{IIR}_3} \tag{7}$$

If $R_1 = R_2 = R_3$, then $V_{A1} = 2\ V_{CC}/\ 3$

Typical Applications (continued)

At this time the comparator output trips pulling down the output to the negative rail. The value of V_A at this point is calculated by Equation 8.

$$V_{A2} = \frac{V_{CC}(R_2 \| R_3)}{R_1 + R_2 \| R_3} \quad (8)$$

If $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The C_1 now discharges though the R_4, and the voltage V_{CC} decreases until it reaches V_{A2}. At this point, the output switches back to the starting state. The oscillation period equals the time duration from 2 V_{CC} / 3 to V_{CC} / 3 then back to 2 V_{CC} / 3, which is given by $R_4C_1 \times \ln 2$ for each trip. Therefore, the total time duration is calculated as 2 $R_4C_1 \times \ln 2$. The oscillation frequency can be obtained by Equation 9:

$$f = 1/(2\ R4 \times C1 \times \ln 2) \quad (9)$$

8.2.3.3 Application Curve

Figure 42 shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100\ k\Omega$
- $C_1 = 100$ pF, $C_L = 20$ pF
- V+ = 5 V, V– = GND
- C_{stray} (not shown) from V_A to GND = 10 pF

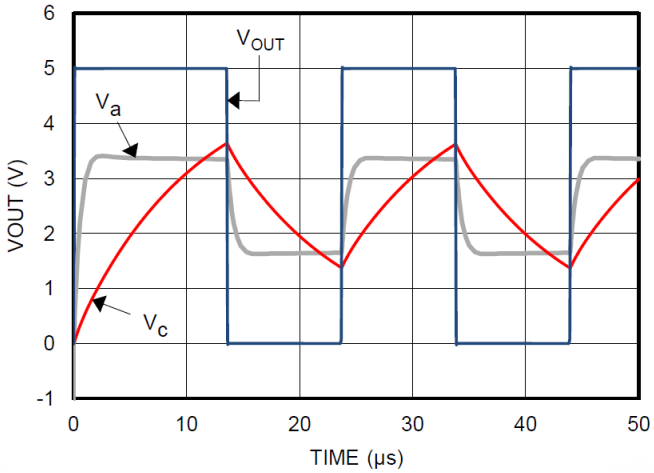


Figure 42. Square-Wave Oscillator Output Waveform

Typical Applications (continued)

8.2.4 Quadrature Rotary Encoder

A quadrature encoder for rotary motors/shafts utilizing a Tunneling Magnetoresitance (TMR) Rotation Sensor can track the position of the motor shaft even when power is turned off, while the TLV7032 provides additional hysteresis to prevent unwanted output toggling between quadrants. The TLV7032 can be used with other sensing techniques as well, such as optical, capacitive, or inductive.

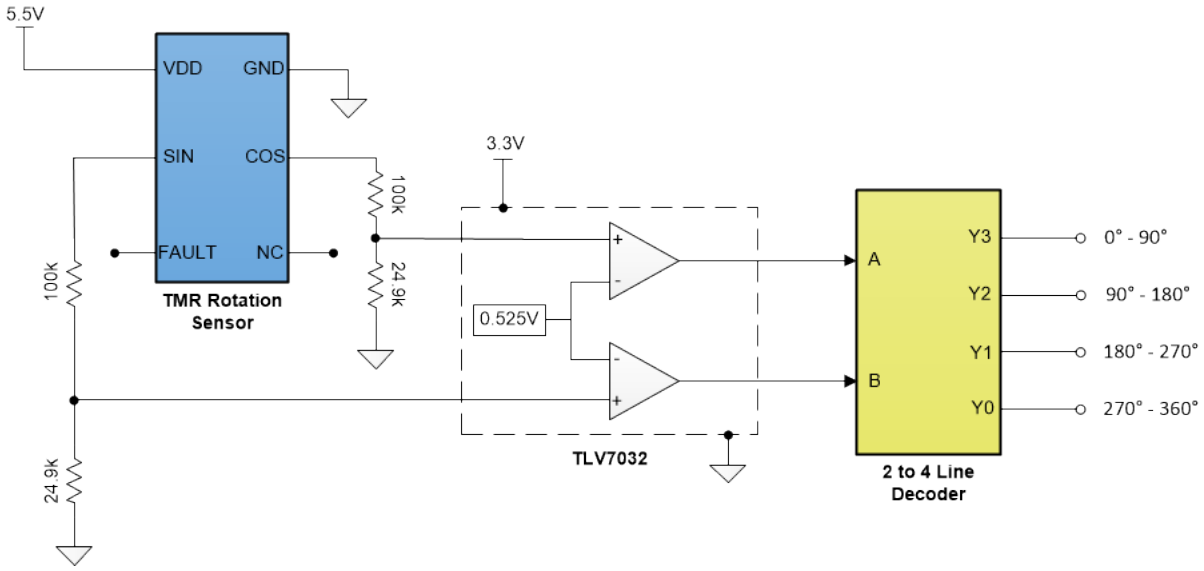
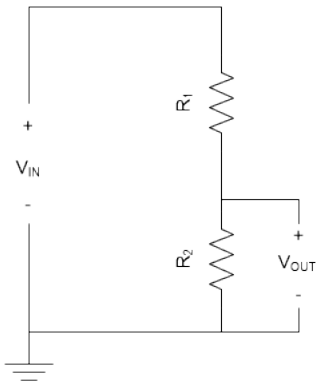


Figure 43. Quadrant Encoder Detector

8.2.4.1 Design Requirements

TMR Rotation Sensors general have two digital, binary outputs that are 90 degrees out of phase. The TLV7032 can be used to provide additional hysteresis to ensure there isn't any unwanted toggling of the output when the sensors are between the transition points of two quadrants. The TLV7032 already provides 10mV of typical internal hysteresis. By dividing down the output voltage from the rotation sensor using a voltage divider, the internal hysteresis will be scaled up by the same voltage divider ratio.



$$V_{OUT} = V_{IN} \times \frac{R2}{R1+R2}$$

Figure 44. Voltage Divider Equation

Typical Applications (continued)

8.2.4.2 Detailed Design Procedure

First, choose a target range of hysteresis to achieve. For this design example, 50mV of hysteresis will be the target. Since the TLV7032 already has 10mV (typ) of internal hysteresis, the voltage output from the TMR Rotation Sensor should be scaled down by a factor of 5. This way, the 10mV of internal hysteresis gets scaled up by a factor of 5, resulting in 50mV of hysteresis. The minimum output HIGH level for the TMR Rotation Sensor used in Figure 47 is 5.25 V. Since 5.25V will be the minimum output high value, it can be used to substitute V_{IN} from the Voltage Divider Equation in Figure 48. Since the voltage from the TMR rotation sensor needs to be scaled down by a factor of 5, the equation in Figure 48 can be rewritten as:

$$\frac{1}{5} = \frac{R_2}{R_1 + R_2}$$

The above equation can be solved for using standard resistor values, where R_1 = 100kΩ, and R_2 = 24.9kΩ. The minimum voltage seen at the noninverting pins of the comparator when the output is HIGH will be 1.05V. To make the device transition at 50% output high level, the inverting pins of the TLV7032 should be tied to a 0.525V reference.

8.2.4.3 Application Curve

Figure 49 shows the TLV7032 achieving approximately 50mV of hysteresis using the following component values:

- R_1 = 100kΩ
- R_2 = 24.9kΩ
- V_{REF} (IN-) = 0.525V

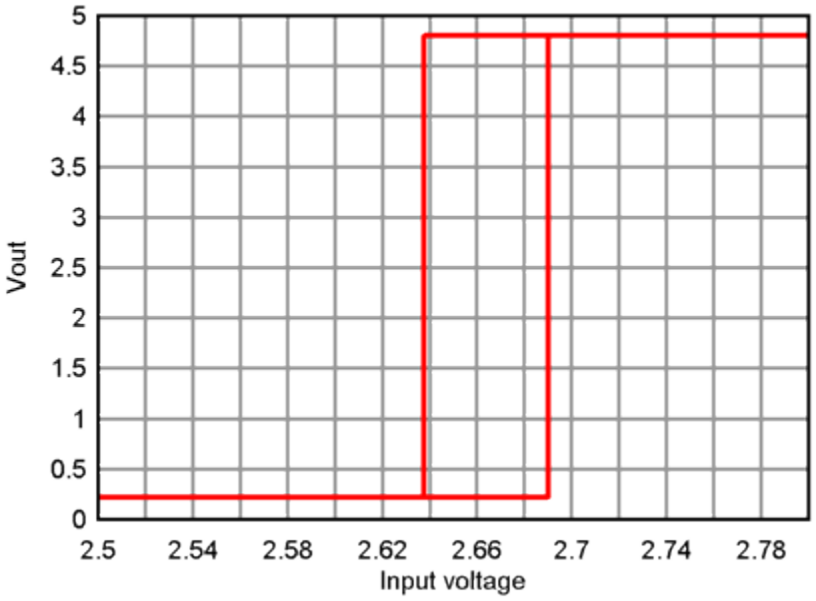


Figure 45. DC Input Voltage Sweep

9 Power Supply Recommendations

The TLV703x and TLV704x have a recommended operating voltage range (V_S) of 1.6 V to 6.5 V. V_S is defined as V_{CC} – V_{EE}. Therefore, the supply voltages used to create V_S can be single-ended or bipolar. For example, single-ended supply voltages of 5 V and 0 V and bipolar supply voltages of +2.5 V and –2.5 V create comparable operating voltages for V_S. However, when bipolar supply voltages are used, it is important to realize that the logic low level of the comparator output is referenced to V_{EE}.

Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current.

10 Layout

10.1 Layout Guidelines

To reduce PCB fabrication cost and improve reliability, TI recommends using a 4-mil via at the center pad connected to the ground trace or plane on the bottom layer.

TI recommends a power-supply bypass capacitor of 100 nF when supply output impedance is high, supply traces are long, or when excessive noise is expected on the supply lines. Bypass capacitors are also recommended when the comparator output drives a long trace or is required to drive a capacitive load. Due to the fast rising and falling edge rates and high-output sink and source capability of the TLV703x and TLV704x output stages, higher than normal quiescent current can be drawn from the power supply. Under this circumstance, the system would benefit from a bypass capacitor across the supply pins.

10.2 Layout Example

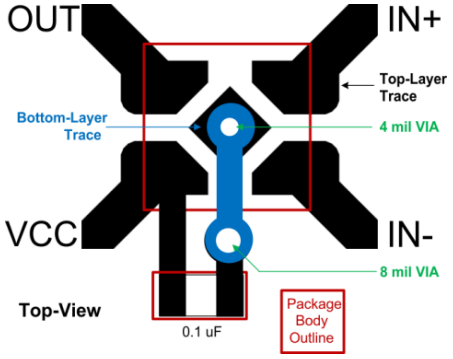


Figure 46. Layout Example

The application report *Designing and Manufacturing With TI's X2SON Packages* (SCEA055) helps PCB designers to achieve optimal designs.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV70x1 device family. The TLV7011 Micro-Power Comparator Dip Adaptor Evaluation Module can be requested at the Texas Instruments website through the product folder or purchased directly from the TI eStore.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *Designing and Manufacturing With TI's X2SON Packages* (SCEA055)
- *Low Power Comparator for Signal Processing and Wake-Up Circuit in Smart Meters* (SNVA808)

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV7031	Click here	Click here	Click here	Click here	Click here
TLV7032	Click here	Click here	Click here	Click here	Click here
TLV7041	Click here	Click here	Click here	Click here	Click here
TLV7042	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV7031DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1IE2	Samples
TLV7031DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19P	Samples
TLV7031DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19P	Samples
TLV7031DPWR	ACTIVE	X2SON	DPW	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7K	Samples
TLV7032DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7032	Samples
TLV7041DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1IF2	Samples
TLV7041DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19Q	Samples
TLV7041DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19Q	Samples
TLV7041DPWR	ACTIVE	X2SON	DPW	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7L	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

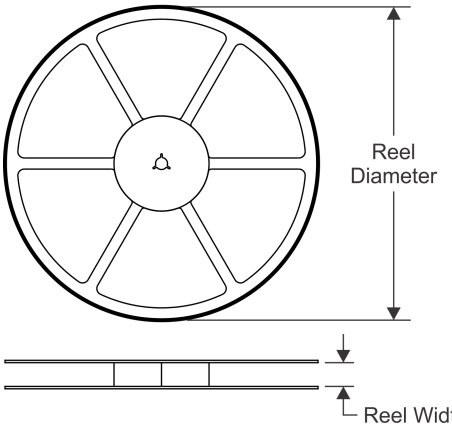
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

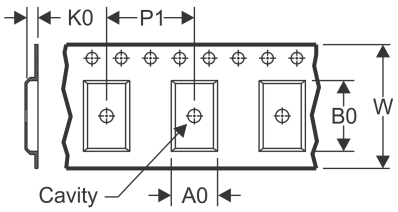
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

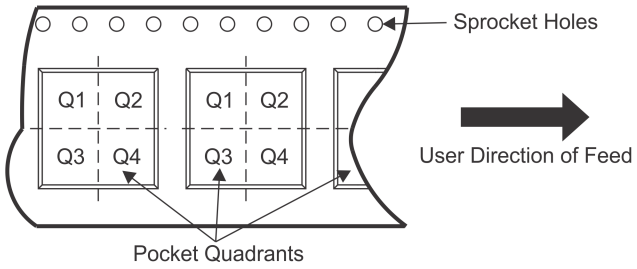


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

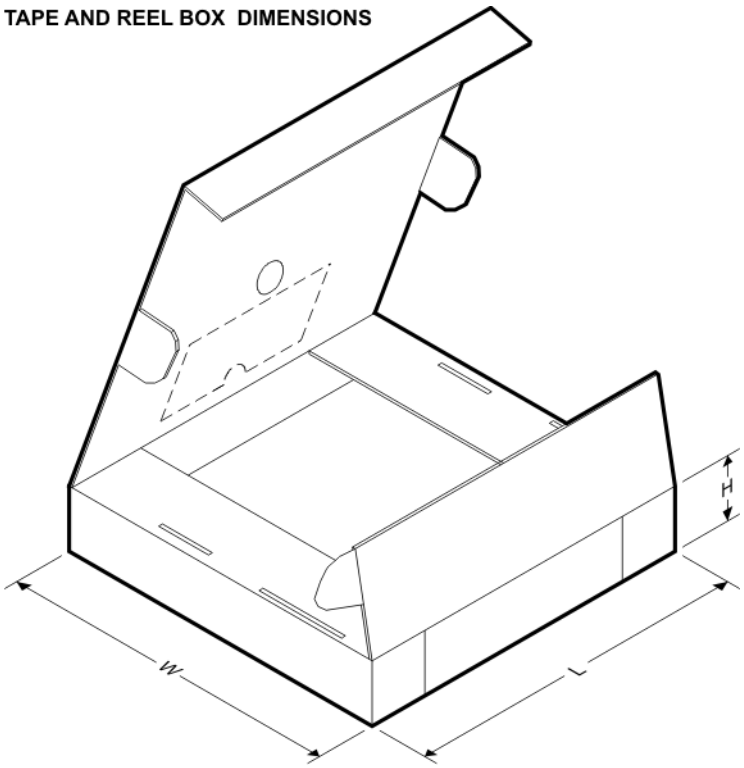
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7031DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV7031DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q2
TLV7031DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q2
TLV7031DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV7032DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV7041DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV7041DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q2
TLV7041DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q2
TLV7041DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2

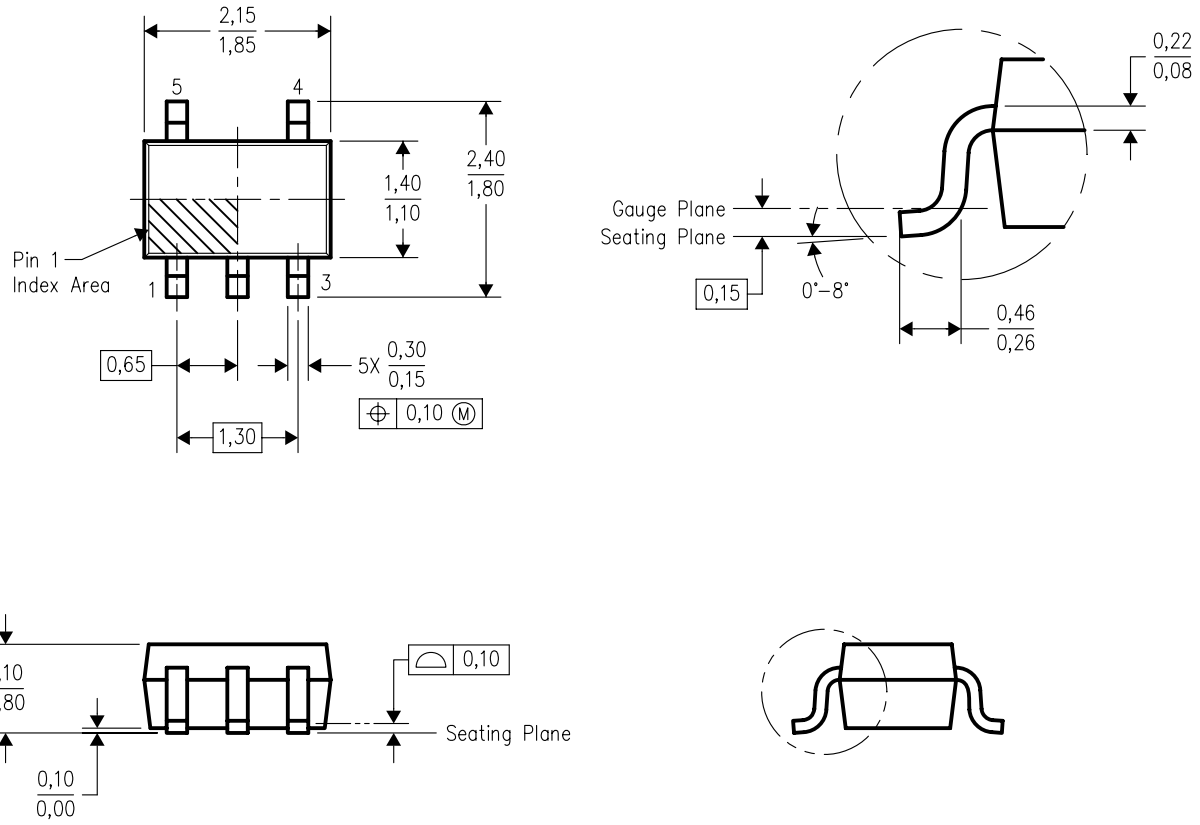
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7031DBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV7031DCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TLV7031DCKT	SC70	DCK	5	250	190.0	190.0	30.0
TLV7031DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV7032DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV7041DBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV7041DCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TLV7041DCKT	SC70	DCK	5	250	190.0	190.0	30.0
TLV7041DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0

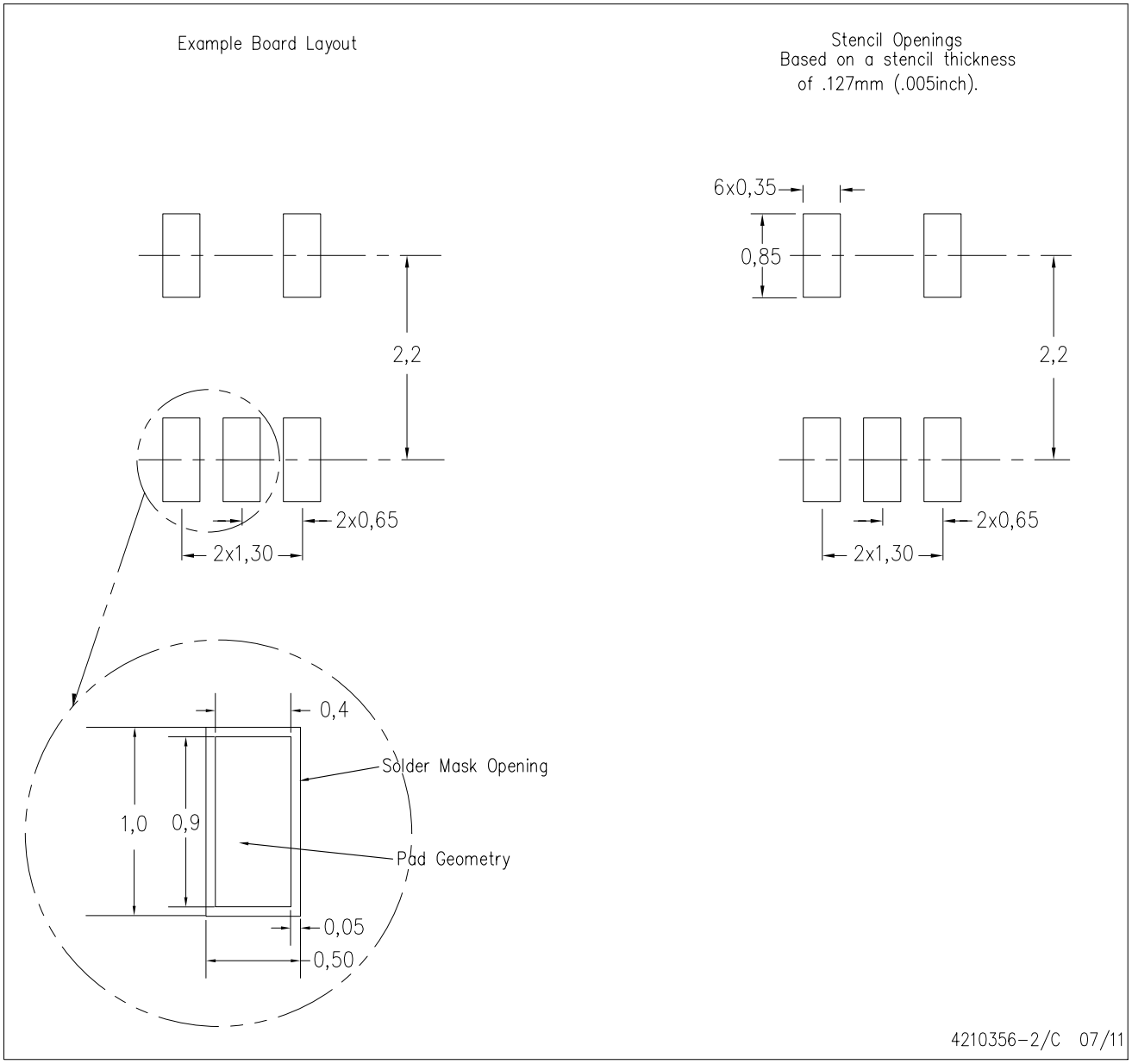
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

GENERIC PACKAGE VIEW

DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

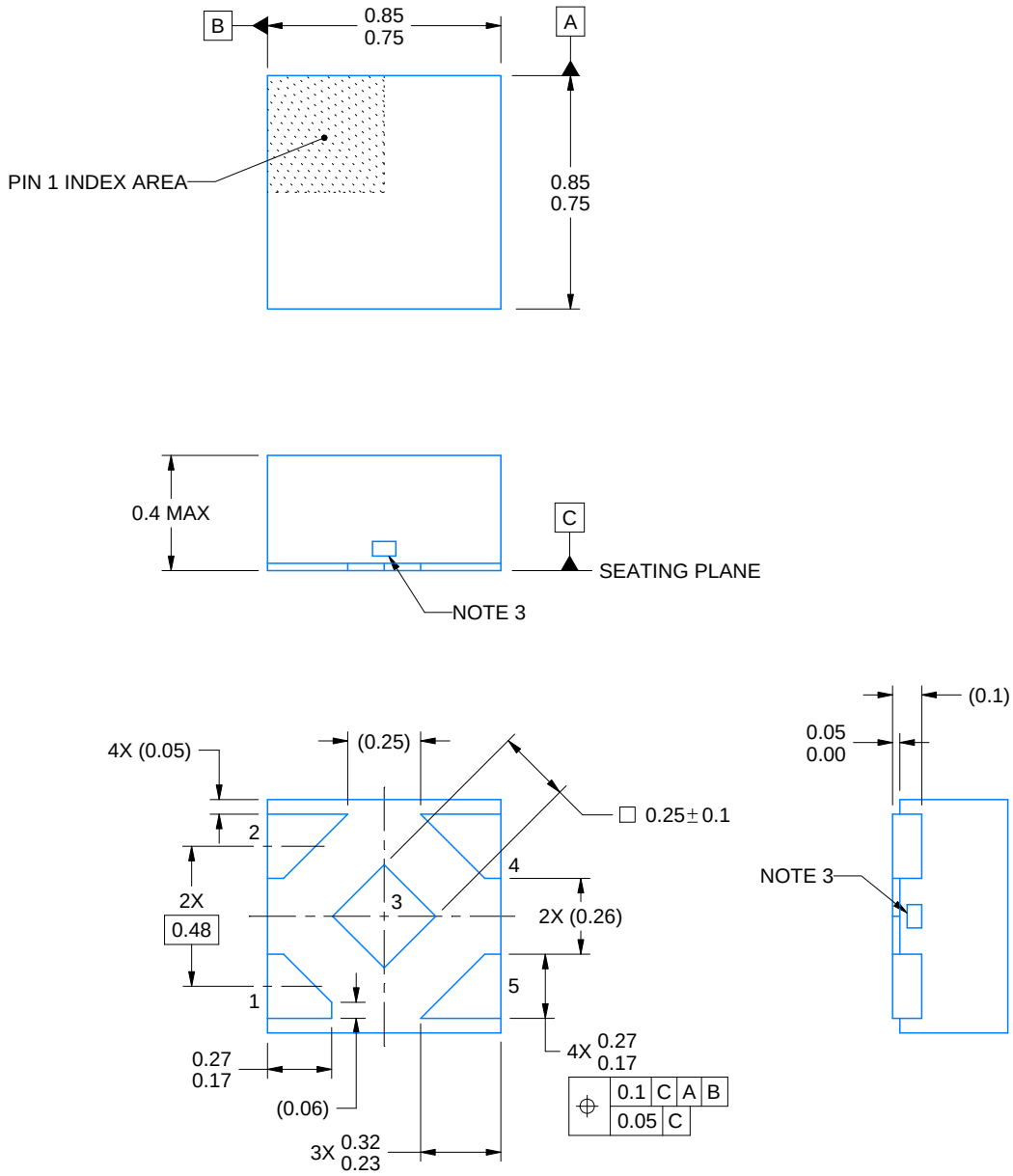
4211218-3/D

PACKAGE OUTLINE

DPW0005A

X2SON - 0.4 mm max height

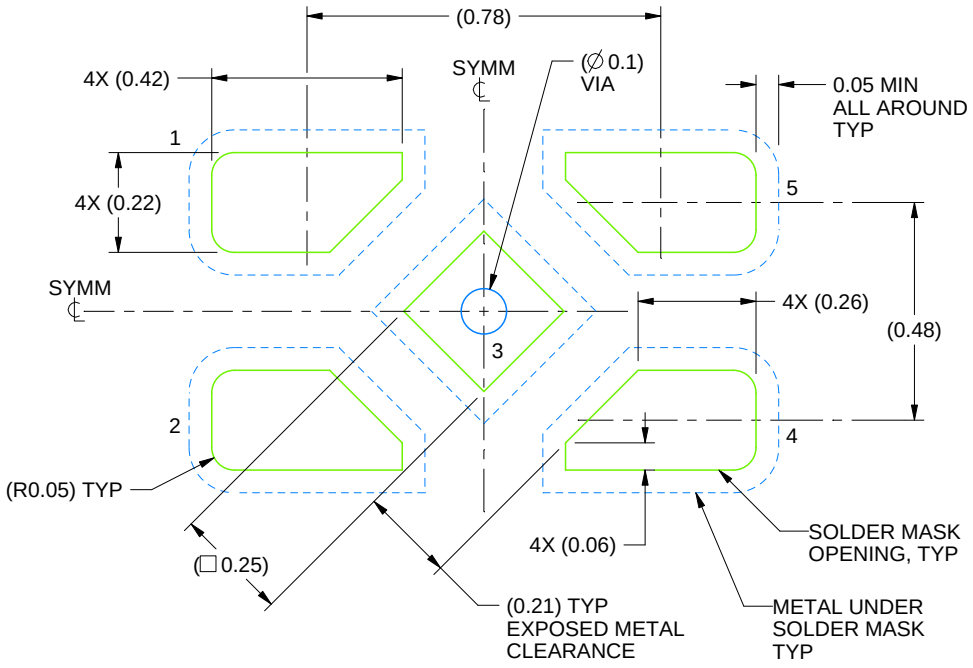
PLASTIC SMALL OUTLINE - NO LEAD



4223102/B 09/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

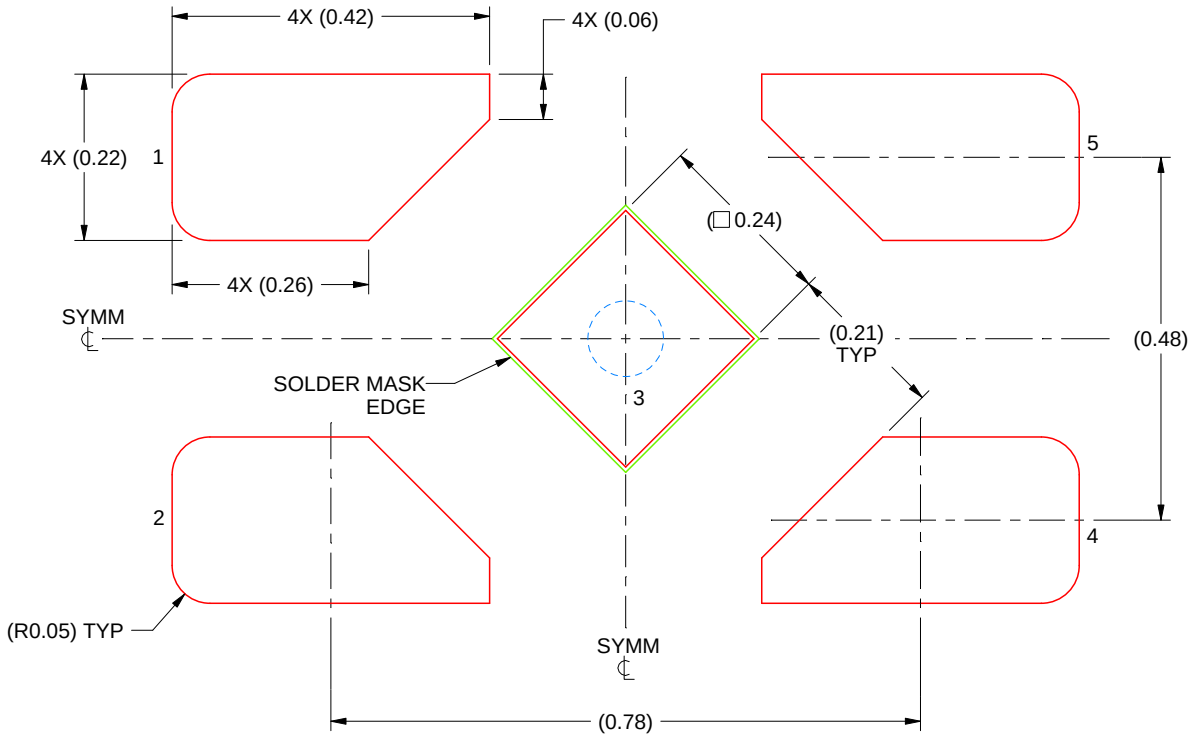


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/B 09/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
92% PRINTED SOLDER COVERAGE BY AREA
SCALE:100X

4223102/B 09/2017

NOTES: (continued)

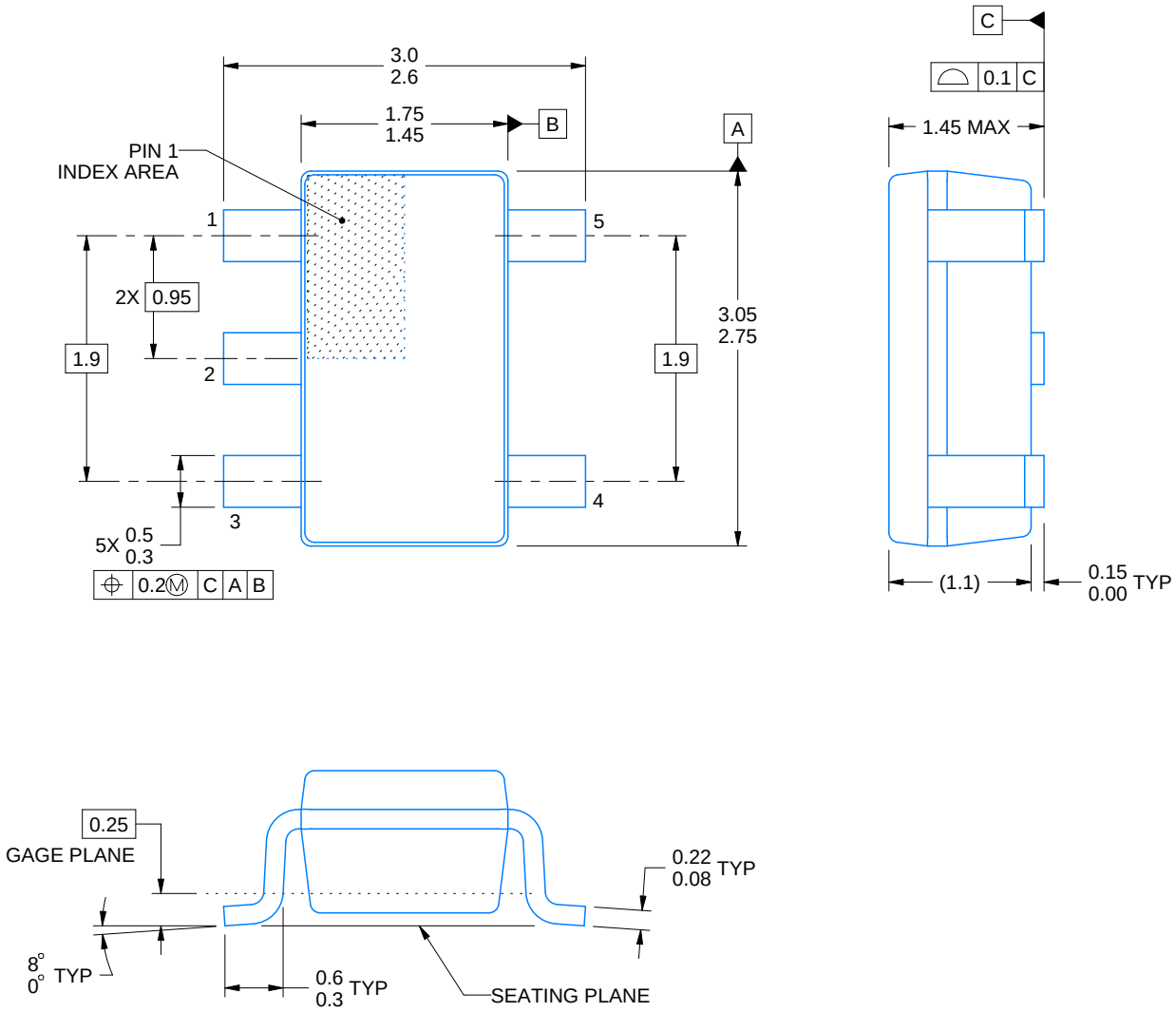
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

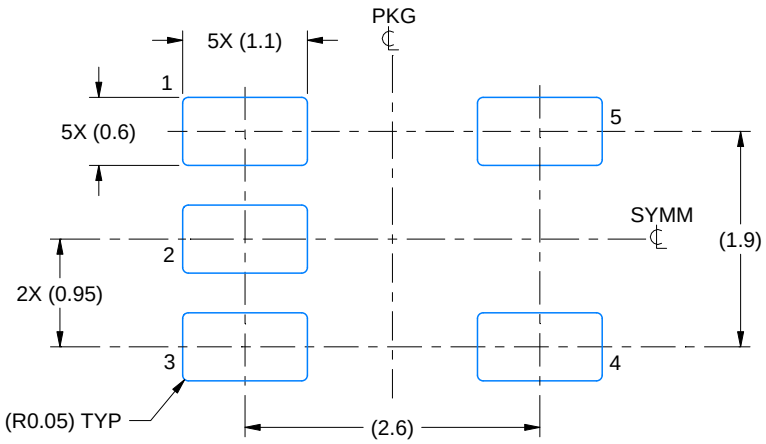
SMALL OUTLINE TRANSISTOR



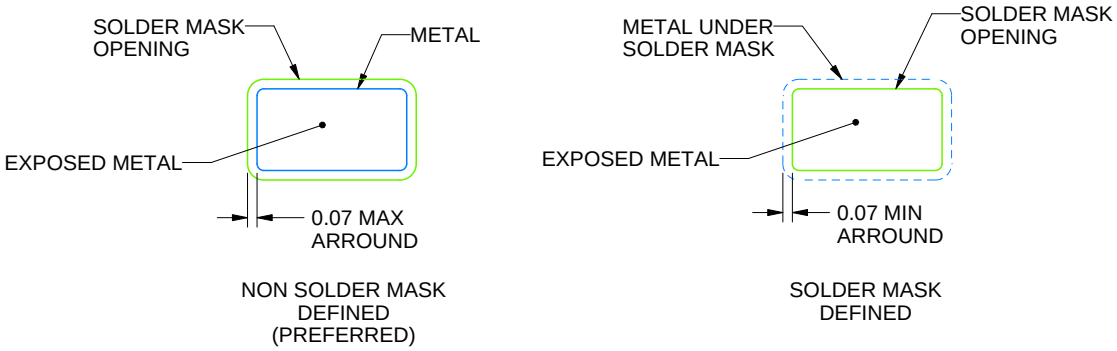
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

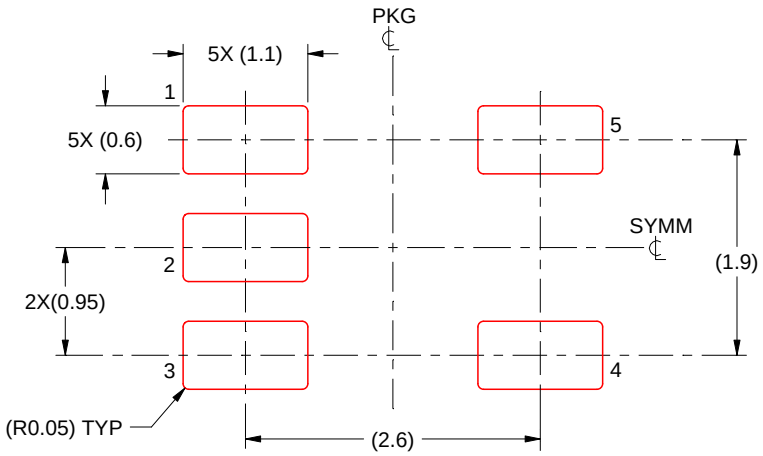


SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



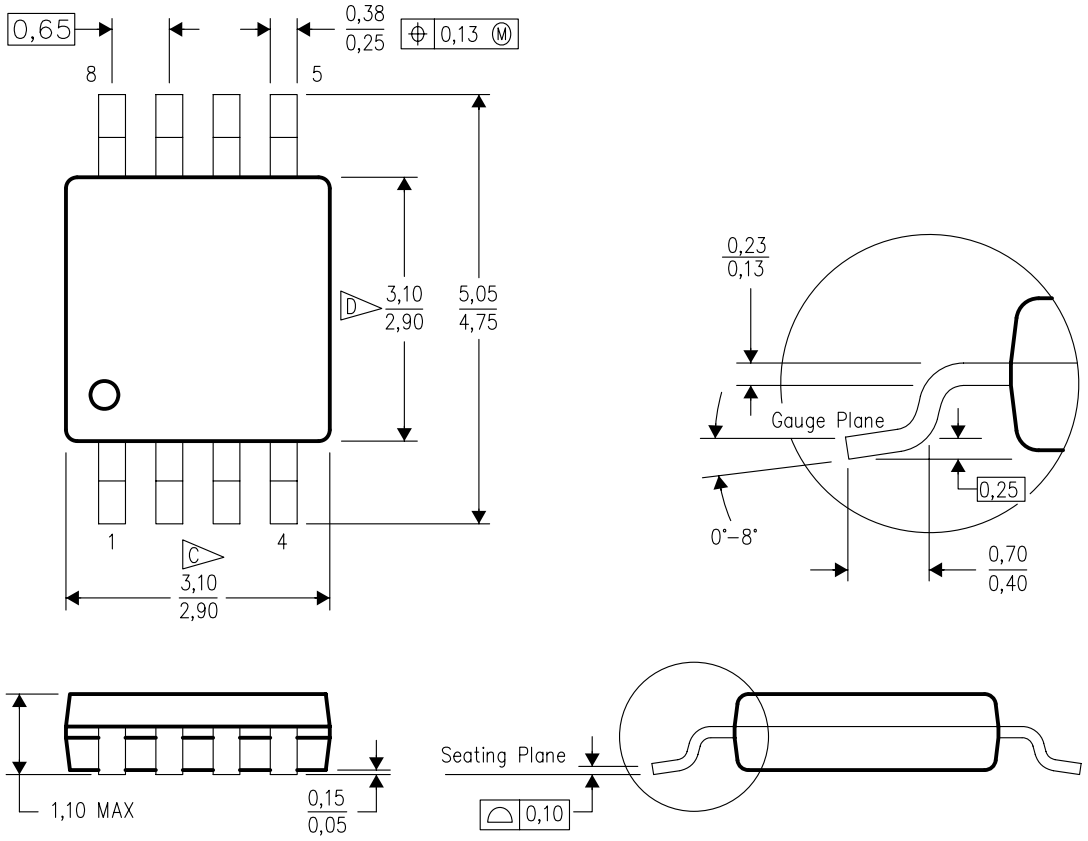
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

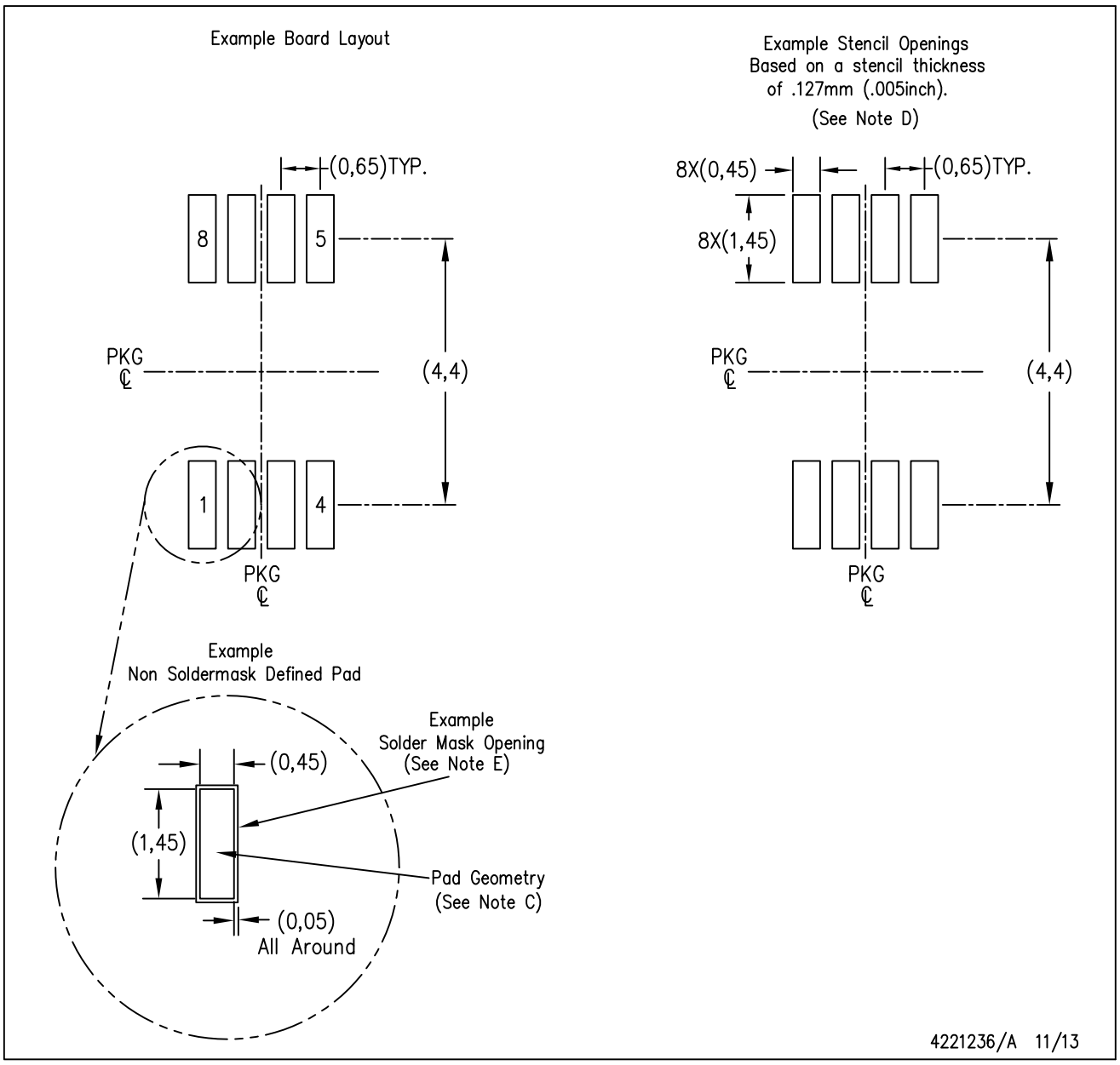
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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