

30V N-Channel NexFET™ Power MOSFET

Check for Samples: [CSD17303Q5](#)

FEATURES

- Optimized for 5V Gate Drive
- Ultralow Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

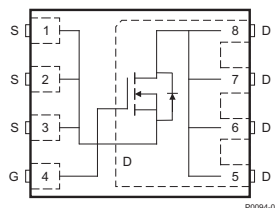
APPLICATIONS

- Notebook Point-of-Load
- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems
- Optimized for Synchronous FET Applications

DESCRIPTION

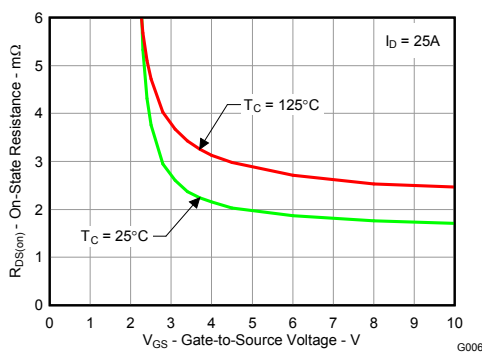
The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications, and optimized for 5V gate drive applications.

Top View



P0094-01

$R_{DS(on)}$ vs V_{GS}



PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	30	V
Q_g	Gate Charge Total (4.5V)	18	nC
Q_{gd}	Gate Charge Gate to Drain	4	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V$	2.7 mΩ
		$V_{GS} = 4.5V$	2 mΩ
		$V_{GS} = 8V$	1.7 mΩ
$V_{GS(th)}$	Threshold Voltage	1.1	V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD17303Q5	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

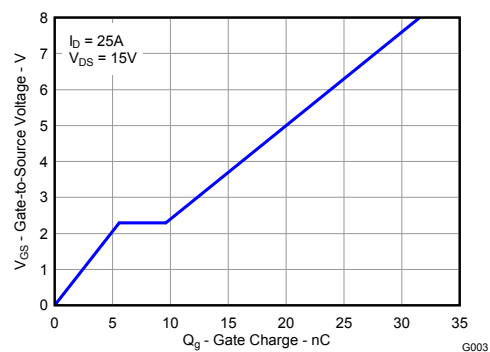
ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	+10 / -8	V
I_D	Continuous Drain Current, $T_C = 25^\circ\text{C}$	100	A
	Continuous Drain Current ⁽¹⁾	32	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ ⁽²⁾	200	A
P_D	Power Dissipation ⁽¹⁾	3.2	W
T_J , T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche Energy, single pulse $I_D = 103A$, $L = 0.1mH$, $R_G = 25\Omega$	530	mJ

(1) $R_{\theta JA} = 39^\circ\text{C/W}$ on 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

GATE CHARGE



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

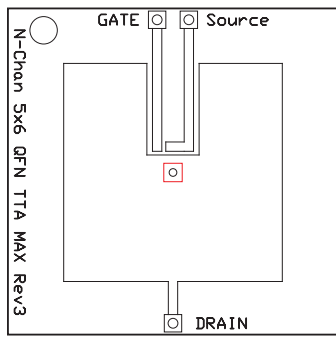
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
Static Characteristics								
BV _{DSS}	Drain to Source Voltage	V _{GS} = 0V, I _D = 250μA	30			V		
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 24V				1 μA		
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = +10/−8V				100 nA		
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	0.9	1.1	1.6	V		
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 3V, I _D = 25A	2.7			3.7 mΩ		
		V _{GS} = 4.5V, I _D = 25A	2			2.6 mΩ		
		V _{GS} = 8V, I _D = 25A	1.7			2.4 mΩ		
g _{fs}	Transconductance	V _{DS} = 15V, I _D = 25A	114			S		
Dynamic Characteristics								
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz	2630			3420 pF		
C _{oss}	Output Capacitance		1440			1870 pF		
C _{rss}	Reverse Transfer Capacitance		83			108 pF		
R _G	Series Gate Resistance		1.4			2.8 Ω		
Q _g	Gate Charge Total (4.5V)	V _{DS} = 15V, I _{DS} = 25A	18			23 nC		
Q _{gd}	Gate Charge Gate to Drain		4			nC		
Q _{gs}	Gate Charge Gate to Source		5.6			nC		
Q _{g(th)}	Gate Charge at V _{th}		3			nC		
Q _{oss}	Output Charge	V _{DS} = 13.7V, V _{GS} = 0V	34			nC		
t _{d(on)}	Turn On Delay Time	V _{DS} = 15V, V _{GS} = 4.5V, I _{DS} = 25A, R _G = 2Ω	11.4			ns		
t _r	Rise Time		16			ns		
t _{d(off)}	Turn Off Delay Time		27			ns		
t _f	Fall Time		10.4			ns		
Diode Characteristics								
V _{SD}	Diode Forward Voltage	I _{SD} = 25A, V _{GS} = 0V	0.8			1 V		
Q _{rr}	Reverse Recovery Charge	V _{DD} = 13.7V, I _F = 25A, di/dt = 300A/μs	50			nC		
t _{rr}	Reverse Recovery Time		33			ns		

THERMAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

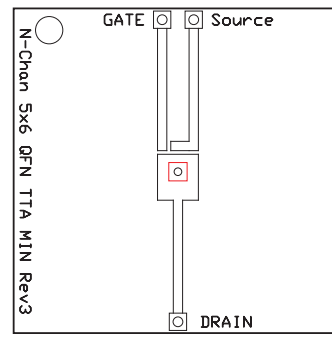
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case ⁽¹⁾			1.1	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			49	$^\circ\text{C/W}$

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch $\times$ 1.5-inch (3.81-cm $\times$ 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



M0137-01

Max $R_{\theta JA} = 49^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.

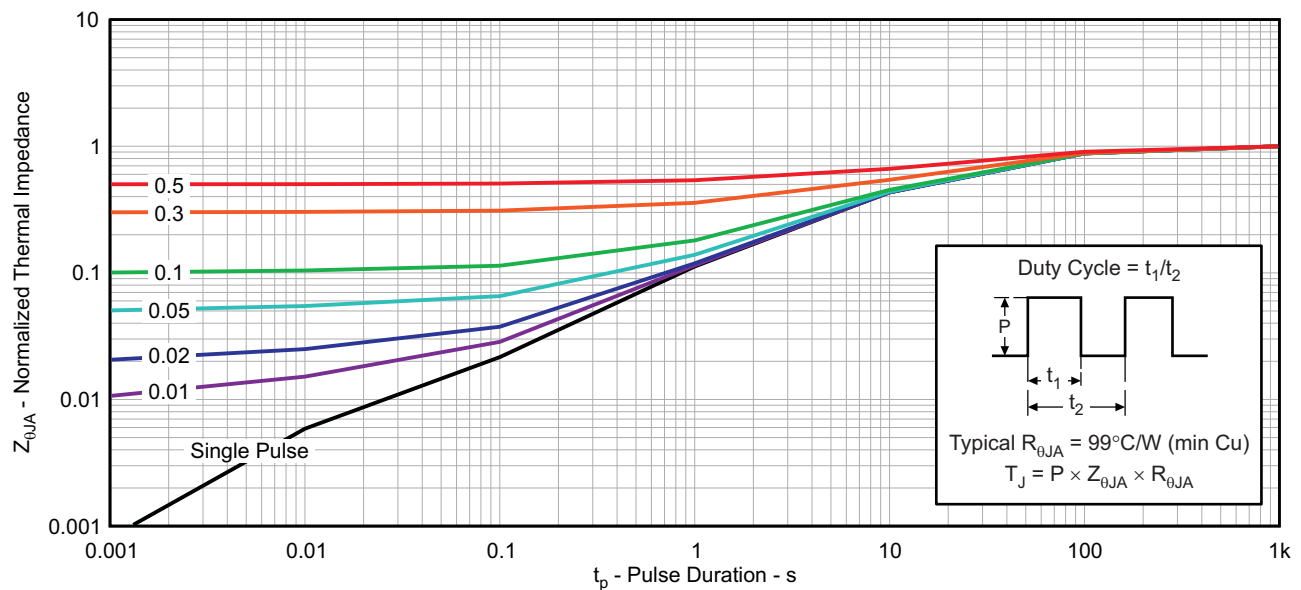


M0137-02

Max $R_{\theta JA} = 124^{\circ}\text{C/W}$
when mounted on
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

TYPICAL MOSFET CHARACTERISTICS

$T_A = 25^{\circ}\text{C}$, unless otherwise specified



G012

Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, unless otherwise specified

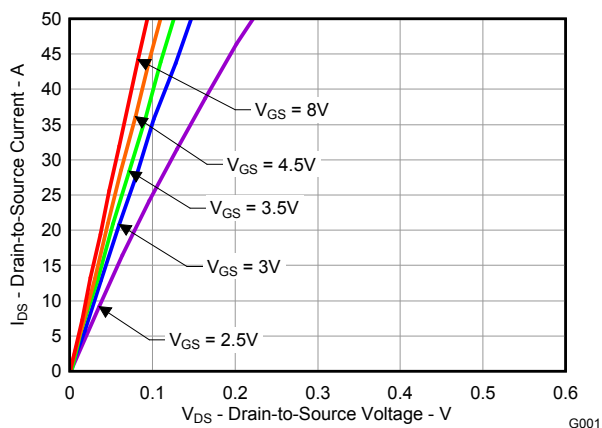


Figure 2. Saturation Characteristics

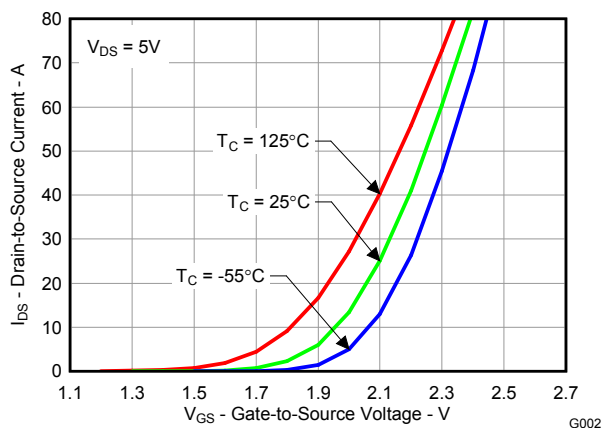


Figure 3. Transfer Characteristics

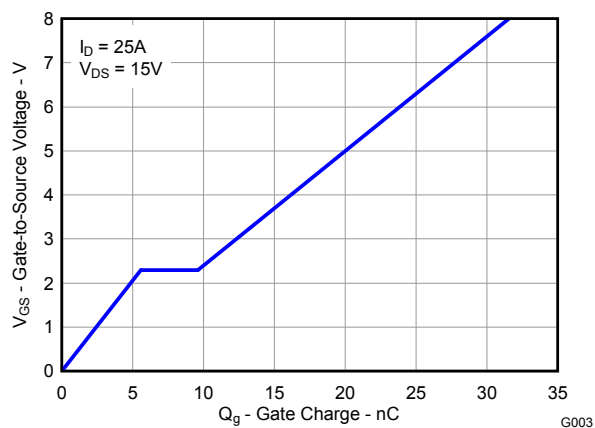


Figure 4. Gate Charge

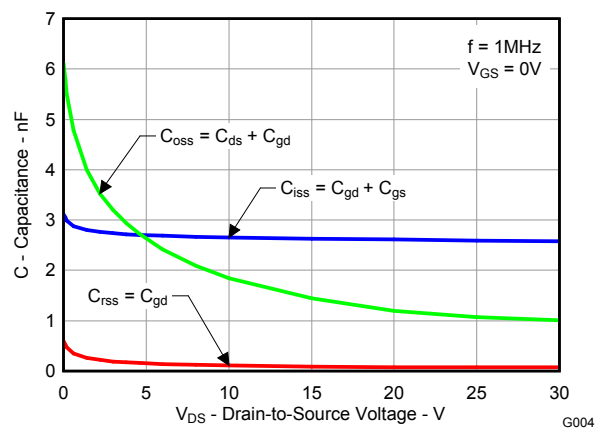


Figure 5. Capacitance

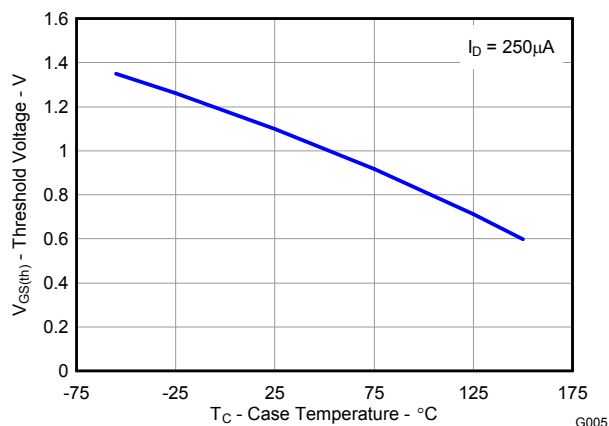


Figure 6. Threshold Voltage vs. Temperature

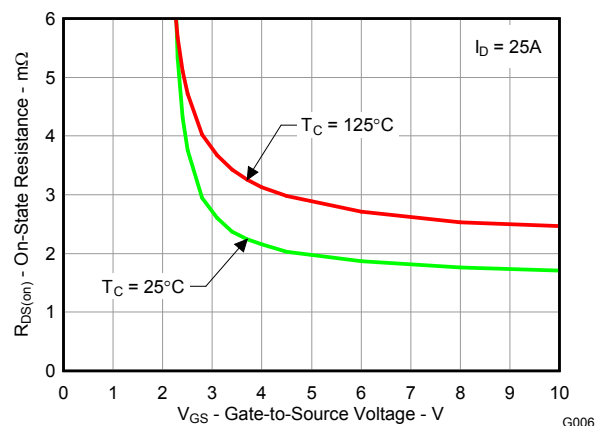


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, unless otherwise specified

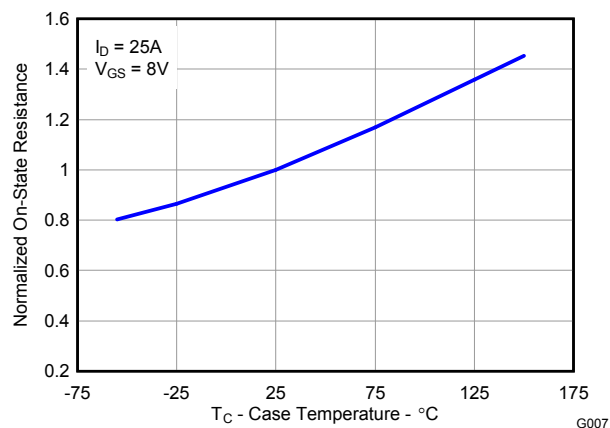


Figure 8. Normalized On-State Resistance vs. Temperature

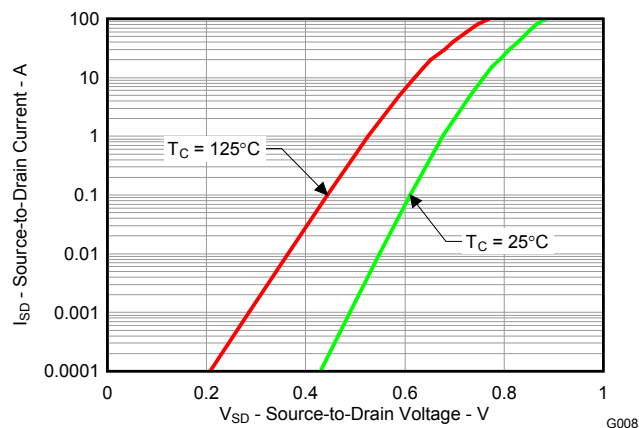


Figure 9. Typical Diode Forward Voltage

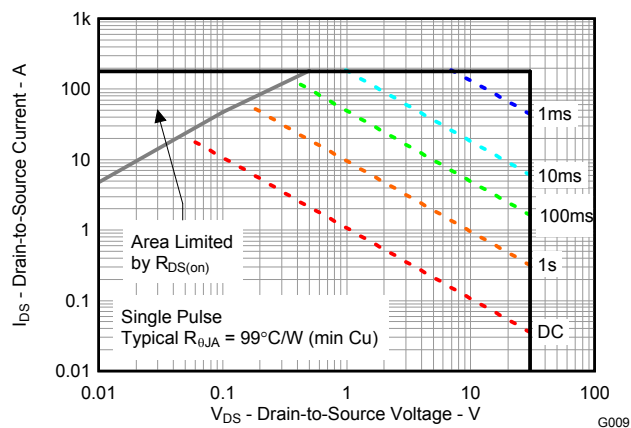


Figure 10. Maximum Safe Operating Area

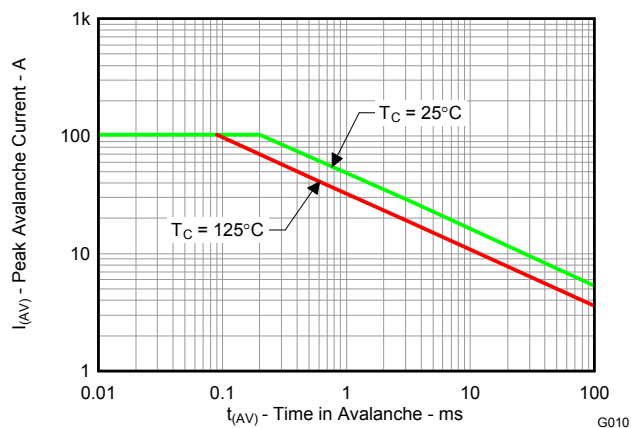


Figure 11. Single Pulse Unclamped Inductive Switching

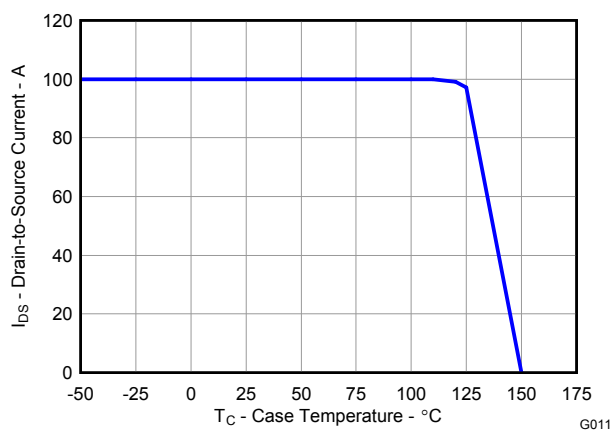
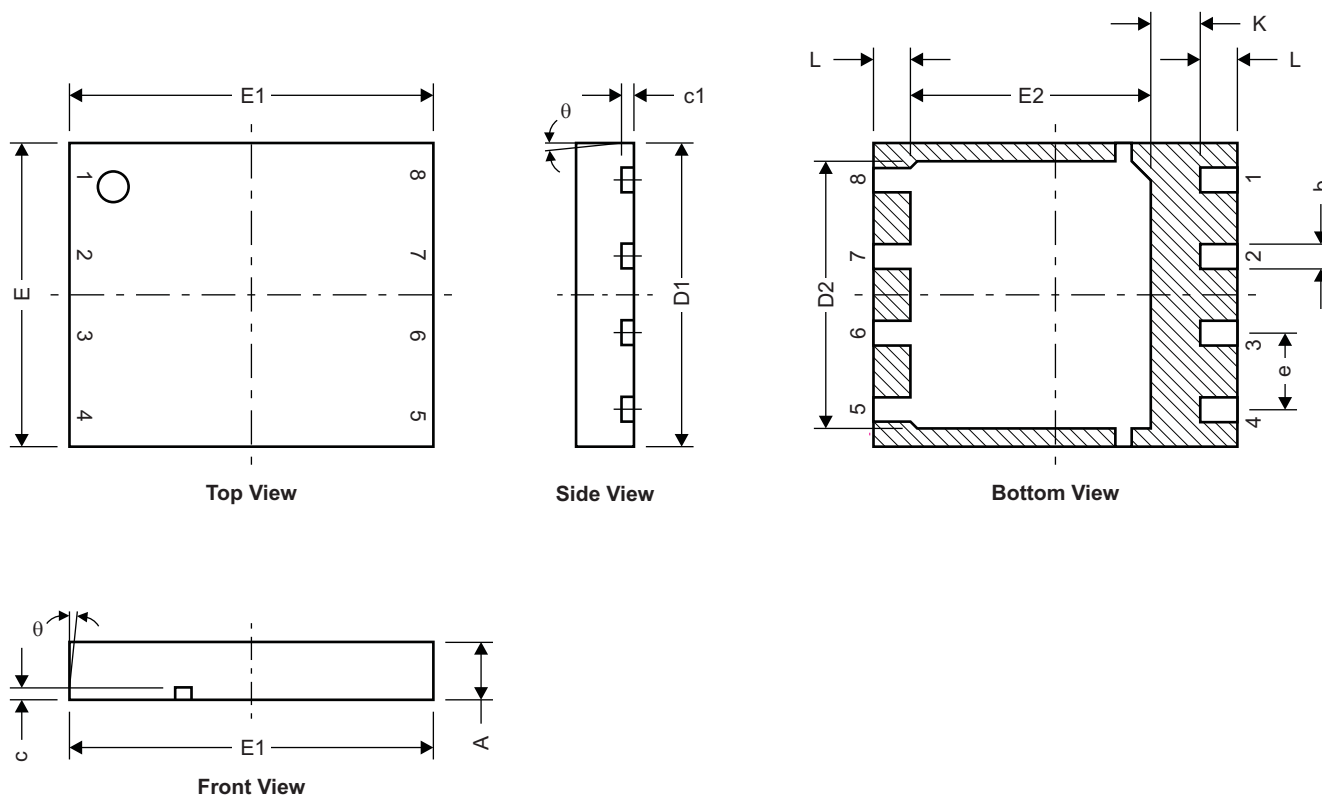


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

Q5 Package Dimensions



M0140-01

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 TYP		0.050	
K	0.760		0.030	
L	0.510	0.710	0.020	0.028
θ	0.00			



For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

Technical drawing of a rectangular plate with mounting holes. The drawing includes a side view on the left and a top view on the right.

Side View (Left):

- Dimension $K0$ is indicated for the top flange.
- Dimension 0.30 ± 0.05 is indicated for the thickness of the top flange.
- Dimension $R 0.30 \text{ MAX}$ is indicated for the rounded bottom corner.

Top View (Right):

- Overall width is 12.00 ± 0.30 .
- Overall height is 5.50 ± 0.05 .
- Distance from the top edge to the center of the first row of holes is 1.75 ± 0.10 .
- Distance between the centers of the first and second rows of holes is 4.00 ± 0.10 (See Note 1).
- Distance from the left edge to the center of the first hole is 2.00 ± 0.05 .
- Distance between the centers of the first and second holes in the first row is $A0$.
- Distance between the centers of the first and second holes in the second row is 8.00 ± 0.10 .
- Distance from the bottom edge to the center of the first row of holes is $B0$.
- Distance from the bottom edge to the center of the second row of holes is 5.50 ± 0.05 .
- Dimension $R 0.30 \text{ TYP}$ is indicated for the rounded corners.
- Dimension $\varnothing 1.50 \text{ MIN}$ is indicated for the minimum hole diameter.
- Dimension $\varnothing 1.50 \text{ }^{+0.10}_{-0.00}$ is indicated for the maximum hole diameter.

Notes:

- $A0 = 6.50 \pm 0.10$
- $B0 = 5.30 \pm 0.10$
- $K0 = 1.40 \pm 0.10$

M0138-01

1. 10-sprocket hole-pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. Thickness: $0.30 \pm 0.05\text{mm}$
6. MSL1 260°C (IR and convection) PbF reflow compatible

REVISION HISTORY

Changes from Original (January 2010) to Revision A	Page
--	------

- | | |
|--|-------------------|
| • Changed the Abs Max Ratings table, Avalanche Energy, single pulse From: $I_D = 85A$, $L = 0.1mH$, $R_G = 25\Omega$ Value = 361 To: $I_D = 103A$, $L = 0.1mH$, $R_G = 25\Omega$ Value = 530 | 1 |
| • Changed Figure 11 | 5 |
-

Changes from Revision A (February 2010) to Revision B	Page
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- | | |
|---|-------------------|
| • Deleted the Package Marking Information section | 7 |
|---|-------------------|
-

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17303Q5	ACTIVE	VSON-CLIP	DQH	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD17303	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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