![Texas Instruments logo]
**TEXAS INSTRUMENTS**
www.ti.com

**bq29311**

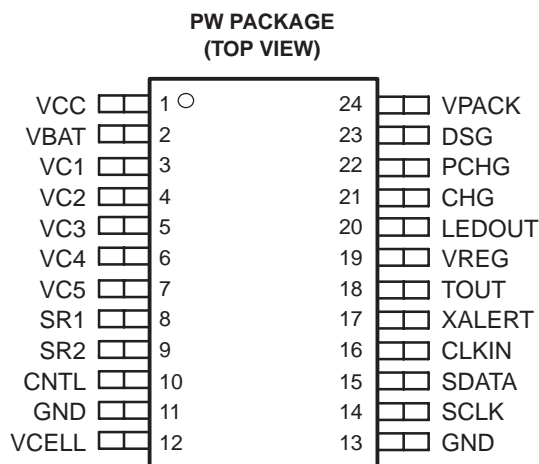# THREE- AND FOUR-CELL LITHIUM-ION OR LITHIUM-POLYMER BATTERY PROTECTION IC

## FEATURES

- **3- or 4-Cell Series Protection Control**
- **Autonomous Overcurrent and Short Circuit Protection**
- **Provides Individual Cell Voltages to Battery Management Host**
- **Integrated Cell Balancing Control**
- **I²C Compatible User Interface Allows Access to Battery Information**
- **User Control to Initiate Protection**
- **Integrated 3.3-V 25-mA LDO**
- **Programmable Shutdown and Brownout Control**
- **Provides Drive for Three External FETs**
- **Low Supply Current of 140 μA Typical**
- **Programmable Threshold and Delay for Short-Circuit Current Protection**
- **Provides Drive for Three External FETs**
- **Can Directly Interface With bq2083/5 for Complete Battery Management Solution**

## APPLICATIONS

- **Notebook Computer Battery Packs**
- **Test Equipment**

## PIN ASSIGNMENTS

**PW PACKAGE**
**(TOP VIEW)**

| | | |
|---|---|---|
| VCC | 1 | 24 VPACK |
| VBAT | 2 | 23 DSG |
| VC1 | 3 | 22 PCHG |
| VC2 | 4 | 21 CHG |
| VC3 | 5 | 20 LEDOUT |
| VC4 | 6 | 19 VREG |
| VC5 | 7 | 18 TOUT |
| SR1 | 8 | 17 XALERT |
| SR2 | 9 | 16 CLKIN |
| CNTL | 10 | 15 SDATA |
| GND | 11 | 14 SCLK |
| VCELL | 12 | 13 GND |

## DESCRIPTION

The bq29311 is a three- or four-cell lithium-ion battery pack protection analog front end (AFE) IC that incorporates a 3.3-V 25-mA low-dropout regulator (LDO) and an I²C compatible interface to extract battery parameters such as cell voltages and control output status. Other parameters, such as overcurrent protection threshold and delay, can also be programmed into the bq29311 to increase the flexibility of the battery management system.

The bq29311 provides safety protection in overcurrent, short circuit, overvoltage, and undervoltage conditions via control from the battery management host. In overcurrent and short-circuit conditions the bq29311 can directly activate the FET drive as a secondary protection level. The communications interface allows the host to control and observe the current status of the protection, to set overcurrent and overload levels, to set the overcurrent and overload blanking delay time, short-circuit threshold levels, and short-circuit blanking delay time, and to program for the VREG shutdown voltage and brownout-detection thresholds.

Each cell is balanced by a discharge path, which is enabled by the internal control registers accessible through the I²C compatible interface. The maximum current is set by an external series resistor with an absolute maximum value of 10 mA discharge current per cell.

## ORDERING INFORMATION

| $T_A$ | PACKAGED TSSOP (PW) |
|---|---|
| −25°C to 85°C | bq29311PW |
| | bq29311PWR[1] |

[1] R suffix indicates tape and reel.

⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**Not Recommended for New Designs**

TEXAS
INSTRUMENTS
www.ti.com

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## PACKAGE DISSIPATION RATINGS

| PACKAGE | $T_A \leq 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| PW | 874 mW | 6.99 W/°C | 559 mW | 454 mW |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1]

| | | bq29311 |
|---|---|---|
| Supply voltage range[2] | $V_{CC}$, VPACK | −0.3 V to 34 V |
| Input voltage range | VC1, VC2, VC3, VC4, VBAT | −0.3 V to 34 V |
| | VC5, SR1, SR2 | −1 V to 1 V |
| | VC1 to VC2, VC2 to VC3, VC3 to VC4, VC4 to VC5 | −0.3 V to 8.5 V |
| | CLK-IN, SCLK, SDATA | −0.3 V to 7 V |
| | CNTL | −0.3 V to 34 V |
| Output voltage range | DSG, CHG, PCHG | −0.3 V to $V_{CC}$ |
| | LEDOUT, TOUT, SCLK, SDATA, VCELL, XALERT | −0.3 V to 7 V |
| Current for cell balancing | | 10 mA |
| Continuous total power dissipation | | See Dissipation Rating Table |
| ESD rating[3] | HBM | 1.5 kV |
| | CDM | 250 V |
| | MM | 50 V |
| Operating free-air temperature range, $T_A$ | | −25°C to 85°C |
| Storage temperature range, $T_{stg}$ | | −65°C to 150°C |
| Lead temperature (soldering, 10 s) | | 260°C |

[1] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
[2] All voltages are with respect to ground of this device except VCn-VC(n+1), where n = 1, 2, 3, 4 cell voltage.
[3] Design considerations should be made with respect to excessive ESD.

## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply voltage ($V_{CC}$ or VPACK) | | | | | 25 | V |
| Input voltage range, $V_I$ | | VBAT | 0 | | $V_{CC}$ | V |
| | | VC1, VC2, VC3, VC4 | 0 | | $V_{CC}$ | |
| | | SR1, SR2, VC5 | −0.5 | | 0.5 | |
| | | VCn−VC(n+1), (n = 1, 2, 3, 4 ) | 0 | | 5 | |
| | | CNTL | | | VREG | |
| Logic level input voltage | $V_{IH}$ | SCLK, SDATA, CLK–IN | 0.8×VREG | | VREG | V |
| | $V_{IL}$ | | 0 | | 0.2×VREG | |
| Output current, $I_O$ | | XALERT | | | 200 | µA |
| | | SDATA | | | 50 | |
| | | VCELL | | | ±10 | |
| Input current, $I_I$ | | CNTL | −0.5 | | 1 | µA |
| External 3.3-V VREG capacitor, $C_{(REG)}$ | | VREG | | 1 | | µF |
| Operating ambient temperature range, $T_A$ | | | −25 | | 85 | °C |

## ELECTRICAL CHARACTERISTICS

$T_A$ = 25°C, $C_{REG}$ = 1 µF, $V_{CC}$ = 14 V (unless otherwise noted)

### SUPPLY CURRENT

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{(CC1)}$ | Supply current 1 | No load at VREG, TOUT, LEDOUT, XALERT, SCLK, SDATA. CLKIN not used | $T_A$ = 25°C | | 140 | 190 | µA |
| | | | $T_A$ = −25°C to 85°C | | | 220 | |
| $I_{(CC2)}$ | Supply current 2 | VBAT ≤ $V_{SD}$, VPACK = 0 DSG, CHG and PCHG = off | $T_A$ = −25°C to 85°C | | | 1 | µA |

### 3.3 V REGULATOR

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{(REG)}$ | Regulator output voltage | $I_O$ ≤ 25 mA, | $T_A$ = −25°C to 85°C | 3.135 | 3.3 | 3.465 | V |
| $\Delta V_{(REGTEMP)}$ | Regulator output change with temperature | $V_{(SD)}$ = 6.5 V ≤ $V_{CC}$ ≤ 25 V, $I_O$ = 25 mA | $T_A$ = −25°C to 25°C | | ±0.2% | ±1.74% | |
| | | | $T_A$ = 25°C to 85°C | | ±0.2% | ±1.74% | |
| $\Delta V_{(REGLINE)}$ | Line regulation | $V_{(SD)}$ =6.5 V ≤ $V_{CC}$ ≤ 25V, | $I_O$ = 25 mA | | 6 | 20 | mV |
| $\Delta V_{(REGLOAD)}$ | Load regulation | 0.1 mA ≤ $I_O$ ≤ 25 mA, | $V_{CC}$ = 14 V | | 2 | 20 | mV |

### SHUTDOWN $V_I$ MONITOR

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(SD)}$ | VREG shutdown threshold range[1] | Measured at VBAT | 6.475 | | 10.975 | V |
| $\Delta V_{(SD)}$ | Shutdown threshold steps | Set by SDV register b0–b3 | | 300 | | mV |
| $V_{hys(SD)}$ | Hysteresis | | 35 | 50 | 65 | mV |
| | Accuracy of the shutdown threshold | | | | ±5% | |

(1) $V_{(SD)}$ = $V_{(REG)}$ brownout threshold voltage as determined by b0–b3 in the SDV register.

### BROWNOUT $V_{IN}$ MONITOR

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{BO}$ | Brownout threshold range[1] | Measured at VBAT | 7.975 | | 12.475 | V |
| $\Delta V_{BO}$ | Brownout threshold steps | Set by SDV register b4 – b7 | | 300 | | mV |
| $V_{hys(BO)}$ | Hysteresis | | 35 | 50 | 65 | mV |
| | Brownout threshold accuracy | | | | ±5% | |

(1) $V_{BO}$ = $V_{(REG)}$ brownout threshold voltage as determined by b4–b7 in the SDV register.

### CELL VOLTAGE MONITOR

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(CELL\_OUT)}$ | VCELL output (see Note 4) | $V_{(CELL\_IN)}$ = 0 V | | 0.975 | | V |
| | | $V_{(CELL\_IN)}$ = 4.5 V | | 0.3 | | |
| $V_{(CELL\_IN)}$ | Differential Input voltage range | VC1 to VC2, VC2 to VC3, VC3 to VC4, VC4 to VC5 | 0 | | 4.5 | V |
| K | VCELL scale factor | [0.975 −$V_{(CELL\_OUT)}$]/$V_{(CELL\_IN)}$ | 0.144 | 0.150 | 0.156 | |
| $R_{(BAL)}$ | Cell balance internal resistance | $RDS_{(ON)}$ for internal FET switch at $V_{(DS)}$ = 2 V | | 500 | | Ω |

(1) The $V_{(CELL)}$ output is inversely proportional to the $V_{(CELL\_OUT)}$ = −K × $V_{(CELL\_IN)}$ + 0.975.

**TEXAS INSTRUMENTS**
www.ti.com

**bq29311**

SLUS487D – DECEMBER 2001 – REVISED NOVEMBER 2003

## ELECTRICAL CHARACTERISTICS   CONTINUED

$T_A$ = 25°C, $C_{REG}$ = 1 µF, $V_{CC}$ = 14 V (unless otherwise noted)

### OVERCURRENT (OC) AND SHORT CIRCUIT (SC) DETECTION

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{(OCD)}$ | OC detection threshold range, typical[1] | Charge (overcurrent) | | 50 | | 205 | mV |
| | | Discharge (overload) | | −50 | | −205 | |
| $\Delta V_{(OCD)}$ | OC detection threshold program step | Charge (overcurrent) | | | 5 | | mV |
| | | Discharge (overload) | | | −5 | | |
| $V_{hys(OCD)}$ | OC detection threshold hysteresis | Charge and discharge (overcurrent and overload) | | 7 | 10 | 13 | mV |
| $V_{(SC)}$ | SC detection threshold range, typical[2] | Charge | | 100 | | 475 | mV |
| | | Discharge | | −100 | | −475 | |
| $\Delta V_{(SC)}$ | SC detection threshold program step | Charge | | | 25 | | mV |
| | | Discharge | | | −25 | | |
| $V_{hys(SC)}$ | SC detection threshold hysteresis | Charge and discharge | | 40 | 50 | 60 | mV |
| $V_{(OCD\_acr)}$ | OC detection threshold accuracy[1] | Charge and discharge | $V_{(OCD)}$ = 50 mV (min) | 37.5 | 50 | 62.5 | mV |
| | | | $V_{(OCD)}$ = 100 mV | 85 | 100 | 115 | |
| | | | $V_{(OCD)}$ = 205 mV (max) | 174 | 205 | 236 | |
| $V_{(SC\_acr)}$ | SC detection threshold accuracy[2] | Charge and discharge | $V_{(SC)}$ = 100 mV (min) | 75 | 100 | 125 | mV |
| | | | $V_{(SC)}$ = 200 mV | 170 | 200 | 230 | |
| | | | $V_{(SC)}$ = 475 mV (max) | 403 | 475 | 547 | |

(1) See OCVD and OCVC registers for setting detection threshold.
(2) See SCV register for setting detection threshold.

### FET DRIVE CIRCUIT

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{(FETOL)}$ | Output voltage | VBAT = 16 V | DSG | 1 | 5 | 7 | V |
| | | VPACK = 16 V | CHG | 1 | 5 | 7 | |
| | | VPACK = 16 V | PCHG | 8.5 | 10.5 | 11.5 | |
| $V_{(FETCLAMP)}$ | Output clamp voltage | VPACK =  4.5 V | PCHG | 3.3 | 3.5 | 3.7 | V |
| $t_r$ | Rise time | $C_L$ = 4700 pF,   10% to 90% | DSG | | 10 | 100 | µs |
| | | | CHG | | 10 | 100 | |
| | | | PCHG | | 170 | 500 | |
| $t_f$ | Fall time | $C_L$ = 4700 pF,   90% to 10% | DSG | | 15 | 100 | µs |
| | | | CHG | | 15 | 100 | |
| | | | PCHG | | 170 | 500 | |

### THERMISTOR DRIVE AND LED DRIVE

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{(t)}$ | TOUT pass-element series resistance | $I_O$ = −1 mA at TOUT pin, $R_{(t)}$ = ($V_{REG}$ − $V_{TOUT}$)/1 mA, $T_A$ = −25°C to 85°C | | 50 | 100 | Ω |
| $V_{(LEDOUT)}$ | LEDOUT output voltage | $I_O$ = −25 mA at LEDOUT pin, $T_A$ = −25°C to 85°C | 2.9 | 3.15 | 3.46 | V |

### LOGIC

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $R_{(PUP)}$ | Internal pullup resistance | XALERT, CLKIN | | 60 | 100 | 140 | kΩ |
| | | SDATA, SCLK | $T_A$ = −25°C to 85°C | 6 | 10 | 14 | |
| $V_{O(L)}$ | Logic low-level output voltage | XALERT, $I_{OUT}$ = 200 µA | | | | 0.2 | V |
| | | SDATA, $I_{OUT}$ = 50 µA | | | | 0.4 | |

## ELECTRICAL CHARACTERISTICS   CONTINUED

$T_A$ = 25°C, $C_{REG}$ = 1 µF, $V_{CC}$ = 14 V (unless otherwise noted)

| AC | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | | **TEST CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNIT** |
| $f_{(CLKIN)}$ | CLKIN input frequency | External clock | 32.100 | 32.768 | 33.420 | kHz |
| $t_{(CLKIN\_HI)}$ | CLKIN high time | External clock | 2 | | 28 | µs |
| $f_{(INTERNAL)}$ | Internal clock frequency | $T_A$ = −25°C to 85°C | 26.2 | 32.768 | 39.4 | kHz |
| $t_{(SCDDELAY)}$ | SC delay time | $t_{d(SC)}$ = 0 ms for charge and discharge $V_{(OCD)}$ = 100 mV, SR(50%) to DSG/CHG(50%) delay. No load. | | 1 | 10 | µs |

## Terminal Functions

| TERMINAL | | DESCRIPTION |
|---|---|---|
| **NAME** | **NO.** | |
| CHG | 21 | Push-pull output charge FET gate voltage supply |
| CLKIN | 16 | Digital input that provides an alternate clock with internal 100-kΩ pullup to VREG |
| CNTL | 10 | Active low input enables CHG, DSG and PCHG. Internal pullup |
| DSG | 23 | Push-pull output discharge FET gate voltage supply |
| GND | 11, 13 | Analog ground pin and negative pack terminal |
| LEDOUT | 20 | Provides current to drive LED capacity display |
| PCHG | 22 | Push-pull output precharge FET gate voltage supply |
| SCLK | 14 | Open-drain bidirectional serial interface clock with internal 10-kΩ pullup to VREG |
| SDATA | 15 | Open-drain bidirectional serial interface data with internal 10-kΩ pullup to VREG |
| SR1 | 8 | Current sense positive terminal when charging relative to SR2 |
| SR2 | 9 | Current sense positive terminal when discharging relative to SR1 |
| TOUT | 18 | Provides thermistor bias current |
| VBAT | 2 | Battery positive terminal sense input for regulator shutdown |
| VC1 | 3 | Sense voltage input terminal for most positive cell and balance current input for most positive cell. Connected to VC2 in 3-cell applications |
| VC2 | 4 | Sense voltage input terminal for second most positive cell, balance current input for second most positive cell, and return balance current for most positive cell |
| VC3 | 5 | Sense voltage input terminal for third most positive cell, balance current input for third most positive cell and return balance current for second most positive cell |
| VC4 | 6 | Sense voltage input terminal for least positive cell, balance current input for least positive cell, and return balance current for third most positive cell |
| VC5 | 7 | Sense voltage input terminal for most negative cell, return balance current for least positive cell |
| VCC | 1 | Diode protected BAT+ terminal and primary power source |
| VCELL | 12 | Output of scaled value of the measured cell voltage |
| VPACK | 24 | Pack positive terminal and alternate power source |
| VREG | 19 | Integrated 3.3-V regulator output |
| XALERT | 17 | Open-drain output used to indicate status register changes. With internal 100 kΩ pullup to VREG |

**bq29311**

SLUS487D – DECEMBER 2001 – REVISED NOVEMBER 2003

## FUNCTIONAL BLOCK DIAGRAM
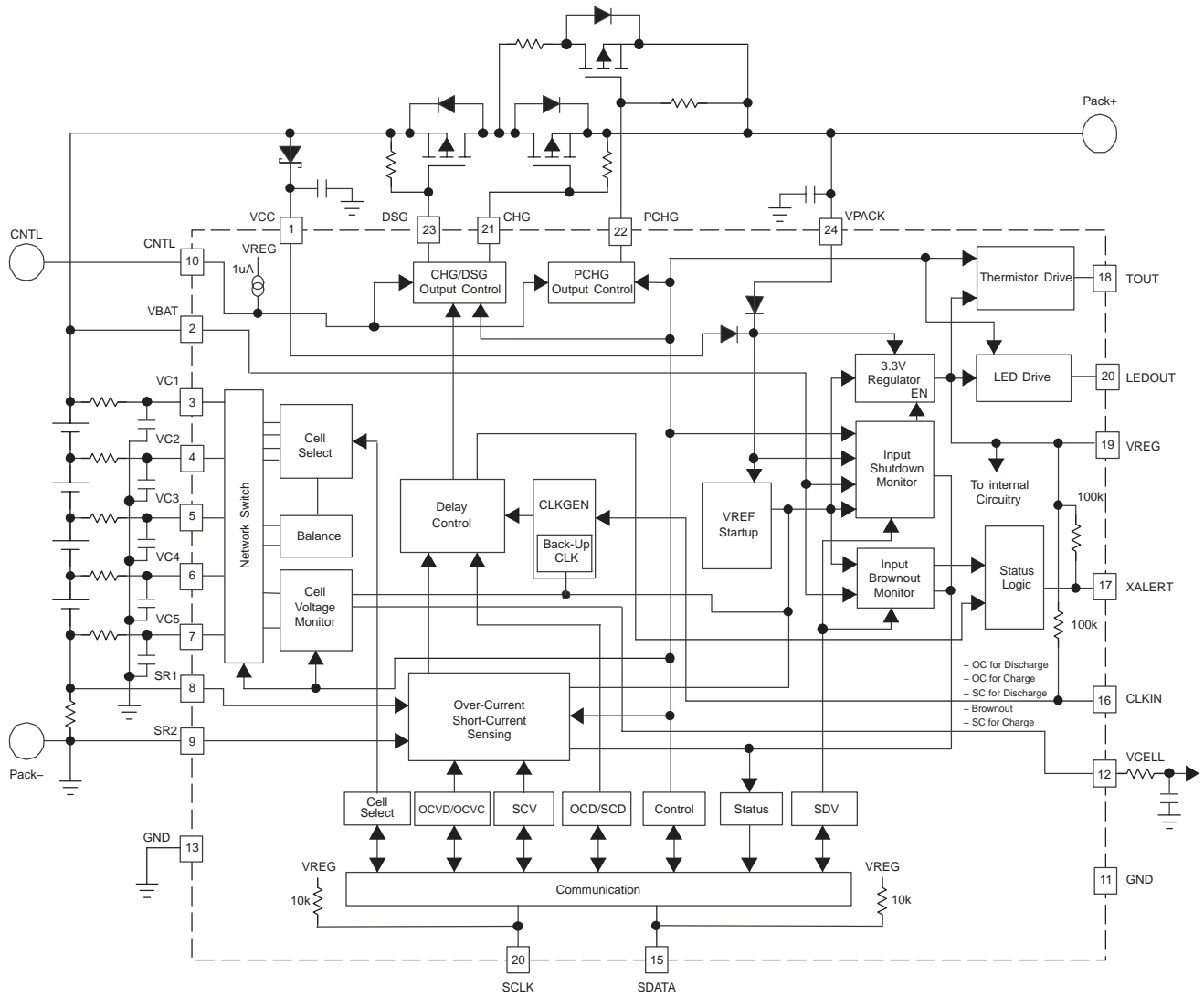
## AC TIMING SPECIFICATIONS (I²C COMPATIBLE SERIAL INTERFACE)
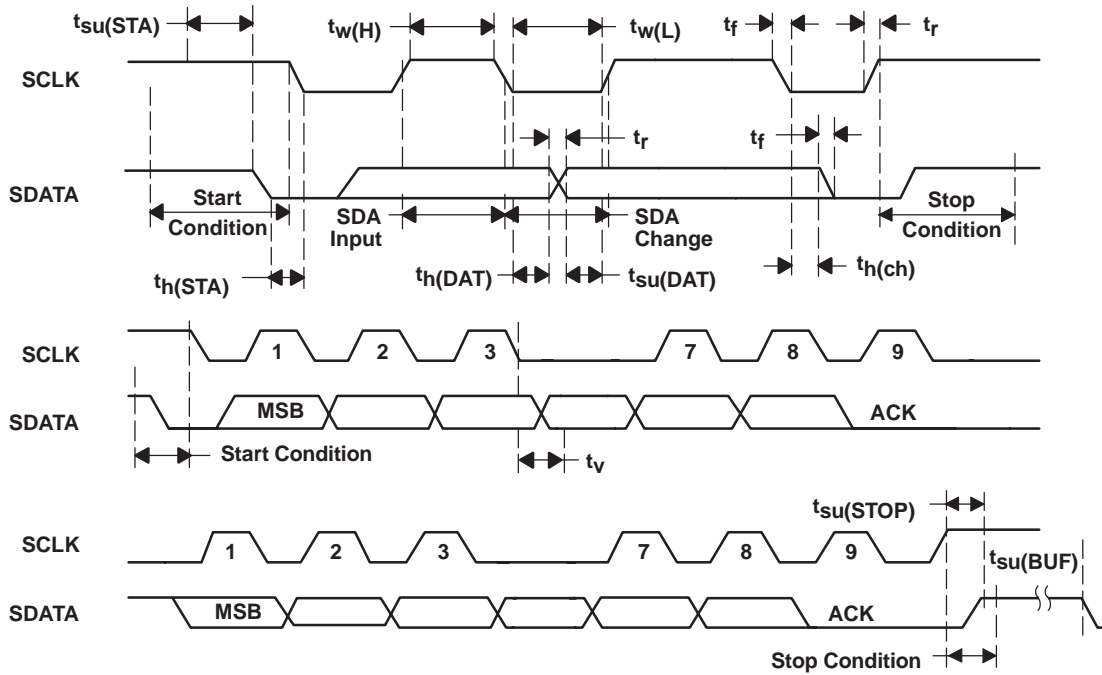


| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_r$ | Clock rise time | | 300 | ns |
| $t_f$ | Clock fall time | | 300 | ns |
| $t_{r(SDA)}$ | SDA rise time | 20 | 300 | ns |
| $t_{f(SDA)}$ | SDA fall time | 20 | 300 | ns |
| $t_{su(STA)}$ | Clock high to input transition setup time | 600 | | ns |
| $t_{w(H)}$ | Clock pulse width high | 600 | | ns |
| $t_{h(STA)}$ | Input low to clock low hold time start condition | 600 | | ns |
| $t_{h(DAT)}$ | Clock low to input transition hold time | 0 | | µs |
| $t_{w(L)}$ | Clock pulse width low | 1.3 | | µs |
| $t_{su(DAT)}$ | Input transition to clock transition setup time | 100 | | ns |
| $t_{su(STOP)}$ | Clock high to input high (STOP) setup time stop condition | 600 | | ns |
| $t_{su(BUF)}$ | Input high to input low (bus free) | 1.3 | | µs |
| $t_v$ | Clock low to data out valid time | 200 | 900 | ns |
| $t_{h(CH)}$ | Data out hold time after clock low | 200 | | ns |
| $f_{(CLK)}$ | Clock frequency | | 100 | kHz |

**TEXAS INSTRUMENTS**
www.ti.com

**bq29311**

SLUS487D – DECEMBER 2001 – REVISED NOVEMBER 2003

## APPLICATION INFORMATION

### PRECHARGE MODE CURRENT LIMITING RESISTOR SELECTION

The selection of this resistor value should take into account the maximum potential charge voltage, which should include the voltage of a failed charger to ensure that 0-V and pre-charge mode current levels are within desirable limits under all conditions.
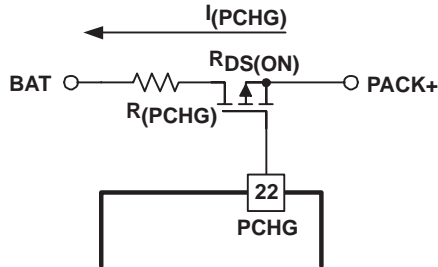
$$I_{(PCHG)} = \frac{V_{PACK(max)} - V_{BAT(min)}}{R_{DS(ON)} + R_{(PCHG)}}$$

UDG−01148

**Figure 1. Pre-Charge Mode Current Limiting Resistor Selection**

This method ensures that the resistor is sized correctly to provide safe zero voltage charging and the optimal performance during precharge.
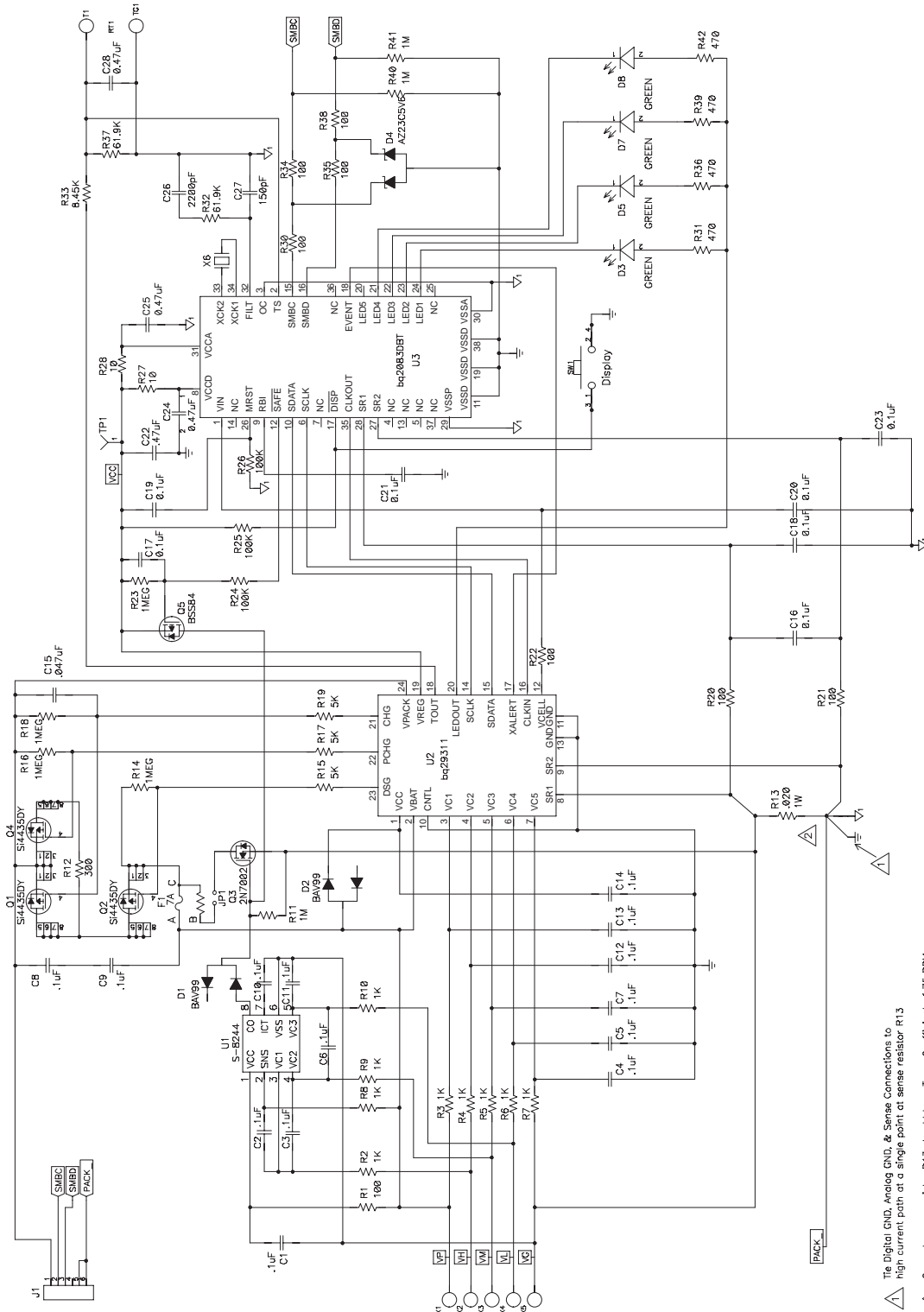
**Figure 2. bq29311 Application Circuit Example Including Battery Management Host Controller**

**bq29311**

SLUS487D – DECEMBER 2001 – REVISED NOVEMBER 2003

## FUNCTIONAL DESCRIPTION

### INTEGRATED REGULATOR

The input for this regulator is derived from the battery cell stack or the pack positive terminal, with a valid range of $V_{SD}$ to 25 V. These two source inputs are ORed internally. An external diode is required to protect uncontrolled charging. The output is typically 3.3 V ±5% ($T_A$ = –25°C to 85°C) with a maximum output current of 25 mA. The output capacitance for stable operation is typically 1 µF. The output voltage line regulation is ±20 mV (max) between $V_{SD}$ and 25 V. The load regulation is ±20 mV (max) over the current range of 0. 1 mA to 25 mA.

The regulator output starts up only when VPACK reaches the valid input voltage. After this voltage is reached, the bios of the regulator is supplied through VBAT from the battery, even if VPACK voltage is removed.

### SHUTDOWN AND BROWNOUT

If the voltage at VBAT falls below 7.975 V±5%(default), the bq29311 sets the BRWO bit to 1 in STATUS (b4) and triggers the XALERT output. The value in the SDV register (b4–b7) determines the threshold value and this can be programmed from 7.975 V to 12.475 V in 0.3-V steps (with an accuracy of ±5% at the falling edge) and has 50 mV ±30% of hysteresis.

Reading the STATUS register clears XALERT in a brownout, but OCL (CONTROL, b0) must be taken from 0 to 1 to 0; then STATUS must be read, to clear the BRWO bit.

If the voltage at VBAT is below 6.475V ±5% (default) the regulator can be shut down. The value in the SDV register (b0–3) determines the threshold value, which can be programmed from 6.475 V to 10.975 V in 0.3-V steps with an accuracy of ±5% at the falling edge and has 50 mV ±30% of hysteresis.

When the input voltage is below the shutdown threshold and a higher voltage at VPACK is not present, then SHDN (STATUS, b5) is set and the bq29311 enters the sleep mode and turns off CHG, DSG, and PCHG. The current consumption in this mode is under 1 µA. SHDN is cleared when the input voltage rises above the shutdown threshold. XALERT does not respond to shutdown.

### OVERCURRENT, OVERLOAD,AND SHORT-CIRCUIT DETECTION

The overcurrent, overload, and short-circuit detection is used to detect abnormal current in either the charge or discharge direction. This safety feature is used to protect the pass FETs, cells, and any other inline components from excessive current conditions. The detection circuit also incorporates a blanking delay before driving the control for the pass FETs to turn off.

The overcurrent, overload, and short-circuit thresholds are set in the OCVD/C and SCV registers with defaults of 50 mV and 100 mV respectively. The individual overcurrent (charge) , and overload (discharge) thresholds can be programmed from 50 mV to 205 mV in 5-mV steps with a hysteresis of 10 mV ±30%. The single short-circuit threshold can be programmed from 100 mV to 475 mV in 25-mV steps with a hysteresis of 50 mV ±20%.

### OVERCURRENT, OVERLOAD AND SHORT-CIRCUIT DELAY

The overcurrent and overload delays allow the system to momentarily accept a high current condition. The default overcurrent delay is 1 ms. The delay time can be increased via the OCD register, where the overcurrent and overload delays can be independently defined. The OCD register can be programmed for a range of 1 ms to 31 ms with steps of 2 ms.

The short-circuit delay has a default value of 0 ms and is also programmable in the SCD register. This register can be programmed from 0 to 915 µs with steps of 61 µs.

### OVERCURRENT, OVERLOAD AND SHORT-CIRCUIT RESPONSE

When an overcurrent, overload, or short-circuit condition is detected, the CHG and DSG FETs are turned off and the PCHG FET turned on, limiting the charge current to the pre-charge rate. The STATUS (b0...b3) register reports the details of discharge short circuit, charge short circuit, overload (discharge overcurrent) and overcurrent. The respective STATUS (b0...b3) bits are set to 1 and the XALERT output changes state. This condition is latched until the CONTROL (b0) is set and then reset. If a FET is turned on by resetting CONTROL (b0) and the error condition is still on the system, then the device again enters the protection response state.

### CELL VOLTAGE

The cell voltage is translated to allow a system host to measure individual series elements of the battery.

The series element voltage is translated to a GND-based voltage equal to 0.15 of the series element voltage. This provides a range from 0 V to 4.5 V. The translation output is inversely proportional to the input.

$$V_{(CELL\_OUT)} = -K \times V_{(CELL\_IN)} + 0.975 \ (V)$$

Programming CELL_SEL (b0...b1) selects the individual series element. The CELL_SEL (b2 . . . b3) selects the measurement mode for the series elements. This allows the offset to be determined for each element in the string.

## CALIBRATION OF CELL VOLTAGE MONITOR AMPLIFIER GAIN

The cell voltage monitor amplifier has an offset, which can be calibrated to increase accuracy.

The following procedure shows how to measure and calculate the offset:

1. Set CAL2=0, CAL1=1, VM1=0, VM0=0
   The output voltage includes the offset and is represented by
   $V_{OUT1} = 0.975 + (1 + K) \times V_{OS}$ (V)
   where K = VCELL scaling factor
   $V_{OS}$ = offset voltage at input of the internal op-amp

2. Set CAL2=1, CAL1=0, VM1=0, VM0=0
   The output voltage includes the scale factor error and offset and is represented by
   $V_{OUT2} = 0.975 + (1 + K) \times V_{OS} - K \times 0.975$ (V)

3. Calculate $(V_{OUT1} - V_{OUT2})/0.975$
   The result is the actual scaling factor, $K_{ACT}$ and is represented by
   $K_{ACT} = (V_{OUT1} - V_{OUT2})/0.975 = (0.975 + (1 + K) \times V_{OS}) - (0.975 + (1 + K) \times V_{OS} - K \times 0.975)/0.975$
   $= K \times 0.975/0.975 = K$

4. Calculate the actual offset value where
   $V_{OS(ACT)} = (V_{OUT1} - 0.975)/(1 + K_{ACT})$

5. Calibrated cell voltage is calculated by
   $VC_n - VC_{(n+1)} = [0.975 + (1 + K_{ACT}) \times V_{OS(ACT)} - V_{CELLOUT}]/K_{ACT}$

## CELL BALANCE CONTROL

The cell balance control allows a small discharge to be controlled for any one series element. The purpose of this discharge is to bring the series elements to the same voltage. Series resistors placed between the input pins and the positive series element nodes control the discharge current value.

Individual series element selection is made using CELL_SEL (b4...b7). Cell balance discharge is also disabled if bits CELL_SEL (b4...b7) are zero. When all CELL_SEL (b4…b7) bits are set to 1, then all series elements are discharged.

## DSG AND CHG FET DRIVER CONTROL

The bq29311 drives the FET off if an OC or SC safety threshold is breached. The host can force any FET on or off only if the bq29311 integrated protection control allows. The DSG and CHG FET drive gate-to-drain voltage is clamped to 15 V (max) and 11 V (typ).

The default-state of the FET drive is off. A host can control the FET drive by programming CONTROL (b1...b2) where b1 is used to control the external discharge FET and b2 is used to control the external charge FET. These controls are valid only when shutdown is not active.

## PCHG FET DRIVER CONTROL

The PCHG FET is used when the battery is under voltage, allowing limited conditioning current modes such as pre-charge and 0 V charging. At startup of the bq29311 (charger connected to battery pack), PCHG is clamped to 3.5 V when VPACK is 3.8 V to 5.25 V. Thus the actual VPACK voltage is decided with this PCHG clamp voltage and the VGS(gate-source voltage) of external precharge FET. When VPACK is over 5.25 V, PCHG voltage would be controlled to two-thirds of VPACK.

The default state of PCHG is on. There are two methods to pull up PCHG to turn off precharge FET. One is through the control register via serial communication. Setting b3 in the control register to 1 turns off the precharge FET. Another method is to use CNTL. Floating CNTL or pulling CNTL up to VREG turns off the precharge FET and also the CHG and DSG FETs.

Overcurrent, overload, and short-circuit detection is not applied during precharge operations. An external resistor located in series with the external precharge FET limits the current flow for precharge operations.
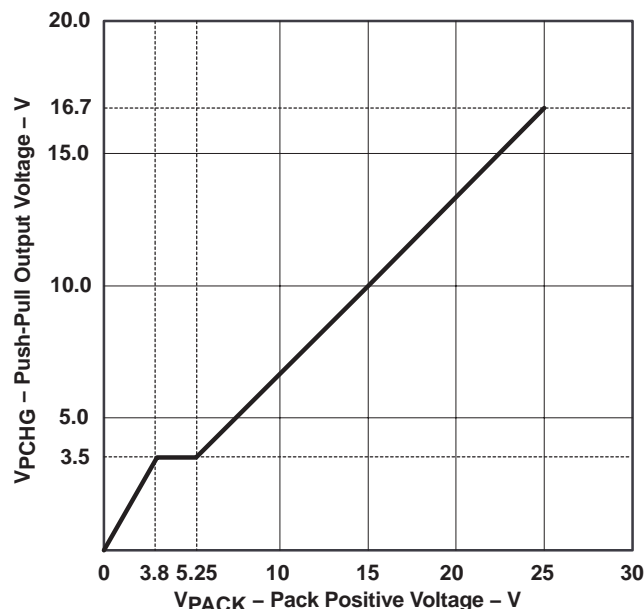


**Figure 3. PCHG Drive Output vs. Pack Voltage (Design Simulation)**

## THERMISTOR DRIVE CIRCUIT

The TOUT pin can be enabled to drive a thermistor from VREG. The typical thermistor resistance is 10 kΩ at 25°C. The default-state for this is OFF to conserve power. The maximum output impedance is 100 Ω. TOUT (b6 of the control register) enables or disables this function. TOUT (b6 of CONTROL register) enables or disables this feature.

## LED DRIVE CIRCUIT

The LED drive provides a current source from VREG. LEDEN (b5 of the control register) enables or disables this function.

## CONTROL INPUT (CNTL)

The control input is pulled up internally to VREG, which disables all the FET outputs. When CNTL is pulled to GND, the bq29311 control outputs are then controlled by safety and register control logic. An external pullup can be added to enable a pullup to a higher voltage. This could cause up to an extra 100 µA leakage through the CNTL input to GND.

## CLOCK INPUT (CLKIN)

The clock input allows for an external time base to be used for increased accuracy in delay timing when determining overcurrent and short-circuit holdoff. The standard frequency is 32.768 kHz but must be above 30 kHz. This input is pulled up via an internal 100-kΩ resistor.

Transitions of the CLKIN pin hold off the internal oscillator so if the external input stops oscillating, the internal oscillator starts and enables all the timing functions.

## COMMUNICATIONS

The I$^2$C compatible serial communications provides read and write access to the bq29311 data area. The data is clocked via separate data (SDATA) and clock (SCLK) pins. The bq29311 acts as a slave device and does not generate clock pulses. Communication to the bq29311 can be provided from GPIO pins or an I$^2$C supporting port of a host system controller. The slave address for the bq29311 is 7 bits and the value is 0100 000 (0x20).

| ADDRESS (0X20) | | | | | | |
|---|---|---|---|---|---|---|
| 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |

The bq29311 does not have the following functions compatible with the I$^2$C specification.

- The bq29311 is always regarded as a slave.

- The bq29311 does not support the general code of the I$^2$C specification and therefore does not return an ACK, but returns a NACK instead.

- The bq29311 does not support the address auto increment, which allows continuous reading and writing.

- The bq29311 allows data to be written or read from the same location without resending the location address.
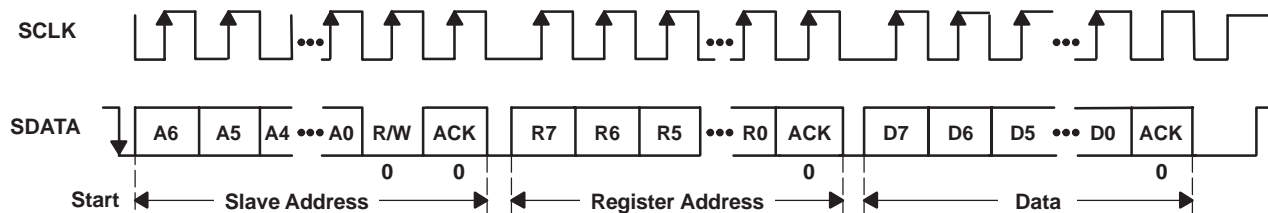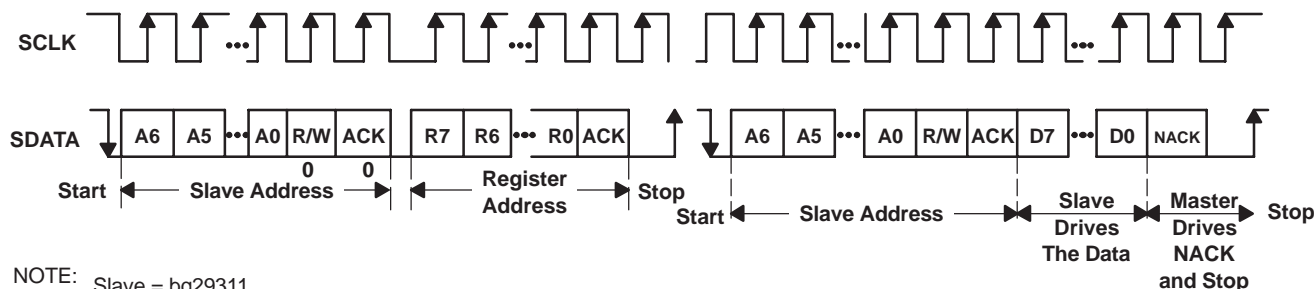


NOTE: Slave = bq29311

**Figure 4. I$^2$C-Bus Write to bq29311**
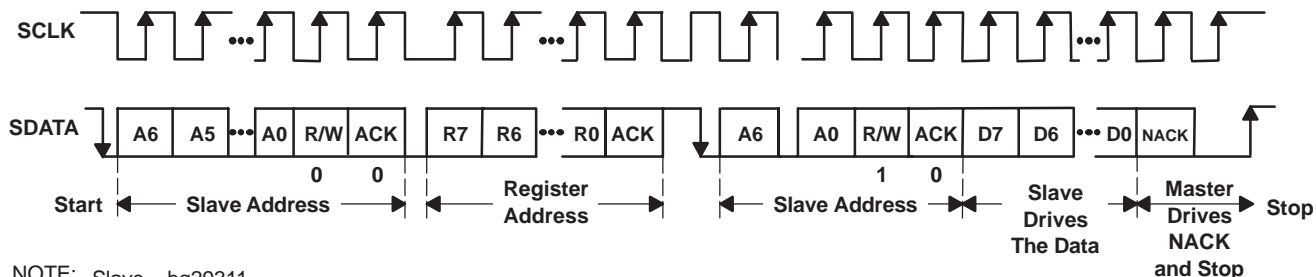


NOTE: Slave = bq29311

**Figure 5. I$^2$C-Bus Read from bq29311: Protocol A**

NOTE: Slave = bq29311

**Figure 6. I²C-Bus Read from bq29311: Protocol B**

## REGISTER MAP

The bq29311 has nine addressable registers. These registers provide status, control, and configuration information for the battery-protection system. All registers except for status are read/write. All registers are reset on power up of the bq29311.

| NAME | ADDRESS | TYPE | DESCRIPTION |
|---|---|---|---|
| STATUS | 0x00 | R | bq29311 status |
| CONTROL | 0x01 | R/W | bq29311 control from system host |
| SDV | 0x02 | R/W | Brownout/shutdown threshold voltage |
| OCVD | 0x03 | R/W | Overcurrent threshold voltage for discharge (overload) |
| OCVC | 0x04 | R/W | Overcurrent threshold voltage for charge |
| OCD | 0x05 | R/W | Overcurrent and overload delay time |
| CELL_SELECT | 0x06 | R/W | Battery cell select for cell translation and balance discharge |
| SCV | 0x07 | R/W | Short-circuit threshold voltage for discharge and charge |
| SCD | 0x08 | R/W | Short-circuit delay time for discharge and charge |

## STATUS register

| STATUS REGISTER (0X00) | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| – | – | SHDN | BRWO | OCCHG | OCDSG | SCCHG | SCDSG |

The status register provides information about the current state of the bq29311. Reading the status register clears the XALERT pin after OCL (CONTROL, b0) has been cleared unless otherwise stated.

STATUS b0 (SCDSG): This bit indicates a short circuit in the discharge direction.

    0 = below the short-circuit threshold in the discharge direction (default)
    1 = greater than or equal to the short-circuit threshold in the discharge direction

STATUS b1 (SCCHG): This bit indicates a short-circuit in the charge direction.

    0 = below the short-circuit threshold in the charge direction (default)
    1 = greater than or equal to the short-circuit threshold in the charge direction

STATUS b2 (OCDSG): This bit indicates an overload condition.

    0 = less than or equal to the overcurrent threshold in the discharge direction (default)
    1 = greater than overcurrent threshold in the discharge direction

STATUS b3 (OCCHG): This bit indicates an overcurrent condition.

    0 = less than or equal to the overcurrent threshold in the charge direction (default)
    1 = greater than overcurrent threshold in the charge direction

STATUS b4 (BRWO): This bit indicates that the brownout voltage threshold has been reached.

    0 = greater than the brownout threshold (default)
    1 = less than or equal to the brownout threshold voltage

STATUS b5 (SHDN): This bit shows that the battery voltage has fallen below the shutdown threshold limit, indicating a shutdown condition.

    0 = greater than the shutdown threshold voltage (default)
    1 = less than or equal to the shutdown threshold voltage

**bq29311**

SLUS487D – DECEMBER 2001 – REVISED NOVEMBER 2003

## CONTROL REGISTER

| CONTROL REGISTER (0X01) | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SVDOFF | TOUT | LEDEN | VMOFF | PCHG | CHG | DSG | OCL |

The CONTROL register controls the outputs of the bq29311 and can be used to clear certain states set by any OC, SC or brownout condition. The OCL latch must be cleared before the STATUS register is read to clear the register.

CONTROL b0 (OCL): This bit releases the overcurrent latch when toggled from 0 to 1 back to 0 (default = 0) after the latch has been set by any OC or SC condition.

CONTROL b1 (DSG): This bit controls the external discharge FET.

0 = discharge FET is off and is controlled by the system host (default)
1 = discharge FET is on and the bq29311 is in normal operating mode

CONTROL b2 (CHG): This bit controls the external charge FET.

0 = charge FET is off and is controlled by the system host (default)
1 = charge FET is on and the bq29311 is in normal operating mode.

CONTROL b3 (PCHG): This bit controls the external precharge FET.

0 = precharge FET is on and controlled by the system host for enabling a charge path prior to turning on the charge FET (default)
1 = precharge FET is off.

CONTROL b4 (VMOFF): This bit enables or disables the voltage monitoring translation function and cell balance discharge.

0 = enables voltage monitoring (default)
1 = disables voltage monitoring

CONTROL b5 (LEDEN): This bit enables or disables the LED driver function

0 = disables LED drive function (default)
1 = enables LED drive function

CONTROL b6 (TOUT): This bit controls the $V_{CC}$ power to the thermistor.

0 = thermistor power is off (default)
1 = thermistor power is on

CONTROL b7 (SDVOFF): This bit enables or disables the shutdown monitor function.

0 = shutdown monitor enabled (default)
1 = shutdown monitor disabled

## SDV: SHUTDOWN VOLTAGE

| SDV REGISTER (0X02) | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BOV3 | BOV2 | BOV1 | BOV0 | SDV3 | SDV2 | SVD1 | SDV0 |

The SDV register is used to configure the regulator shutdown and brownout thresholds. 00000000 is the default.

### SDV b3...b0 With Corresponding Threshold

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0000 | 6.475 V | 0100 | 7.675 V | 1000 | 8.875 V | 1100 | 10.075 V |
| 0001 | 6.775 V | 0101 | 7.975 V | 1001 | 9.175 V | 1101 | 10.375 V |
| 0010 | 7.075 V | 0110 | 8.275 V | 1010 | 9.475 V | 1110 | 10.675 V |
| 0011 | 7.375 V | 0111 | 8.575 V | 1011 | 9.775 V | 1111 | 10.975 V |

### SDV b7...b4 With Corresponding Threshold

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0000 | 7.975 V | 0100 | 9.175 V | 1000 | 10.375 V | 1100 | 11.575 V |
| 0001 | 8.275 V | 0101 | 9.475 V | 1001 | 10.675 V | 1101 | 11.875 V |
| 0010 | 8.575 V | 0110 | 9.775 V | 1010 | 10.975 V | 1110 | 12.175 V |
| 0011 | 8.875 V | 0111 | 10.075 V | 1011 | 11.275 V | 1111 | 12.475 V |

## OCVD: OVERCURRENT (OVERLOAD) VOLTAGE THRESHOLD IN DISCHARGE

| OCVD REGISTER (0X03) | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| – | – | – | OCVD4 | OCVD3 | OCVD2 | OCVD1 | OCVD0 |

OCVD b0–b4 (OCVD0–OCVD4): These five bits select the value of the overcurrent threshold in the discharge direction. 00000 is the default.

### OCVD b4...b0 With Corresponding Threshold

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 00000 | 0.050 V | 01000 | 0.090 V | 10000 | 0.130 V | 11000 | 0.170 V |
| 00001 | 0.055 V | 01001 | 0.095 V | 10001 | 0.135 V | 11001 | 0.175 V |
| 00010 | 0.060 V | 01010 | 0.100 V | 10010 | 0.140 V | 11010 | 0.180 V |
| 00011 | 0.065 V | 01011 | 0.105 V | 10011 | 0.145 V | 11011 | 0.185 V |
| 00100 | 0.070 V | 01100 | 0.110 V | 10100 | 0.150 V | 11100 | 0.190 V |
| 00101 | 0.075 V | 01101 | 0.115 V | 10101 | 0.155 V | 11101 | 0.195 V |
| 00110 | 0.080 V | 01110 | 0.120 V | 10110 | 0.160 V | 11110 | 0.200 V |
| 00111 | 0.085 V | 01111 | 0.125 V | 10111 | 0.165 V | 11111 | 0.205 V |

## OCVC: OVERCURRENT VOLTAGE THRESHOLD REGISTER

| OCVC REGISTER (0X04) | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| – | – | – | OCVC4 | OCVC3 | OCVC2 | OCVC1 | OCVC0 |

OCVC b0–b4 (OCVC0–OCVC4): These five bits select the value of the overcurrent threshold in the charge direction. 00000 is the default.

### OCVC b4...b0 With Corresponding Threshold

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 00000 | 0.050 V | 01000 | 0.090 V | 10000 | 0.130 V | 11000 | 0.170 V |
| 00001 | 0.055 V | 01001 | 0.095 V | 10001 | 0.135 V | 11001 | 0.175 V |
| 00010 | 0.060 V | 01010 | 0.100 V | 10010 | 0.140 V | 11010 | 0.180 V |
| 00011 | 0.065 V | 01011 | 0.105 V | 10011 | 0.145 V | 11011 | 0.185 V |
| 00100 | 0.070 V | 01100 | 0.110 V | 10100 | 0.150 V | 11100 | 0.190 V |
| 00101 | 0.075 V | 01101 | 0.115 V | 10101 | 0.155 V | 11101 | 0.195 V |
| 00110 | 0.080 V | 01110 | 0.120 V | 10110 | 0.160 V | 11110 | 0.200 V |
| 00111 | 0.085 V | 01111 | 0.125 V | 10111 | 0.165 V | 11111 | 0.205 V |

**bq29311**

SLUS487D – DECEMBER 2001 – REVISED NOVEMBER 2003

## OCD: OVERCURRENT/OVERLOAD BLANKING DELAY

| OCD REGISTER (0X05) | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OCDC3 | OCDC2 | OCDC1 | OCDC0 | OCDD3 | OCDD2 | OCDD1 | OCDD0 |

This register is used to set the overcurrent and overload delay times.

OCD b0–b3 (OCDD0–OCDD3): These four bits select the value of the delay time for overcurrent triggering in the discharge direction. 0000 is the default.

### OCD b3...b0 With Corresponding Delay Time

| 0000 | 1 ms | 0100 | 9 ms | 1000 | 17 ms | 1100 | 25 ms |
|---|---|---|---|---|---|---|---|
| 0001 | 3 ms | 0101 | 11 ms | 1001 | 19 ms | 1101 | 27 ms |
| 0010 | 5 ms | 0110 | 13 ms | 1010 | 21 ms | 1110 | 29 ms |
| 0011 | 7 ms | 0111 | 15 ms | 1011 | 23 ms | 1111 | 31 ms |

OCD b4–b7 (OCDC0–OCDC3): These four bits select the value of the delay time for overcurrent triggering in the charge direction. 0000 is the default.

### OCD b7...b4 With Corresponding Delay Time

| 0000 | 1 ms | 0100 | 9 ms | 1000 | 17 ms | 1100 | 25 ms |
|---|---|---|---|---|---|---|---|
| 0001 | 3 ms | 0101 | 11 ms | 1001 | 19 ms | 1101 | 27 ms |
| 0010 | 5 ms | 0110 | 13 ms | 1010 | 21 ms | 1110 | 29 ms |
| 0011 | 7 ms | 0111 | 15 ms | 1011 | 23 ms | 1111 | 31 ms |

## SCV: SHORT-CIRCUIT THRESHOLD VOLTAGE

| SCV REGISTER (0X07) | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| – | – | – | – | SCV3 | SCV2 | SCV1 | SCV0 |

This register selects the common short-circuit threshold voltage for both charge and discharge.

SCV b0–b3 (SCV0–SCV3): These four bits select the value of the short-circuit voltage threshold for both charge and discharge. 0000 is the default.

### SCV b0...b3 With Corresponding Threshold Voltage

| 0000 | 0.10V | 0100 | 0.20V | 1000 | 0.30V | 1100 | 0.40V |
|---|---|---|---|---|---|---|---|
| 0001 | 0.125V | 0101 | 0.225V | 1001 | 0.325V | 1101 | 0.425V |
| 0010 | 0.150V | 0110 | 0.250V | 1010 | 0.350V | 1110 | 0.450V |
| 0011 | 0.175V | 0111 | 0.275V | 1011 | 0.375V | 1111 | 0.475V |

## SCD: SHORT-CIRCUIT BLANKING DELAY

| SCD REGISTER (0X08) | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SCDC3 | SCDC2 | SCDC1 | SCDC0 | SCDD3 | SCDD2 | SCDD1 | SCDD0 |

This register selects the short-circuit blanking delay time for charge and discharge.

SCD b0–b3 (SCDD0–SCDD3): These four bits select the value of the short-circuit delay time for discharge. Exceeding the short-circuit voltage threshold for longer than this period turns off the DSG output. 0000 is the default.

### SCD b3...b0 With Corresponding Delay Time

| 0000 | 0 µs | 0100 | 244 µs | 1000 | 488 µs | 1100 | 732 µs |
|---|---|---|---|---|---|---|---|
| 0001 | 61 µs | 0101 | 305 µs | 1001 | 549 µs | 1101 | 793 µs |
| 0010 | 122 µs | 0110 | 366 µs | 1010 | 610 µs | 1110 | 854 µs |
| 0011 | 183 µs | 0111 | 427 µs | 1011 | 671 µs | 1111 | 915 µs |

SCD b4–b7 (SCDC0–SCDC3): These four bits select the value of the short-circuit delay time for charge. Exceeding the short-circuit voltage threshold for longer than this period turns off the CHG output.

## SCD b7...b4 With Corresponding Delay Time

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0000 | 0 µs | 0100 | 244 µs | 1000 | 488 µs | 1100 | 732 µs |
| 0001 | 61 µs | 0101 | 305 µs | 1001 | 549 µs | 1101 | 793 µs |
| 0010 | 122 µs | 0110 | 366 µs | 1010 | 610 µs | 1110 | 854 µs |
| 0011 | 183 µs | 0111 | 427 µs | 1011 | 671 µs | 1111 | 915 µs |

## CELL_SELECT: CELL SELECTION

| CELL_SELECT REGISTER (0X06) | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CELL4 | CELL3 | CELL2 | CELL1 | CAL1 | CAL0 | VM1 | VM0 |

This register determines cell selection for voltage measurement and translation, cell balancing and the operational mode of the cell voltage monitoring.

### CELL_SELECT b0–b1 (VM0–VM1)

These two bits select the series cell for voltage measurement translation.

| VM1 | VM0 | SELECTED CELL |
|---|---|---|
| 0 | 0 | Bottom series element (default) |
| 0 | 1 | Second lowest series element |
| 1 | 0 | Second highest series element |
| 1 | 1 | Top series element |

CELL_SELECT b2–b3 (CAL0, CAL1): These bits determine the mode of the voltage monitor block.

| CAL1 | CAL0 | MEASUREMENT MODE |
|---|---|---|
| 0 | 0 | Cell translation for selected cell (default) |
| 0 | 1 | Offset measurement for selected cell |
| 1 | x | Monitor the $V_{REF}$ value for gain calibration |

CELL_SELECT b3–b6 (CELL1–CELL4): These four bits select the series cell for cell balance discharge. Cell balance discharge is disabled if bits b4...b7 are set to zero (default), and all cells are discharged if bits b4...b7 are set to 1.

CELL1 =1 = bottom series element
CELL2 =1 = second lowest series element
CELL3 =1 = second highest series element
CELL4 =1 = top series element

Figure 2 shows a typical application for the bq29311 smart lithium-ion battery protector. All functions required to protect three- or four-series lithium-ion cells from overcharge and over-discharge, as well as provide short-circuit protection, are included in a single chip.

An R-C filter is recommended at the VCELL pin where $R_{(VCELL)} = 100\ \Omega$ (typ) and $C_{(VCELL)} = 100$ nF (typ)

## CELL CONNECTION ORDER

The cells should be connected in the following order: Bat– to VC5, Bat+ to VC1, top of bottom cell to VC4, top of second cell to VC3 and top of third cell to VC2.

## 3 OR 4 CELL CONFIGURATION

The 4-series cell configuration is shown in Figure 1. In a 3-cell configuration, VC1 is shorted to VC2, and R3 and C13 are removed. VC2, VC3, VC4, and VC5 pins are used for three cells.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ29311PW | NRND | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -25 to 85 | 29311PW | |
| BQ29311PWG4 | NRND | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -25 to 85 | 29311PW | |
| BQ29311PWR | NRND | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -25 to 85 | 29311PW | |
| BQ29311PWRG4 | NRND | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -25 to 85 | 29311PW | |

**(1)** The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ29311PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

**TAPE AND REEL BOX  DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|-----|-------------|------------|-------------|
| BQ29311PWR | TSSOP | PW | 24 | 2000 | 367.0 | 367.0 | 38.0 |

PW (R−PDSO−G24)                                    PLASTIC SMALL OUTLINE

0,65    0,30
        0,19        ⊕ | 0,10 Ⓜ

24                13

△D  4,50   6,60
    4,30   6,20

1                 12

7,90
7,70

△C

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX          0,15
                  0,05

Seating Plane

△ | 0,10

4040064−6/G  02/11

NOTES:   A.  All linear dimensions are in millimeters.  Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.  This drawing is subject to change without notice.
        △C  Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
             not exceed 0,15 each side.
        △D  Body width does not include interlead flash.  Interlead flash shall not exceed 0,25 each side.
         E.  Falls within JEDEC MO−153

PW (R−PDSO−G24)  PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

22x0,65

5,6

24x0,25

5,6

1,55

22x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note E)

0,3

1,6

Pad Geometry

0,07
All Around

4211284−4/G  08/15

NOTES:  A.  All linear dimensions are in millimeters.
B.  This drawing is subject to change without notice.
C.  Publication IPC−7351 is recommended for alternate design.
D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS
INSTRUMENTS
www.ti.com

# IMPORTANT NOTICE

| Products | | Applications | |
|---|---|---|---|
| Audio | www.ti.com/audio | Automotive and Transportation | www.ti.com/automotive |
| Amplifiers | amplifier.ti.com | Communications and Telecom | www.ti.com/communications |
| Data Converters | dataconverter.ti.com | Computers and Peripherals | www.ti.com/computers |
| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Security | www.ti.com/security |
| Power Mgmt | power.ti.com | Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Microcontrollers | microcontroller.ti.com | Video and Imaging | www.ti.com/video |
| RFID | www.ti-rfid.com | | |
| OMAP Applications Processors | www.ti.com/omap | **TI E2E Community** | e2e.ti.com |
| Wireless Connectivity | www.ti.com/wirelessconnectivity | | |