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NTE4012B & NTE4012BT **Integrated Circuit** **CMOS, Quad 4-Input NAND Gate**

Description:

The NTE4012B (14-Lead DIP) and NTE4012BT (SOIC-14) are quad 4-input NAND gate devices constructed with P-Channel and N-Channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

Features:

- Supply Voltage Range: 3Vdc to 18Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs

Absolute Maximum Ratings: (Voltages referenced to V_{SS} , Note 1)

DC Supply Voltage, V_{DD}	-0.5 to +18.0V
Input Voltage (DC or Transient), V_{in}	-0.5 to V_{DD} to +0.5V
Output Voltage (DC or Transient), V_{out}	-0.5 to V_{DD} to +0.5V
Input Current (DC or Transient, Per Pin), I_{in}	± 10 mA
Output Current (DC or Transient, Per Pin), I_{out}	± 10 mA
Power Dissipation (Per Package), P_D	500mW
Temperature Derating (from +65° to +125°C)	-7.0mW/°C
Storage Temperature, T_{stg}	-65° to +150°C
Lead Temperature (During Soldering, 8sec max), T_L	+260°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

Electrical Characteristics: (Voltages referenced to V_{SS} , Note 2)

Parameter	Symbol	V_{DD} Vdc	-55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage “0” Level $V_{in} = V_{DD}$ or 0 “1” Level $V_{in} = 0$ or V_{DD}	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage “0” Level ($V_O = 4.5$ or $0.5V_{dc}$) ($V_O = 9.0$ or $1.0V_{dc}$) ($V_O = 13.5$ or $1.5V_{dc}$) “1” Level ($V_O = 0.5$ or $4.5V_{dc}$) ($V_O = 1.0$ or $9.0V_{dc}$) ($V_O = 1.5$ or $13.5V_{dc}$)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source ($V_{OH} = 2.5V_{dc}$) ($V_{OH} = 4.6V_{dc}$) ($V_{OH} = 9.5V_{dc}$) ($V_{OH} = 13.5V_{dc}$) Sink ($V_{OL} = 0.4V_{dc}$) ($V_{OL} = 0.5V_{dc}$) ($V_{OL} = 1.5V_{dc}$)	I_{OH}	5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	mAdc
		10	–1.6	–	–1.3	–2.25	–	–0.9	–	mAdc
		15	–4.2	–	–3.4	–8.8	–	–2.4	–	mAdc
	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	± 0.1	–	± 0.00001	± 0.1	–	± 0.1	μ Adc
Input Capacitance ($V_{IN} = 0$)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μ Adc
		10	–	0.5	–	0.0010	0.5	–	15	μ Adc
		15	–	1.0	–	0.0015	1.0	–	30	μ Adc
Total Supply Current (Dynamic plus Quiescent, Per Gate, $C_L = 50pF$, Note 3, Note 4)	I_T	5.0	$I_T = (0.3\mu A/kHz) f + I_{DD}/N$							μ Adc
		10	$I_T = (0.6\mu A/kHz) f + I_{DD}/N$							μ Adc
		15	$I_T = (0.8\mu A/kHz) f + I_{DD}/N$							μ Adc

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50) V_{fk}$$

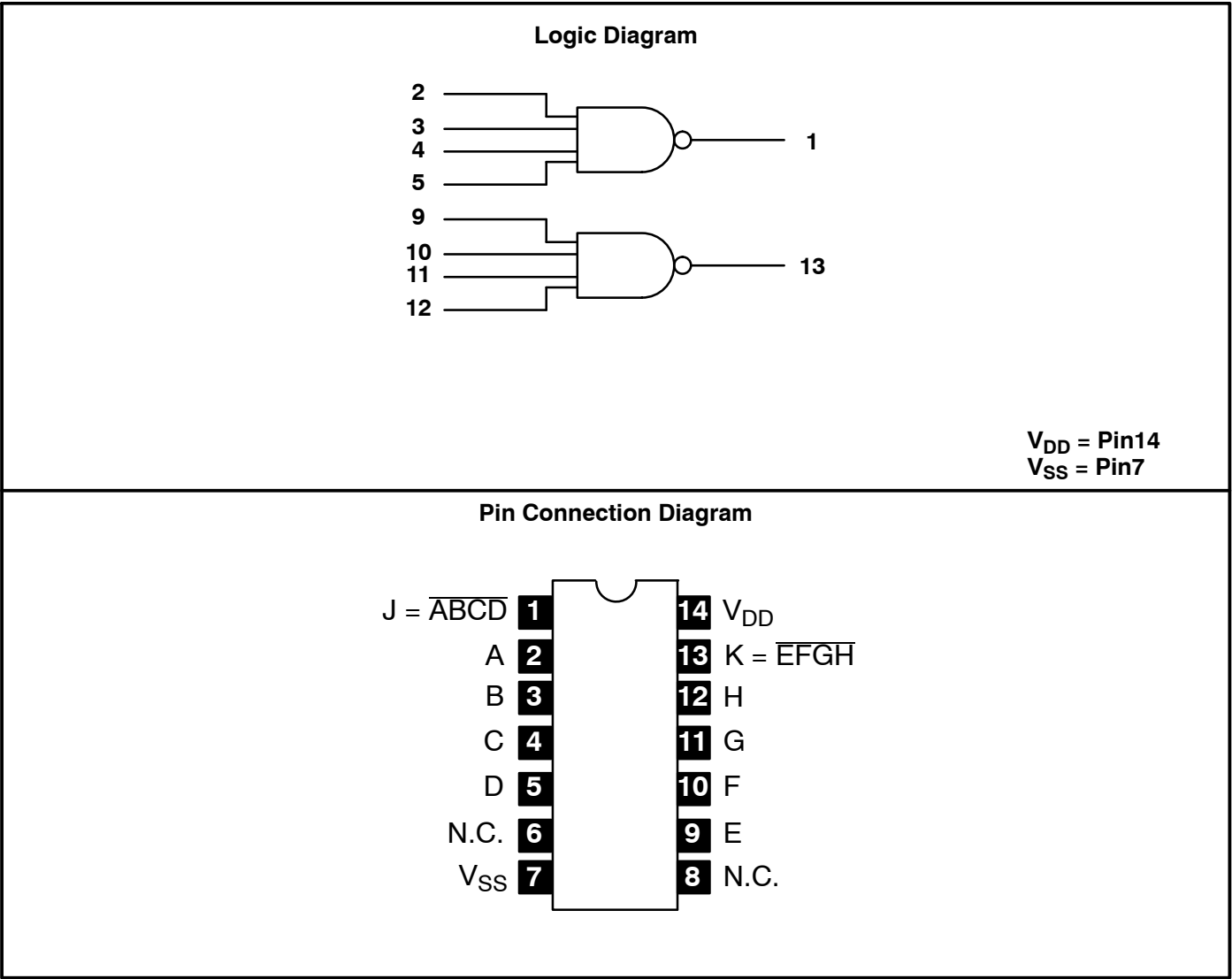
where: I_T is in μH (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.001 \times$ the number of exercised gates per package.

Switching Characteristics: ($C_L = 50\text{pF}$, $T_A = +25^\circ\text{C}$, Note 2)

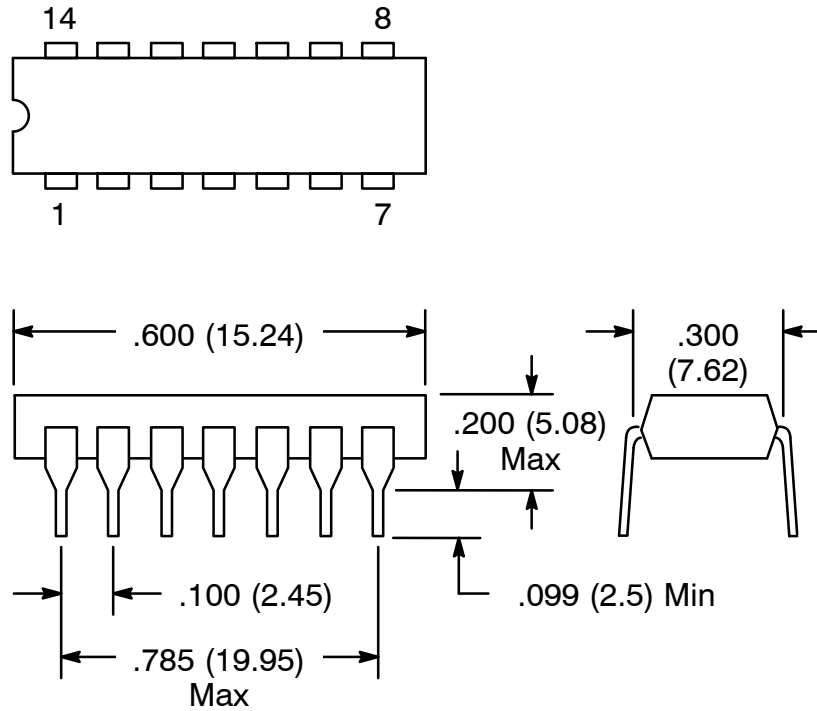
Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time $t_{TLH} = (1.35\text{ns/pf}) C_L + 33\text{ns}$ $t_{TLH} = (0.60\text{ns/pf}) C_L + 20\text{ns}$ $t_{TLH} = (0.40\text{ns/pf}) C_L + 20\text{ns}$	t_{TLH}	5.0	–	100	200	ns
		10	–	50	100	ns
		15	–	40	80	ns
Output Fall Time $t_{THL} = (1.35\text{ns/pf}) C_L + 33\text{ns}$ $t_{THL} = (0.60\text{ns/pf}) C_L + 20\text{ns}$ $t_{THL} = (0.40\text{ns/pf}) C_L + 20\text{ns}$	t_{THL}	5.0	–	100	200	ns
		10	–	50	100	ns
		15	–	40	80	ns
Propagation Delay Time $t_{PLH}, t_{PHL} = (0.90\text{ns/pf}) C_L + 115\text{ns}$ $t_{PLH}, t_{PHL} = (0.36\text{ns/pf}) C_L + 47\text{ns}$ $t_{PLH}, t_{PHL} = (0.26\text{ns/pf}) C_L + 37\text{ns}$	t_{PLH}, t_{PHL}	5.0	–	160	300	ns
		10	–	65	130	ns
		15	–	50	100	ns

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

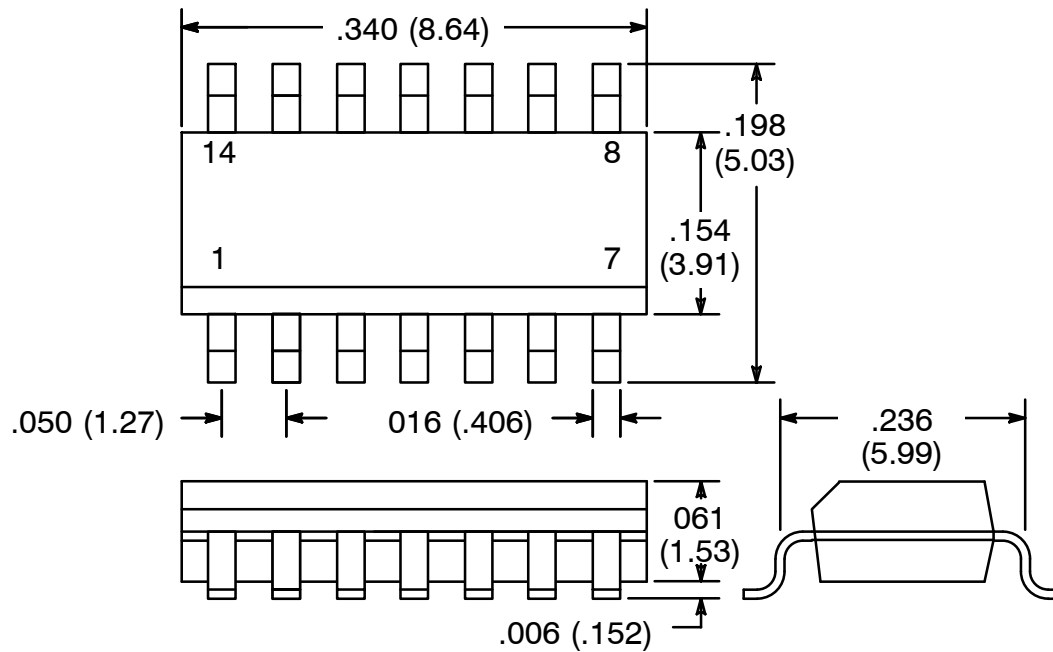
Note 3. The formulas given are for the typical characteristics only at +25°C.



NTE4012B



NTE4012BT



NOTE: Pin1 on Beveled Edge