

单路差分比较器

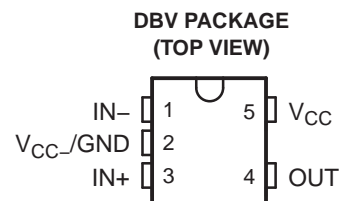
查询样品: [TL331-EP](#)

特性

- 单电源或双电源
- 宽电源电压范围: **2V 至 36V**
- 独立于电源电压的低电源电流漏极: **0.4mA** (典型值)
- 低输入偏置电流: **25nA** (典型值)
- 低输入偏移电压: **2mV** (典型值)
- 共模输入电压范围包括接地
- 差分输入电压范围等于最大额定电源电压: **±36V**
- 低输出饱和电压
- 输出与 **TTL, MOS 和 CMOS** 兼容

支持国防、航空航天、和医疗应用

- 受控基线
- 一个组装和测试场所
- 一个制造场所
- 支持军用 (**-55°C 至 125°C**) 温度范围
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性



说明/订购信息

这个器件包含一个单电压比较器，此比较器被设计成在宽范围电压上由一个单电源供电运行。如果两个电源之间的电压差在 **2V** 和 **36V** 之间且 V_{CC} 比输入共模电压的正值至少高 **1.5V**，也可使用双电源供电运行。电流漏极与电源电压无关。为了实现线与关系，用户可将输出连接至另外一个集电极开路输出。

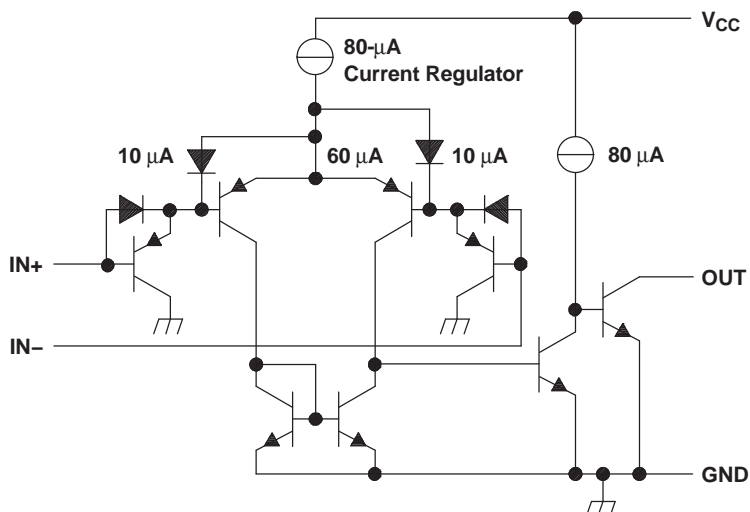
ORDERING INFORMATION⁽¹⁾

T_A	$V_{IO(MAX)}$ at 25°C	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
-55°C to 125°C	5 mV	SOT-23 (DBV)	Reel of 3000	TL331MDBVREP	TEPU	V62/13611-01XE
			Reel of 250	TL331MDBVTEP		

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



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LOGIC DIAGRAM**SCHEMATIC**

COMPONENT COUNT	
Epi-FET	1
Diodes	2
Resistors	1
Transistors	20

Note: Current values shown are nominal.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage ⁽²⁾	36 V
V_{ID}	Differential input voltage ⁽³⁾	± 36 V
V_I	Input voltage range (either input)	-0.3 V to 36 V
V_O	Output voltage	36 V
I_O	Output current	20 mA
	Duration of output short-circuit to ground ⁽⁴⁾	Unlimited
T_J	Operating virtual junction temperature	150°C
T_{stg}	Storage temperature range	-65°C to 150°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the network ground.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		TL331-EP	UNITS
		DBV	
		5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	299	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance ⁽³⁾	65.4	
θ_{JB}	Junction-to-board thermal resistance ⁽⁴⁾	97.1	
ψ_{JT}	Junction-to-top characterization parameter ⁽⁵⁾	0.8	
ψ_{JB}	Junction-to-board characterization parameter ⁽⁶⁾	95.5	
θ_{JCbott}	Junction-to-case (bottom) thermal resistance ⁽⁷⁾	N/A	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

at specified free-air temperature, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS ⁽¹⁾	T_A	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	$V_{CC} = 5\text{ V}$ to 30 V , $V_O = 1.4\text{ V}$, $V_{IC} = V_{IC(min)}$	25°C		2	5	mV
		–55°C to 125°C			9	
I_{IO} Input offset current	$V_O = 1.4\text{ V}$	25°C		5	50	nA
		–55°C to 125°C			250	
I_{IB} Input bias current	$V_O = 1.4\text{ V}$	25°C		–25	–250	nA
		–55°C to 125°C			–400	
V_{ICR} Common-mode input voltage range ⁽²⁾		25°C		0 to $V_{CC} - 1.5$		V
		–55°C to 125°C		0 to $V_{CC} - 2$		
A_{VD} Large-signal differential-voltage amplification	$V_{CC} = 15\text{ V}$, $V_O = 1.4\text{ V}$ to 11.4 V , $R_L \geq 15\text{ k}\Omega$ to V_{CC}	25°C		50	200	V/mV
I_{OH} High-level output current	$V_{OH} = 5\text{ V}$, $V_{ID} = 1\text{ V}$	25°C		0.1	50	nA
	$V_{OH} = 30\text{ V}$, $V_{ID} = 1\text{ V}$	–55°C to 125°C			1	μA
V_{OL} Low-level output voltage	$I_{OL} = 4\text{ mA}$, $V_{ID} = -1\text{ V}$	25°C		150	400	mV
		–55°C to 125°C			700	
I_{OL} Low-level output current	$V_{OL} = 1.5\text{ V}$, $V_{ID} = -1\text{ V}$	25°C		6		mA
I_{CC} Supply current	$R_L = \infty$, $V_{CC} = 5\text{ V}$	25°C		0.4	0.7	mA

- (1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (2) The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC+} - 1.5\text{ V}$, but either or both inputs can go to 30 V without damage.

SWITCHING CHARACTERISTICS $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	R_L connected to 5 V through 5.1 k Ω , $C_L = 15\text{ pF}$ ⁽¹⁾ ⁽²⁾	100-mV input step with 5-mV overdrive	1.3	μs
		TTL-level input step	0.3	

(1) C_L includes probe and jig capacitance.

(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL331MDBVREP	PREVIEW	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	TEPU	
TL331MDBVTEP	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	TEPU	Samples
V62/13611-01XE	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	TEPU	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TL331-EP :

- Catalog: [TL331](#)
- Automotive: [TL331-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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