



CYPRESS

PRELIMINARY

CY7C1512

## 64K x 8 Static RAM

## Features

- High speed
  - $t_{AA} = 15 \text{ ns}$
- CMOS for optimum speed/power
- Low active power
  - 770 mW
- Low standby power
  - 28 mW
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  options

## Functional Description

The CY7C1512 is a high-performance CMOS static RAM organized as 65,536 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{CE}_1$ ), an active HIGH chip enable ( $CE_2$ ), an active LOW output enable ( $\overline{OE}$ ),

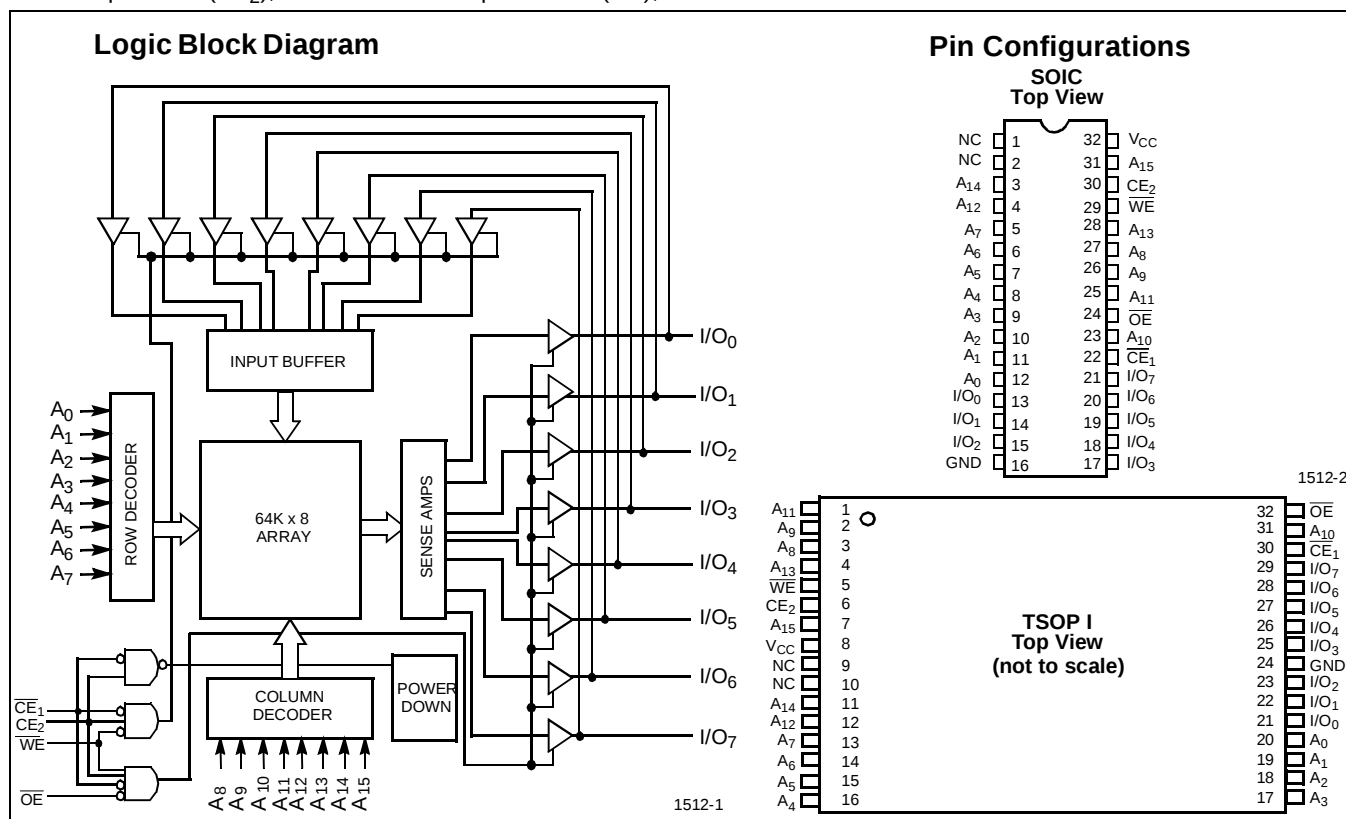
and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

Writing to the device is accomplished by taking chip enable one ( $\overline{CE}_1$ ) and write enable ( $WE$ ) inputs LOW and chip enable two ( $CE_2$ ) input HIGH. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{15}$ ).

Reading from the device is accomplished by taking chip enable one ( $\overline{CE}_1$ ) and output enable ( $\overline{OE}$ ) LOW while forcing write enable ( $WE$ ) and chip enable two ( $CE_2$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $WE$  LOW).

The CY7C1512 is available in standard TSOP type I and 450-mil-wide plastic SOIC packages.



## Selection Guide

|                                   |            | 7C1512-15 | 7C1512-20 | 7C1512-25 | 7C1512-35 | 7C1512-70 |
|-----------------------------------|------------|-----------|-----------|-----------|-----------|-----------|
| Maximum Access Time (ns)          |            | 15        | 20        | 25        | 35        | 70        |
| Maximum Operating Current (mA)    | Commercial | 140       | 130       | 120       | 110       | 110       |
| Maximum CMOS Standby Current (mA) | Commercial | 5         | 5         | 5         | 5         | 5         |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND<sup>[1]</sup> .... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[1]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

## Operating Range

| Range      | Ambient Temperature <sup>[2]</sup> | $V_{CC}$ |
|------------|------------------------------------|----------|
| Commercial | 0°C to +70°C                       | 5V ± 10% |
| Industrial | -40°C to +85°C                     | 5V ± 10% |

## Electrical Characteristics Over the Operating Range<sup>[3]</sup>

| Parameter | Description                                   | Test Conditions                                                                                                                   | 7C1512-15 |                | 7C1512-20 |                | 7C1512-25 |                | Unit |
|-----------|-----------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|-----------|----------------|-----------|----------------|-----------|----------------|------|
|           |                                               |                                                                                                                                   | Min.      | Max.           | Min.      | Max.           | Min.      | Max.           |      |
| $V_{OH}$  | Output HIGH Voltage                           | $V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$                                                                                  | 2.4       |                | 2.4       |                | 2.4       |                | V    |
| $V_{OL}$  | Output LOW Voltage                            | $V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$                                                                                   |           | 0.4            |           | 0.4            |           | 0.4            | V    |
| $V_{IH}$  | Input HIGH Voltage                            |                                                                                                                                   | 2.2       | $V_{CC} + 0.3$ | 2.2       | $V_{CC} + 0.3$ | 2.2       | $V_{CC} + 0.3$ | V    |
| $V_{IL}$  | Input LOW Voltage <sup>[1]</sup>              |                                                                                                                                   | -0.3      | 0.8            | -0.3      | 0.8            | -0.3      | 0.8            | V    |
| $I_{IX}$  | Input Load Current                            | $GND \leq V_I \leq V_{CC}$                                                                                                        | -1        | +1             | -1        | +1             | -1        | +1             | μA   |
| $I_{OZ}$  | Output Leakage Current                        | $GND \leq V_I \leq V_{CC}$ , Output Disabled                                                                                      | -5        | +5             | -5        | +5             | -5        | +5             | μA   |
| $I_{OS}$  | Output Short Circuit Current <sup>[4]</sup>   | $V_{CC} = \text{Max.}, V_{OUT} = GND$                                                                                             |           | -300           |           | -300           |           | -300           | mA   |
| $I_{CC}$  | $V_{CC}$ Operating Supply Current             | $V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$                                                            |           | 140            |           | 130            |           | 120            | mA   |
| $I_{SB1}$ | Automatic CE Power-Down Current — TTL Inputs  | Max. $V_{CC}, \overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}, V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$         |           | 40             |           | 30             |           | 30             | mA   |
| $I_{SB2}$ | Automatic CE Power-Down Current — CMOS Inputs | Max. $V_{CC}, \overline{CE}_1 \geq V_{CC} - 0.3V$ , or $CE_2 \leq 0.3V, V_{IN} \geq V_{CC} - 0.3V$ , or $V_{IN} \leq 0.3V, f = 0$ |           | 5              |           | 5              |           | 5              | mA   |

| Parameter | Description                                   | Test Conditions                                                                                                                   | 7C1512-35 |                | 7C1512-70 |                | Unit |
|-----------|-----------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|-----------|----------------|-----------|----------------|------|
|           |                                               |                                                                                                                                   | Min.      | Max.           | Min.      | Max.           |      |
| $V_{OH}$  | Output HIGH Voltage                           | $V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$                                                                                  | 2.4       |                | 2.4       |                | V    |
| $V_{OL}$  | Output LOW Voltage                            | $V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$                                                                                   |           | 0.4            |           | 0.4            | V    |
| $V_{IH}$  | Input HIGH Voltage                            |                                                                                                                                   | 2.2       | $V_{CC} + 0.3$ | 2.2       | $V_{CC} + 0.3$ | V    |
| $V_{IL}$  | Input LOW Voltage <sup>[1]</sup>              |                                                                                                                                   | -0.3      | 0.8            | -0.3      | 0.8            | V    |
| $I_{IX}$  | Input Load Current                            | $GND \leq V_I \leq V_{CC}$                                                                                                        | -1        | +1             | -1        | +1             | μA   |
| $I_{OZ}$  | Output Leakage Current                        | $GND \leq V_I \leq V_{CC}$ , Output Disabled                                                                                      | -5        | +5             | -5        | +5             | μA   |
| $I_{OS}$  | Output Short Circuit Current <sup>[4]</sup>   | $V_{CC} = \text{Max.}, V_{OUT} = GND$                                                                                             |           | -300           |           | -300           | mA   |
| $I_{CC}$  | $V_{CC}$ Operating Supply Current             | $V_{CC} = \text{Max.}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$                                                            |           | 110            |           | 110            | mA   |
| $I_{SB1}$ | Automatic CE Power-Down Current — TTL Inputs  | Max. $V_{CC}, \overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}, V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}, f = f_{MAX}$         |           | 25             |           | 25             | mA   |
| $I_{SB2}$ | Automatic CE Power-Down Current — CMOS Inputs | Max. $V_{CC}, \overline{CE}_1 \geq V_{CC} - 0.3V$ , or $CE_2 \leq 0.3V, V_{IN} \geq V_{CC} - 0.3V$ , or $V_{IN} \leq 0.3V, f = 0$ |           | 5              |           | 5              | mA   |

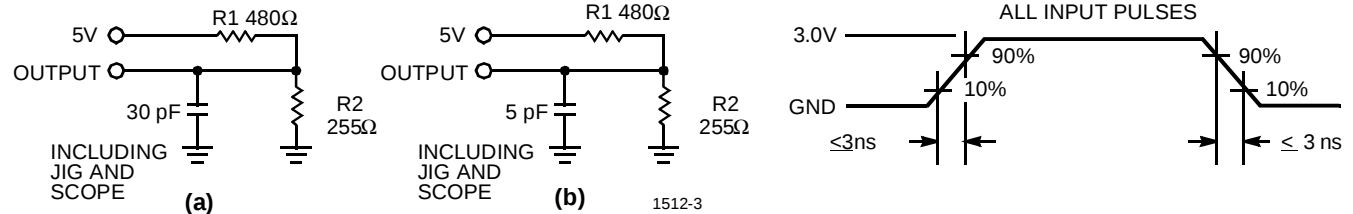
### Notes:

- $V_{IL}(\text{min.}) = -2.0V$  for pulse durations of less than 20 ns.
- $T_A$  is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

## Capacitance<sup>[5]</sup>

| Parameter        | Description        | Test Conditions                                             | Max. | Unit |
|------------------|--------------------|-------------------------------------------------------------|------|------|
| C <sub>IN</sub>  | Input Capacitance  | T <sub>A</sub> = 25°C, f = 1 MHz,<br>V <sub>CC</sub> = 5.0V | 9    | pF   |
| C <sub>OUT</sub> | Output Capacitance |                                                             | 9    | pF   |

## AC Test Loads and Waveforms



Equivalent to: THVENIN EQUIVALENT  
 OUTPUT — 167Ω — 1.73V

## Switching Characteristics<sup>[3, 6]</sup> Over the Operating Range

| Parameter                  | Description                                                                       | 7C1512-15 |      | 7C1512-20 |      | 7C1512-25 |      | Unit |
|----------------------------|-----------------------------------------------------------------------------------|-----------|------|-----------|------|-----------|------|------|
|                            |                                                                                   | Min.      | Max. | Min.      | Max. | Min.      | Max. |      |
| READ CYCLE                 |                                                                                   |           |      |           |      |           |      |      |
| t <sub>RC</sub>            | Read Cycle Time                                                                   | 15        |      | 20        |      | 25        |      | ns   |
| t <sub>AA</sub>            | Address to Data Valid                                                             |           | 15   |           | 20   |           | 25   | ns   |
| t <sub>OHA</sub>           | Data Hold from Address Change                                                     | 3         |      | 3         |      | 5         |      | ns   |
| t <sub>ACE</sub>           | $\overline{CE}_1$ LOW to Data Valid, CE <sub>2</sub> HIGH to Data Valid           |           | 15   |           | 20   |           | 25   | ns   |
| t <sub>DOE</sub>           | $\overline{OE}$ LOW to Data Valid                                                 |           | 7    |           | 8    |           | 10   | ns   |
| t <sub>LZOE</sub>          | $\overline{OE}$ LOW to Low Z                                                      | 0         |      | 0         |      | 0         |      | ns   |
| t <sub>HZOE</sub>          | $\overline{OE}$ HIGH to High Z <sup>[7, 8]</sup>                                  |           | 7    |           | 8    |           | 10   | ns   |
| t <sub>LZCE</sub>          | $\overline{CE}_1$ LOW to Low Z, CE <sub>2</sub> HIGH to Low Z <sup>[8]</sup>      | 3         |      | 3         |      | 5         |      | ns   |
| t <sub>HZCE</sub>          | $\overline{CE}_1$ HIGH to High Z, CE <sub>2</sub> LOW to High Z <sup>[7, 8]</sup> |           | 7    |           | 8    |           | 10   | ns   |
| t <sub>PU</sub>            | $\overline{CE}_1$ LOW to Power-Up, CE <sub>2</sub> HIGH to Power-Up               | 0         |      | 0         |      | 0         |      | ns   |
| t <sub>PD</sub>            | $\overline{CE}_1$ HIGH to Power-Down, CE <sub>2</sub> LOW to Power-Down           |           | 15   |           | 20   |           | 25   | ns   |
| WRITE CYCLE <sup>[9]</sup> |                                                                                   |           |      |           |      |           |      |      |
| t <sub>WC</sub>            | Write Cycle Time                                                                  | 15        |      | 20        |      | 25        |      | ns   |
| t <sub>SCE</sub>           | $\overline{CE}_1$ LOW to Write End, CE <sub>2</sub> HIGH to Write End             | 12        |      | 15        |      | 20        |      | ns   |
| t <sub>AW</sub>            | Address Set-Up to Write End                                                       | 12        |      | 15        |      | 20        |      | ns   |
| t <sub>HA</sub>            | Address Hold from Write End                                                       | 0         |      | 0         |      | 0         |      | ns   |
| t <sub>SA</sub>            | Address Set-Up to Write Start                                                     | 0         |      | 0         |      | 0         |      | ns   |
| t <sub>PWE</sub>           | $\overline{WE}$ Pulse Width                                                       | 12        |      | 15        |      | 20        |      | ns   |
| t <sub>SD</sub>            | Data Set-Up to Write End                                                          | 8         |      | 10        |      | 15        |      | ns   |
| t <sub>HD</sub>            | Data Hold from Write End                                                          | 0         |      | 0         |      | 0         |      | ns   |
| t <sub>LZWE</sub>          | $\overline{WE}$ HIGH to Low Z <sup>[8]</sup>                                      | 3         |      | 3         |      | 5         |      | ns   |
| t <sub>HZWE</sub>          | $\overline{WE}$ LOW to High Z <sup>[7, 8]</sup>                                   |           | 7    |           | 8    |           | 10   | ns   |

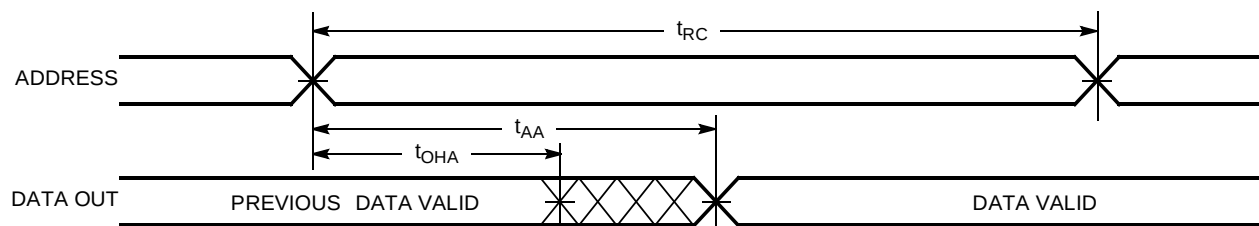
- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE_1}$  LOW, CE<sub>2</sub> HIGH, and  $\overline{WE}$  LOW.  $\overline{CE_1}$  and  $\overline{WE}$  must be LOW and CE<sub>2</sub> HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

**Switching Characteristics**<sup>[3, 6]</sup> Over the Operating Range (continued)

| Parameter                  | Description                                                                       | 7C1512-35 |      | 7C1512-70 |      | Unit |
|----------------------------|-----------------------------------------------------------------------------------|-----------|------|-----------|------|------|
|                            |                                                                                   | Min.      | Min. | Min.      | Min. |      |
| READ CYCLE                 |                                                                                   |           |      |           |      |      |
| t <sub>RC</sub>            | Read Cycle Time                                                                   | 35        |      | 70        |      | ns   |
| t <sub>AA</sub>            | Address to Data Valid                                                             |           | 35   |           | 70   | ns   |
| t <sub>OHA</sub>           | Data Hold from Address Change                                                     | 5         |      | 5         |      | ns   |
| t <sub>ACE</sub>           | $\overline{CE}_1$ LOW to Data Valid, CE <sub>2</sub> HIGH to Data Valid           |           | 35   |           | 70   | ns   |
| t <sub>DOE</sub>           | $\overline{OE}$ LOW to Data Valid                                                 |           | 15   |           | 15   | ns   |
| t <sub>LZOE</sub>          | $\overline{OE}$ LOW to Low Z                                                      | 0         |      | 0         |      | ns   |
| t <sub>HZOE</sub>          | $\overline{OE}$ HIGH to High Z <sup>[7, 8]</sup>                                  |           | 15   |           | 15   | ns   |
| t <sub>LZCE</sub>          | $\overline{CE}_1$ LOW to Low Z, CE <sub>2</sub> HIGH to Low Z <sup>[8]</sup>      | 5         |      | 5         |      | ns   |
| t <sub>HZCE</sub>          | $\overline{CE}_1$ HIGH to High Z, CE <sub>2</sub> LOW to High Z <sup>[7, 8]</sup> |           | 15   |           | 15   | ns   |
| t <sub>PU</sub>            | $\overline{CE}_1$ LOW to Power-Up, CE <sub>2</sub> HIGH to Power-Up               | 0         |      | 0         |      | ns   |
| t <sub>PD</sub>            | $\overline{CE}_1$ HIGH to Power-Down, CE <sub>2</sub> LOW to Power-Down           |           | 35   |           | 70   | ns   |
| WRITE CYCLE <sup>[9]</sup> |                                                                                   |           |      |           |      |      |
| t <sub>WC</sub>            | Write Cycle Time                                                                  | 35        |      | 70        |      | ns   |
| t <sub>SCE</sub>           | $\overline{CE}_1$ LOW to Write End, CE <sub>2</sub> HIGH to Write End             | 25        |      | 60        |      | ns   |
| t <sub>AW</sub>            | Address Set-Up to Write End                                                       | 25        |      | 60        |      | ns   |
| t <sub>HA</sub>            | Address Hold from Write End                                                       | 0         |      | 0         |      | ns   |
| t <sub>SA</sub>            | Address Set-Up to Write Start                                                     | 0         |      | 0         |      | ns   |
| t <sub>PWE</sub>           | $\overline{WE}$ Pulse Width                                                       | 25        |      | 60        |      | ns   |
| t <sub>SD</sub>            | Data Set-Up to Write End                                                          | 20        |      | 55        |      | ns   |
| t <sub>HD</sub>            | Data Hold from Write End                                                          | 0         |      | 0         |      | ns   |
| t <sub>LZWE</sub>          | $\overline{WE}$ HIGH to Low Z <sup>[8]</sup>                                      | 5         |      | 5         |      | ns   |
| t <sub>HZWE</sub>          | $\overline{WE}$ LOW to High Z <sup>[7, 8]</sup>                                   |           | 15   |           | 15   | ns   |

**Switching Waveforms**

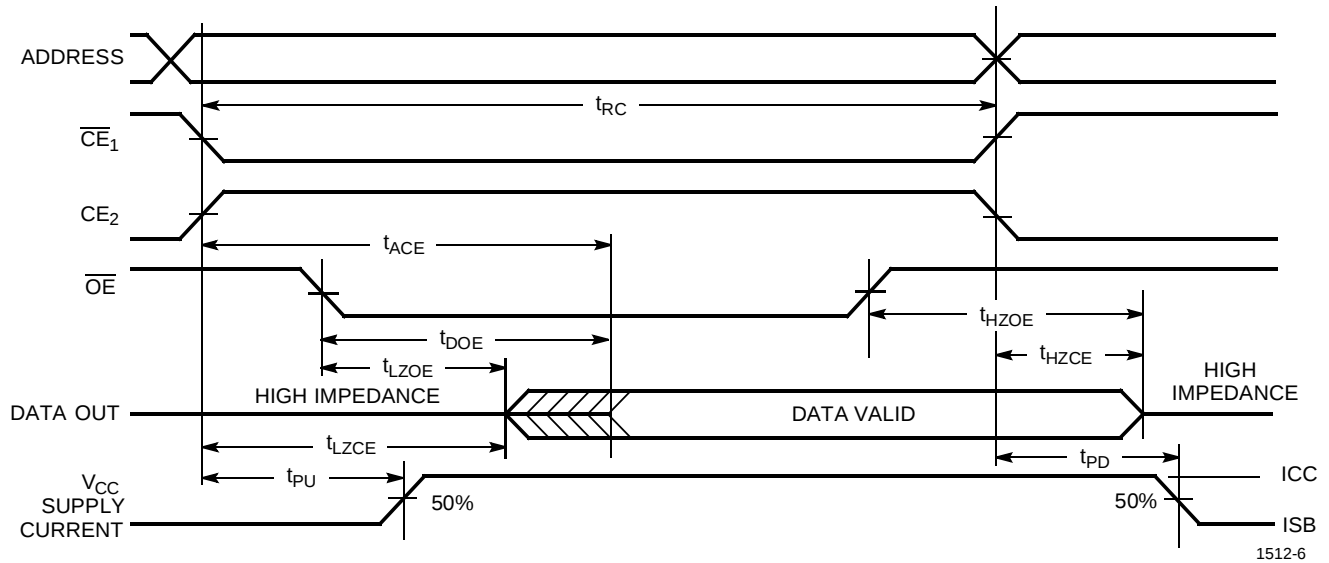
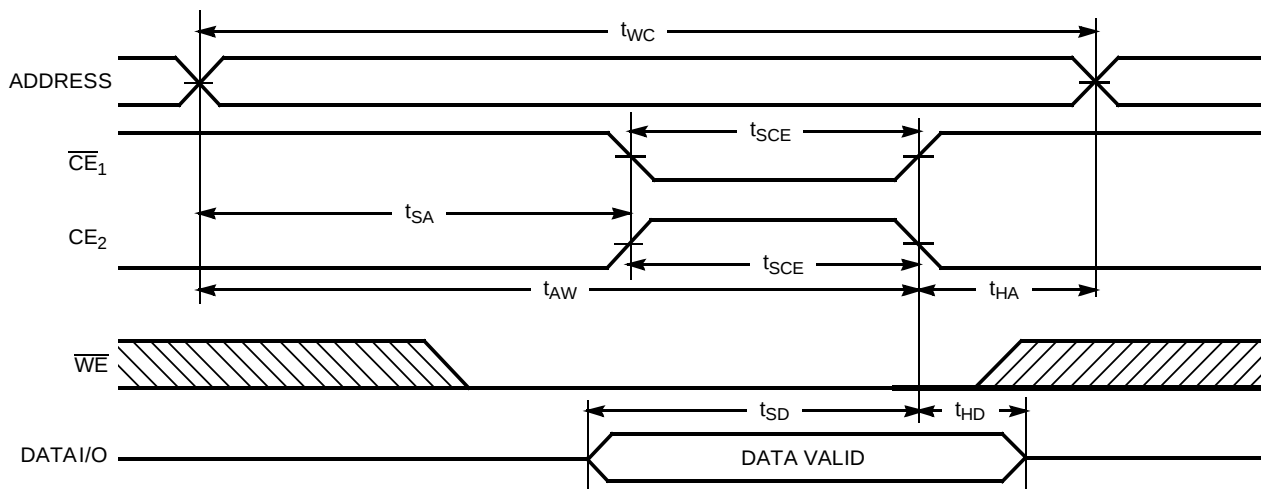
**Read Cycle No. 1**<sup>[10, 11]</sup>



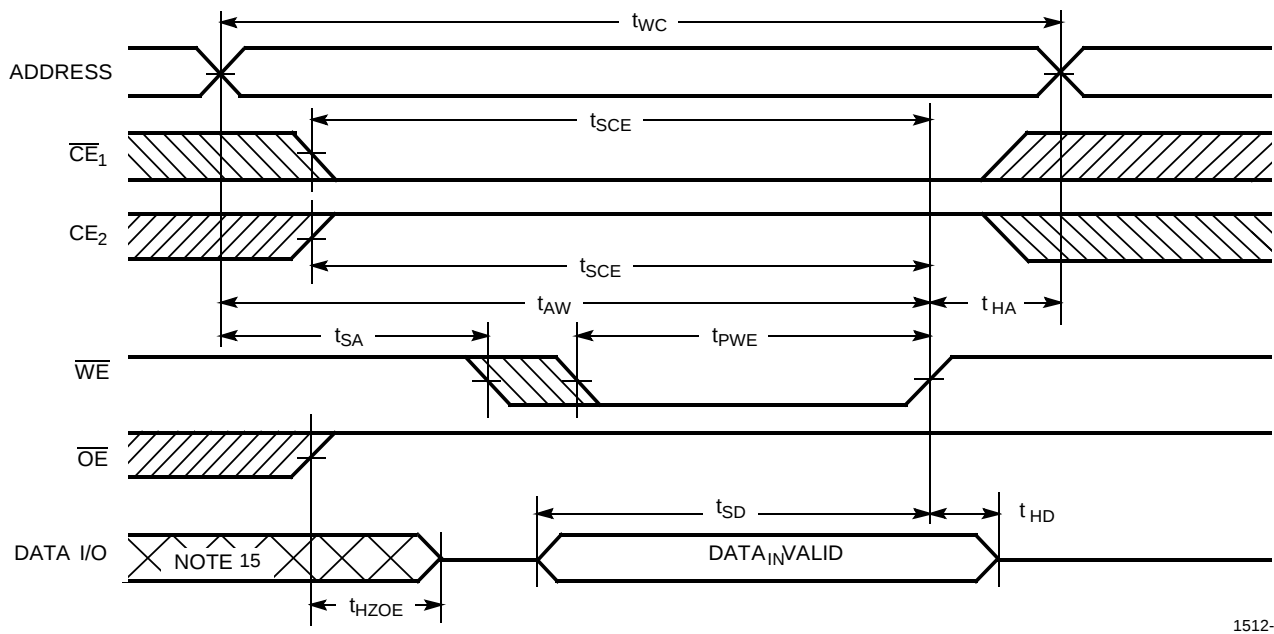
1512-5

**Notes:**

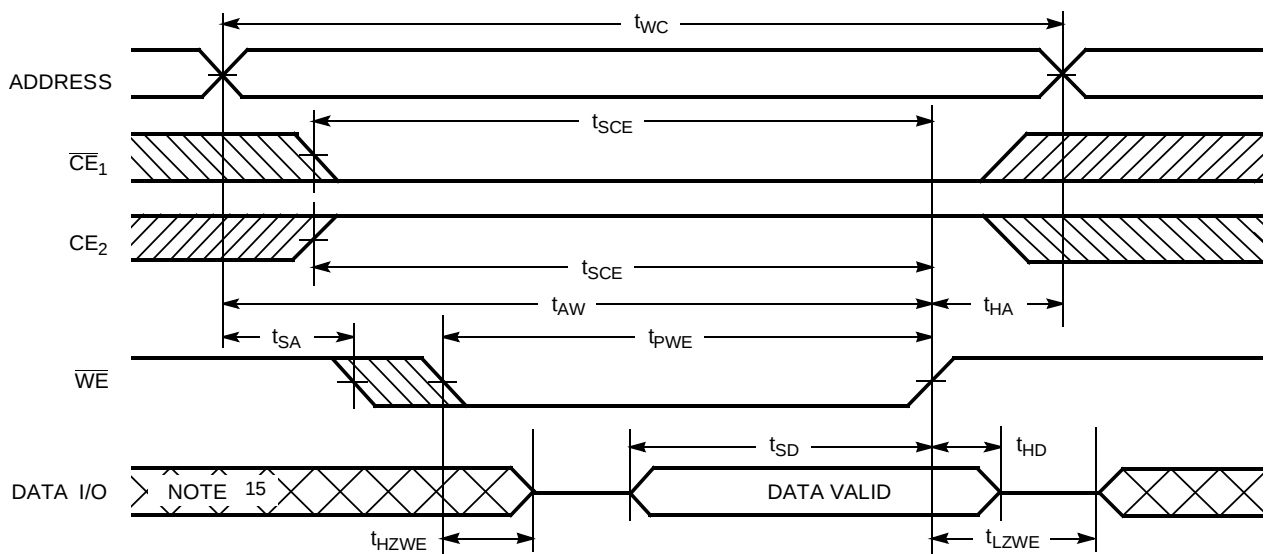
10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .  
 11.  $\overline{WE}$  is HIGH for read cycle.

**Switching Waveforms (continued)**
**Read Cycle No. 2 ( $\overline{OE}$  Controlled) [11, 12]**

**Write Cycle No. 1 ( $\overline{CE}_1$  or  $CE_2$  Controlled) [13, 14]**

**Notes:**

12. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.
13. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
14. If  $\overline{CE}_1$  goes HIGH or  $CE_2$  goes LOW simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.

**Switching Waveforms (continued)**
**Read Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[13, 14]</sup>**


1512-8

**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[14]</sup>**


1512-9

**Note:**

15. During this period the I/Os are in the output state and input signals should not be applied.



### Truth Table

| $\overline{CE}_1$ | $CE_2$ | $\overline{OE}$ | $\overline{WE}$ | I/O <sub>0</sub> – I/O <sub>7</sub> | Mode                       | Power                |
|-------------------|--------|-----------------|-----------------|-------------------------------------|----------------------------|----------------------|
| H                 | X      | X               | X               | High Z                              | Power-Down                 | Standby ( $I_{SB}$ ) |
| X                 | L      | X               | X               | High Z                              | Power-Down                 | Standby ( $I_{SB}$ ) |
| L                 | H      | L               | H               | Data Out                            | Read                       | Active ( $I_{CC}$ )  |
| L                 | H      | X               | L               | Data In                             | Write                      | Active ( $I_{CC}$ )  |
| L                 | H      | H               | H               | High Z                              | Selected, Outputs Disabled | Active ( $I_{CC}$ )  |

### Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type                  | Operating Range |
|------------|---------------|--------------|-------------------------------|-----------------|
| 15         | CY7C1512-15SC | S34          | 32-Lead (450-Mil) Molded SOIC | Commercial      |
|            | CY7C1512-15ZC | Z32          | 32-Lead TSOP Type I           |                 |
|            | CY7C1512-20ZI | Z32          | 32-Lead TSOP Type I           | Industrial      |
| 20         | CY7C1512-20SC | S34          | 32-Lead (450-Mil) Molded SOIC | Commercial      |
|            | CY7C1512-20ZC | Z32          | 32-Lead TSOP Type I           |                 |
|            | CY7C1512-20ZI | Z32          | 32-Lead TSOP Type I           | Industrial      |
| 25         | CY7C1512-25SC | S34          | 32-Lead (450-Mil) Molded SOIC | Commercial      |
|            | CY7C1512-25ZC | Z32          | 32-Lead TSOP Type I           |                 |
|            | CY7C1512-25ZI | Z32          | 32-Lead TSOP Type I           | Industrial      |
| 35         | CY7C1512-35SC | S34          | 32-Lead (450-Mil) Molded SOIC | Commercial      |
| 70         | CY7C1512-70SC | S34          | 32-Lead (450-Mil) Molded SOIC | Commercial      |
|            | CY7C1512-70ZC | Z32          | 32-Lead TSOP Type I           |                 |
|            | CY7C1512-70ZI | Z32          | 32-Lead TSOP Type I           | Industrial      |

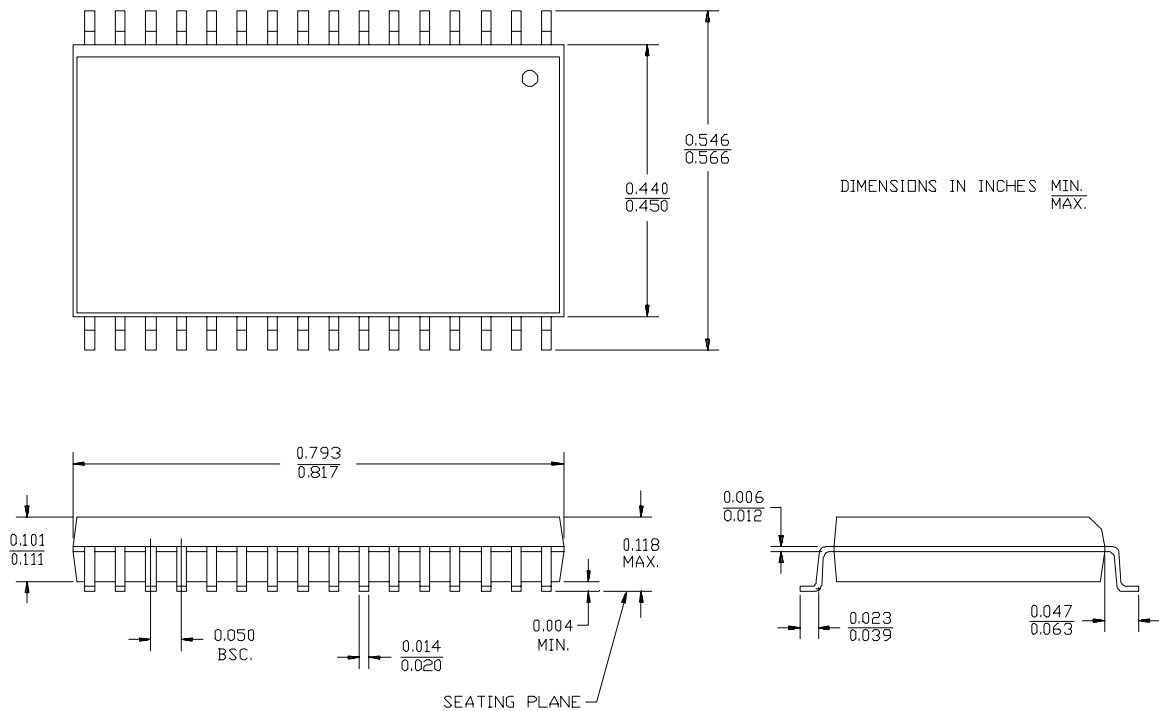
Shaded areas contain advanced information.

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***PRELIMINARY***

**CY7C1512**

**Package Diagrams**
**32-Lead (450 -Mil) Molded SOIC S34**

**32-Lead Thin Small Outline Package Z32**
