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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

Character Display Module

Part Number

C162ALBFGS16WN55PAB

Overview

Display area: 80mm x 36mm (16 x 2)
FSTN, Black background, RGB Edge lit, Bottom view, Wide temp, Transmissive (negative), 5V LCD, 5V LED, Controller=ST7066U,
RoHS Compliant

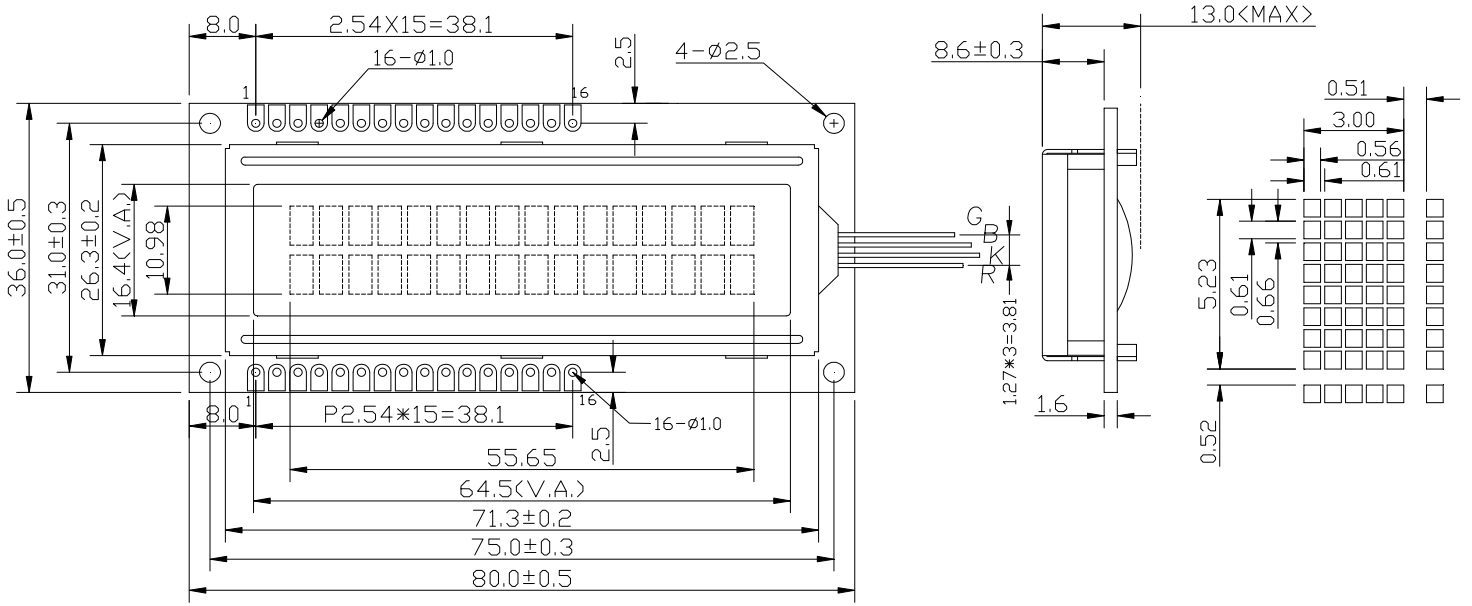
1. 5x8 dots with cursor
2. 16characters *2lines display
3. 4-bit or 8-bit MPU interfaces
4. Built-in controller (ST7066U or equivalent)
5. Display Mode & Backlight Variations
6. ROHS Compliant

LCD type	☐TN			
	☐FSTN	☑FSTN Negative		
	☐STN Yellow Green	☐STN Gray	☐STN Blue Negative	
View direction	☑6 O'clock	☐12 O'clock		
Rear Polarizer	☐Reflective	☑Transflective	☐Transmissive	
Backlight Type	☐LED Array	☐EL	☐Internal Power	☐3.0V Input
	☑LED Edge	☐CCFL	☑External Power	☐5.0V Input
Backlight Color	☐White	☐ Blue	☐ Amber	☑Red-Green-Blue
Temperature Range	☐Normal	☑Wide	☐Super Wide	
DC to DC circuit	☐Build-in	☑Not Build-in		
Touch screen	☐With	☑Without		
Font type	☑English-Japanese	☐English-Europen	☐English-Russian	☐other

MECHANICAL SPECIFICATIONS

Module size	80.0mm(L)*36.0mm(W)* Max13.0(H)mm
Viewing area	64.5mm(L)*16.4mm(W)
Character size	3.00mm(L)*5.23mm(W)
Character pitch	3.51mm(L)*5.75mm(W)
Weight	Approx.

REV	DESCRIPTION:	DATE
1.0	First	



PIN ASSIGNMENT

1	VSS
2	VDD
3	V0
4	RS
5	RW
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	K
16	A-Red
17	A-Green
18	A-Blue

Notes:

1). Driver Method: 1/16duty, 1/5bias, VDD5.0V VLCD4.5V
2). Display Type: FSTN/Negative/Transflective/6:00 Visual Angle
3). Operating Temp: -20°C~70°C/Storage Temp: -30°C~80°C
4). Backlight Type: Edge/ RGB/ 5V
5). Driver: ST7066U/4bit or 8bit MPU
6). RoHS Compliant

Model Name:

AFF.

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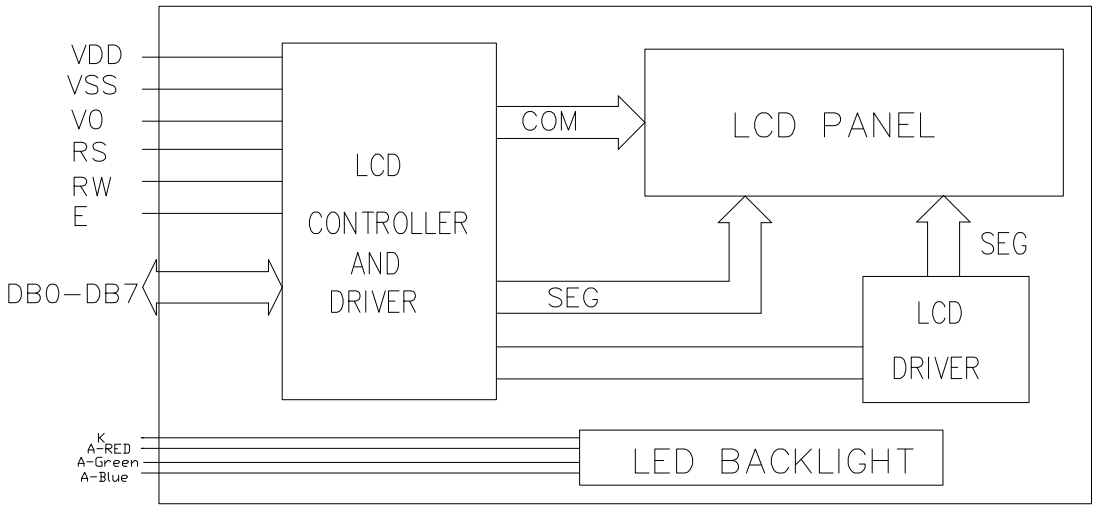
Absolute maximum ratings

Item	Symbol	Standard			Unit
Power voltage	V_{DD}-V_{SS}	0	-	7.0	V
Input voltage	V_{IN}	VSS	-	VDD	
Operating temperature range	V_{OP}	-20	-	+70	℃
Storage temperature range	V_{ST}	-30	-	+80	

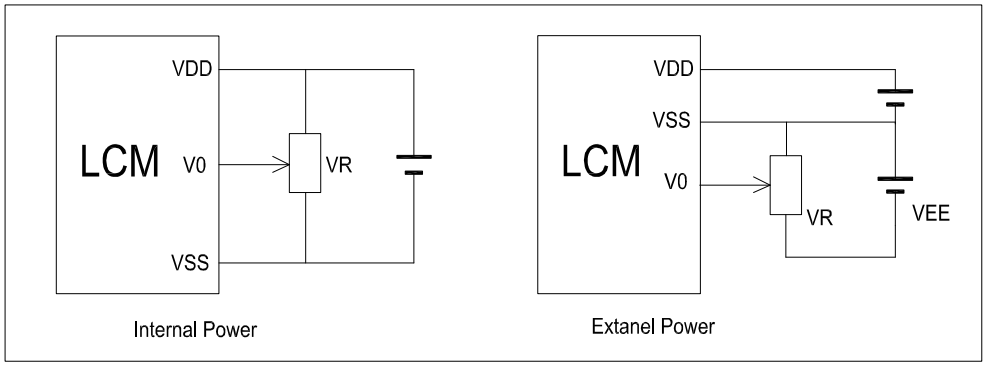
Block diagram



Interface pin description

Pin no.	Symbol	External connection	Function
1	Vss	Power supply	Signal ground for LCM
2	V_{DD}		Power supply for logic for LCM
3	V_0		Contrast adjust
4	RS	MPU	Register select signal
5	R/W	MPU	Read/write select signal
6	E	MPU	Operation (data read/write) enable signal
7~10	DB0~DB3	MPU	Four low order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCM. These four are not used during 4-bit operation.
11~14	DB4~DB7	MPU	Four high order bi-directional three-state data bus lines. Used for data transfer between the MPU
15	K	Power supply	Signal ground for BKL
16	A-Red		Signal ground for LCM
17	A-Green		Signal ground for LCM
18	A-Blue		Signal ground for LCM

Contrast adjust



V_{DD}-V_0: LCD Driving voltage
VR: 10k~20k

8. Optical characteristics

FSTN type display module (Ta=25℃, VDD=5.0V)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle (6 0'clock)	Left--Right	θ	Ta=25℃	-	60	-	deg
	Top--Bottom	θ		-	70	-	
Contrast ratio		CR	Ta=25℃	3	5	-	-
Response time	Rise	t_r		-	150	250	ms
	Tall	t_f		-	200	300	

Electrical characteristics

DC characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage for LCD	V_{DD}-V_0	Ta =25℃	4.3	4.5	4.7	V
Input voltage	V_{DD}		4.8	5.0	5.2	
Supply current	I_{DD}	Ta=25℃, V_{DD}=5.0V	-	1.5	2.5	mA
Input leakage current	I_{LKG}		-	-	1.0	uA
"H" level input voltage	V_{IH}		2.2	-	V_{DD}	V
"L" level input voltage	V_{IL}	Twice initial value or less	0	-	0.6	
"H" level output voltage	V_{OH}	LOH=-0.25mA	2.4	-	-	
"L" level output voltage	V_{OL}	LOH=1.6mA	-	-	0.4	

Backlight information (Ta =25℃)

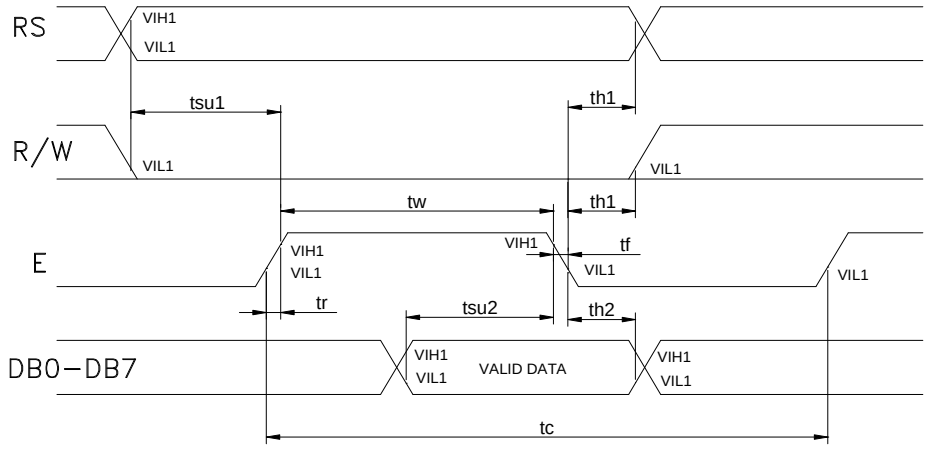
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Current	I_{LED}	Vf=2.0V, Red	-	10	20	mA
		Vf=3.0V, Green	-	15	20	
		Vf=3.0V, Blue	-	15	20	
Supply voltage	Vf	Red	1.8	-	2.2	V
		Green	2.8	-	3.3	
		Blue	2.8	-	3.3	
Reverse voltage	VR	Ta=25℃,	-	5.0	-	
Luminous Intensity	IV	Red	-	55	60	Cd/m2
		Green	-	190	200	
		Blue	-	25	30	
Peak wavelength	V_{IH}	Red	630	-	645	nm
		Green	515	-	525	
		Blue	465	-	475	

10. Timing Characteristics

Write cycle (Ta=25℃, VDD=5.0V)

Parameter	Symbol	Test pin	Min.	Typ.	Max.	Unit
Enable cycle time	t_c	E	500	-	-	ns
Enable pulse width	t_w		300	-	-	
Enable rise/fall time	t_r, t_f		-	-	25	
RS; R/W setup time	t_{su1}	RS; R/W	100	-	-	
RS; R/W address hold time	t_{h1}	RS; R/W	10	-	-	
Read data output delay	t_{su2}	DB0~DB7	60	-	-	
Read data hold time	t_{h2}		10	-	-	

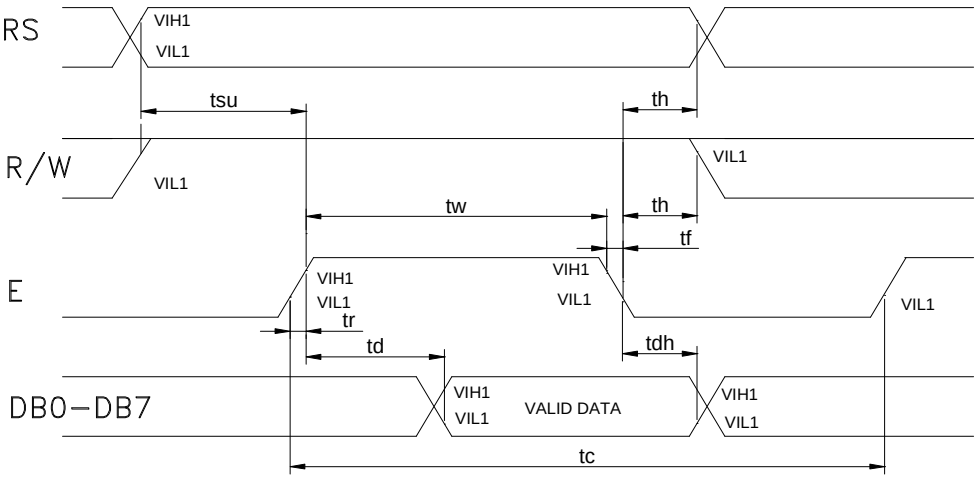
Write mode timing diagram



Read cycle (Ta=25℃, VDD=5.0V)

Parameter	Symbol	Test pin	Min.	Typ.	Max.	Unit
Enable cycle time	t_c	E	500	-	-	ns
Enable pulse width	t_w		300	-	-	
Enable rise/fall time	t_r, t_f		-	-	25	
RS; R/W setup time	t_{su}	RS; R/W	100	-	-	
RS; R/W address hold time	t_h	RS; R/W	10	-	-	
Read data output delay	t_d	DB0~DB7	60	-	90	
Read data hold time	t_{dh}		20	-	-	

Read mode timing diagram



Instruction description

Outline

To overcome the speed difference between the internal clock of SPLC780D and the MPU clock, SPLC780D performs internal operations by storing control in formations to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus (Refer to Table7).
Instructions can be divided largely into four groups:

1) SPLC780D function set instructions (set display methods, set data length, etc.)
2) Address set instructions to internal RAM
3) Data transfer instructions with internal RAM
4) Others

The address of the internal RAM is automatically increased or decreased by 1.

Note: during internal operation, busy flag (DB7) is read “High”.
Busy flag check must be preceded by the next instruction.

11.2 Instruction Table

Instruction	Instruction code										Description	Execution time (fosc= 270 KHZ
	RS	R/W	DB7	DB6	DB 5	DB4	DB3	DB2	DB 1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write “20H” to DDRA and set DDRAM address to “00H” from AC	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to “00H” From AC and return cursor to Its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction And blinking of entire display	39us
Display ON/ OFF control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and Blinking of cursor (B) on/off Control bit.	
Cursor or Display shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display Shift control bit, and the Direction, without changing of DDRAM data.	39us
Function set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-Bit/4-bit), numbers of display Line (N: =2-line/1-line) and, Display font type (F: 5x11/5x8)	39us
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address Counter.	39us
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address Counter.	39us
Read busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal Operation or not can be known By reading BF. The contents of Address counter can also be read.	0us
Write data to Address	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43us
Read data From RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43us

NOTE:
When an MPU program with checking the busy flag (DB7) is made, it must be necessary 1/2fosc is necessary for executing the next instruction by the falling edge of the “E” signal after the busy flag (DB7) goes to “Low”.

Contents

1) Clear display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing “20H” (space code) to all DDRAM address, and set DDRAM address to “00H” into AC (address counter).

Return cursor to the original status, namely, bring the cursor to the left edge on the fist line of the display.

Make the entry mode increment (I/D=“High”).

2) Return home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

Return home is cursor return home instruction.

Set DDRAM address to “00H” into the address counter.

Return cursor to its original site and return display to its original status, if shifted.

Contents of DDRAM does not change.

3) Entry mode set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.

I/D: increment / decrement of DDRAM address (cursor or blink)

When I/D=“high”, cursor/blink moves to right and DDRAM address is increased by 1.

When I/D=“Low”, cursor/blink moves to left and DDRAM address is increased by 1.

*CGRAM operates the same way as DDRAM, when reading from or writing to CGRAM.

SH: shift of entire display

When DDRAM read (CGRAM read/write) operation or SH=“Low”, shifting of entire display is not performed. If SH =“High” and DDRAM write operation, shift of entire display is performed according to I/D value. (I/D=“high”. shift left, I/D=“Low”. Shift right).

4) Display ON/OFF control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF control bit

When D=“High”, entire display is turned on.

When D=“Low”, display is turned off, but display data remains in DDRAM.

C: cursor ON/OFF control bit

When D=“High”, cursor is turned on.

When D=“Low”, cursor is disappeared in current display, but I/D register preserves its data.

B: Cursor blink ON/OFF control bit

When B=“High”, cursor blink is on, which performs alternately between all the “High” data and display characters at the cursor position.

When B=“Low”, blink is off.

5) Cursor or display shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shifting of right/left cursor position or display without writing or reading of display data.
This instruction is used to correct or search display data.
During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line.
Note that display shift is performed simultaneously in all the lines.
When display data is shifted repeatedly, each line is shifted individually.
When display shift is performed, the contents of the address counter are not changed.

Shift patterns according to S/C and R/L bits

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

6) Function set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

DL: Interface data length control bit
When DL="High", it means 8-bit bus mode with MPU.
When DL="Low", it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.
When 4-but bus mode, it needs to transfer 4-bit data twice.

N: Display line number control bit
When N="Low", 1-line display mode is set.
When N="High", 2-line display mode is set.

F: Display line number control bit
When F="Low", 5x8 dots format display mode is set.
When F="High", 5x11 dots format display mode.

7) Set CGRAM address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
The instruction makes CGRAM data available from MPU.

8) Set DDRAM address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available form MPU.
When 1-line display mode (N=LOW), DDRAM address is form "00H" to "4FH".In 2-line display mode (N=High), DDRAM address in the 1st line form "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

9) Read busy flag & address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether SPLC780D is in internal operation or not.
If the resultant BF is “High”, internal operation is in progress and should wait BF is to be LOW, which by then the nest instruction can be performed. In this instruction you can also read the value of the address counter.

10) Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.
The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction (DDRAM address set, CGRAM address set).
RAM set instruction can also determine the AC direction to RAM.
After write operation. The address is automatically increased/decreased by 1, according to the entry mode.

11) Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, the data that has been read first is invalid, as the direction of AC is not yet determined. If RAM data is read several times without RAM address instructions set before, read operation, the correct RAM data can be obtained from the second. But the first data would be incorrect, as there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction, it also transfers RAM data to output data register.

After read operation, address counter is automatically increased/decreased by 1 according to the entry mode.

After CGRAM read operation, display shift may not be executed correctly.

NOTE: In case of RAM write operation, AC is increased/decreased by 1 as in read operation.
At this time, AC indicates next address position, but only the previous data can be read by the read instruction.

Display character address code:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

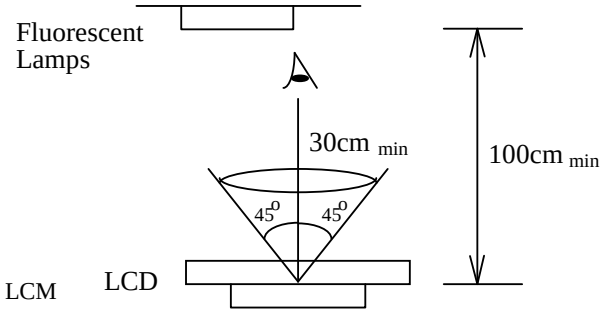
Standard character pattern

QUALITY SPECIFICATIONS

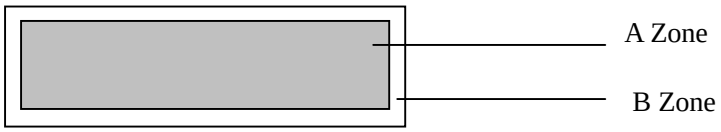
Standard of the product appearance test

Manner of appearance test: The inspection should be performed in using 20W x 2 fluorescent lamps. Distance between LCM and fluorescent lamps should be 100 cm or more. Distance between LCM and inspector eyes should be 30 cm or more.

Viewing direction for inspection is 45° from vertical against LCM.



Definition of zone:



A Zone: Active display area (minimum viewing area).
B Zone: Non-active display area (outside viewing area).

Specification of quality assurance

AQL inspection standard

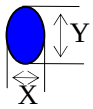
Sampling method: MIL-STD-105E, Level II, single sampling

Defect classification **(Note: * is not including)**

Classify	Item		Note	AQL
Major	Display state	Short or open circuit	1	0.65
		LC leakage		
		Flickering		
		No display		
		Wrong viewing direction		
		Contrast defect (dim, ghost)	2	
		Back-light	1,8	
	Non-display	Flat cable or pin reverse	10	
		Wrong or missing component	11	
Minor	Display state	Background color deviation	2	1.0
		Black spot and dust	3	
		Line defect, Scratch	4	
		Rainbow	5	
		Chip	6	
		Pin hole	7	
	Polarizer	Protruded	12	
		Bubble and foreign material	3	
	Soldering	Poor connection	9	
	Wire	Poor connection	10	
	TAB	Position, Bonding strength	13	

Note on defect classification

<table>
<tr><th>No.</th><th>Item</th><th>Criterion</th></tr>
<tr><td rowspan="6">1</td><td>Short or open circuit</td><td rowspan="6">Not allow</td></tr>
<tr><td>LC leakage</td></tr>
<tr><td>Flickering</td></tr>
<tr><td>No display</td></tr>
<tr><td>Wrong viewing direction</td></tr>
<tr><td>Wrong Back-light</td></tr>
<tr><td rowspan="2">2</td><td>Contrast defect</td><td rowspan="2">Refer to approval sample</td></tr>
<tr><td>Background color deviation</td></tr>
<tr><td>3</td><td>Point defect,
Black spot, dust
(including Polarizer)

ϕ = (X+Y)/2</td><td> 

<table>
<tr><th>Point Size</th><th>Acceptable Qty.</th></tr>
<tr><td>ϕ≤0.10</td><td>Disregard</td></tr>
<tr><td>0.10<ϕ≤0.20</td><td>3</td></tr>
<tr><td>0.20<ϕ≤0.25</td><td>2</td></tr>
<tr><td>0.25<ϕ≤0.30</td><td>1</td></tr>
<tr><td>ϕ>0.30</td><td>0</td></tr>
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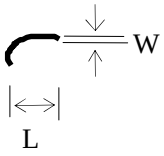
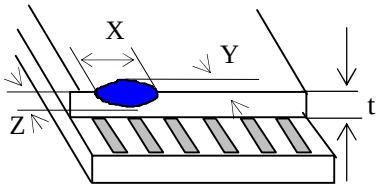
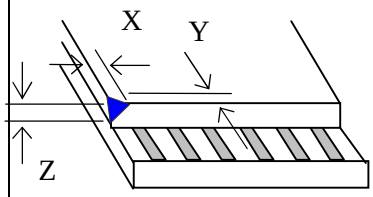
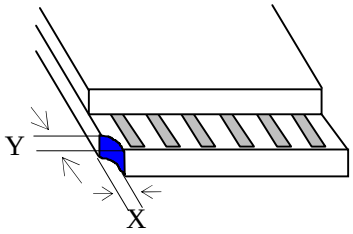
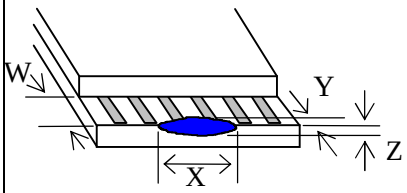
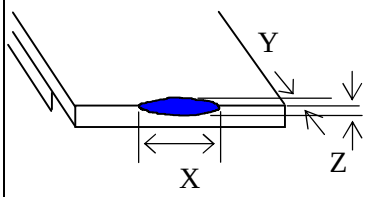
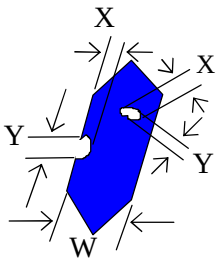
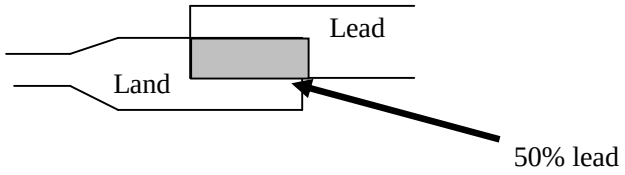
Unit: mm</td></tr>
<tr><td>4</td><td>Line defect,

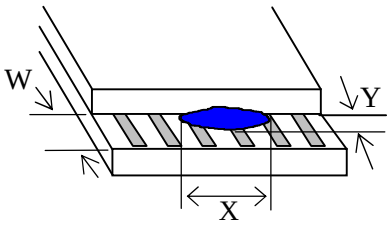
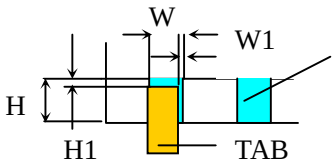
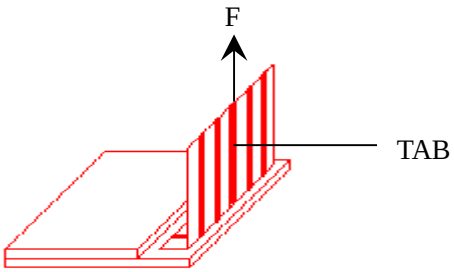
Scratch</td><td> 

<table>
<tr><th colspan="2">Line</th><th>Acceptable Qty.</th></tr>
<tr><td>L</td><td>W</td><td></td></tr>
<tr><td>---</td><td>0.015≥W</td><td>Disregard</td></tr>
<tr><td>3.0≥L</td><td>0.03≥W</td><td rowspan="2">2</td></tr>
<tr><td>2.0≥L</td><td>0.05≥W</td></tr>
<tr><td>1.0≥L</td><td>0.1>W</td><td>1</td></tr>
<tr><td>---</td><td>0.05<W</td><td>Applied as point defect</td></tr>
</table>
Unit: mm</td></tr>
<tr><td>5</td><td>Rainbow</td><td>Not more than two color changes across the viewing area.</td></tr>
</table>

No	Item	Criterion
6	Chip Remark: X: Length direction Y: Short direction Z: Thickness direction t: Glass thickness W: Terminal Width	 Acceptable criterion X: ≤2; Y: 0.5mm; Z: ≤t/2  Acceptable criterion X: ≤2; Y: 0.5mm; Z: ≤t  Acceptable criterion X: ≤3; Y: ≤2; Z: ≤t shall not reach to ITO  Acceptable criterion X: Disregard; Y: ≤0.2; Z: ≤t  Acceptable criterion X: ≤5; Y: ≤2; Z: ≤t/3

<table>
<tr><th>No.</th><th>Item</th><th>Criterion</th></tr>
<tr><td>7</td><td>Segment
pattern
W = Segment width
ϕ = (X+Y)/2</td><td>(1) Pin hole
ϕ < 0.10mm is acceptable.
 

<table>
<tr><th>Point Size</th><th>Acceptable Qty</th></tr>
<tr><td>ϕ≤1/4W</td><td>Disregard</td></tr>
<tr><td>1/4W< ϕ≤1/2W</td><td>1</td></tr>
<tr><td>ϕ>1/2W</td><td>0</td></tr>
</table>
Unit: mm</td></tr>
<tr><td>8</td><td>Back-light</td><td>(1) The color of backlight should correspond its specification.
(2) Not allow flickering</td></tr>
<tr><td>9</td><td>Soldering</td><td>(1) Not allow heavy dirty and solder ball on PCB.
(The size of dirty refer to point and dust defect)
(2) Over 50% of lead should be soldered on Land.
 
</td></tr>
<tr><td>10</td><td>Wire</td><td>(1) Copper wire should not be rusted
(2) Not allow crack on copper wire connection.
(3) Not allow reversing the position of the flat cable.
(4) Not allow exposed copper wire inside the flat cable.</td></tr>
<tr><td>11*</td><td>PCB</td><td>(1) Not allow screw rust or damage.
(2) Not allow missing or wrong putting of component.</td></tr>
</table>

No	Item	Criterion
12	Protruded W: Terminal Width	 Acceptable criteria: Y ≤ 0.4
13	TAB	1. Position  W1≤1/3W H1≤1/3H 2 TAB bonding strength test  P (=F/TAB bonding width) ≥650gf/cm ,(speed rate: 1mm/min) 5pcs per SOA (shipment)
14	Total no. of acceptable Defect	A. Zone Maximum 2 minor non-conformities per one unit. Defect distance: each point to be separated over 10mm B. Zone It is acceptable when it is no trouble for quality and assembly in customer's end product.