

N-Channel 650 V (D-S) MOSFET

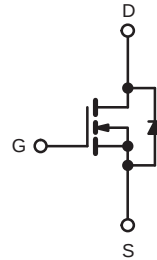
PRODUCT SUMMARY

V_{DS} (V)	650	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	5
Q_g (Max.) (nC)	11	
Q_{gs} (nC)	2.3	
Q_{gd} (nC)	5.2	
Configuration	Single	

FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Compliant to RoHS directive 2002/95/EC


RoHS
TO-220AB

 G D S
 Top View


N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted

ABSOLUTE MAXIMUM RATINGS T _C = 25 °C, unless otherwise noted					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	650	V
Gate-Source Voltage			V _{GS}	± 30	
Continuous Drain Current ^e	V _{GS} at 10 V	T _C = 25 °C	I _D	2.0	A
Continuous Drain Current		T _C = 100 °C		1.28	
Pulsed Drain Current ^a			I _{DM}	8	
Linear Derating Factor				0.48	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	165	mJ
Repetitive Avalanche Current ^a			I _{AR}	2	A
Repetitive Avalanche Energy ^a			E _{AR}	6	mJ
Maximum Power Dissipation	T _C = 25 °C		P _D	45	W
Peak Diode Recovery dV/dt ^c			dV/dt	2.8	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature) ^d	for 10 s			300	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 24\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 3.2\text{ A}$ (see fig. 12).
- $I_{SD} \leq 3.2\text{ A}$, $dI/dt \leq 90\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.
- Drain current limited by maximum junction temperature.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	2.1	

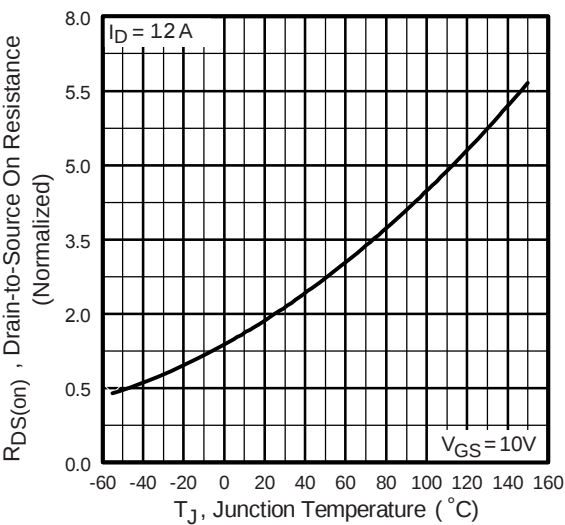
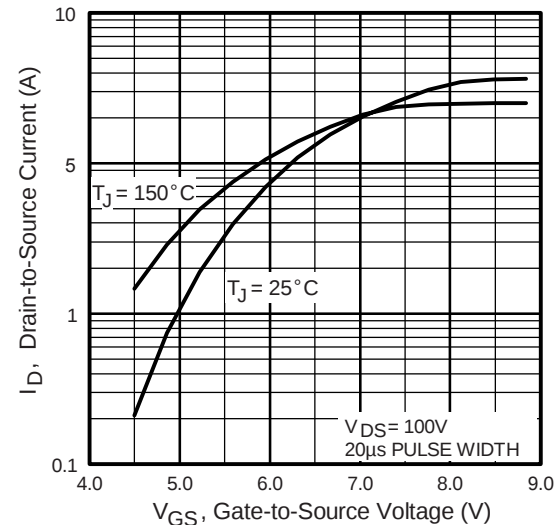
SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$		650	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 1\text{ mA}^d$		-	670	-	mV/ $^{\circ}\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650\text{ V}$, $V_{GS} = 0\text{ V}$		-	-	25	μA
		$V_{DS} = 520\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 1\text{ A}$ ^b	-	4.0	-	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 1\text{ A}$		3.9	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5		-	417	-	pF
Output Capacitance	C_{oss}			-	45	-	
Reverse Transfer Capacitance	C_{rss}			-	5	-	
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}$, $f = 1.0\text{ MHz}$	-	912	-	
			$V_{DS} = 520\text{ V}$, $f = 1.0\text{ MHz}$	-	26		
Effective Output Capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 0\text{ V to } 520\text{ V}^c$	-	42	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 12\text{ A}$, $V_{DS} = 400\text{ V}$ see fig. 6 and 13 ^b	-	-	11	nC
Gate-Source Charge	Q_{gs}			-	-	2.3	
Gate-Drain Charge	Q_{gd}			-	-	5.2	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 325\text{ V}$, $I_D = 1.2\text{ A}$ $R_G = 9.1\text{ }\Omega$, $R_D = 62\text{ }\Omega$, see fig. 10 ^b		-	14	-	ns
Rise Time	t_r			-	20	-	
Turn-Off Delay Time	$t_{d(off)}$			-	34	-	
Fall Time	t_f			-	18	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	2	A	
Pulsed Diode Forward Current ^a	I_{SM}		-	-	8		
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_S = 3.2\text{ A}$, $V_{GS} = 0\text{ V}^b$		-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = 3.2\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$		-	180	230	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	2.1	3.2	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .
- $t = 60\text{ s}$, $f = 60\text{ Hz}$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



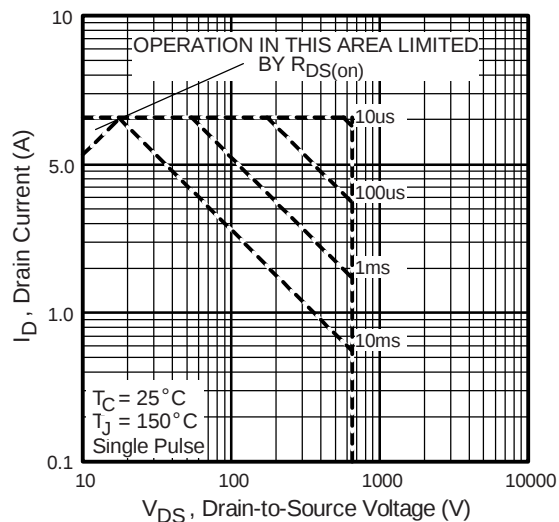
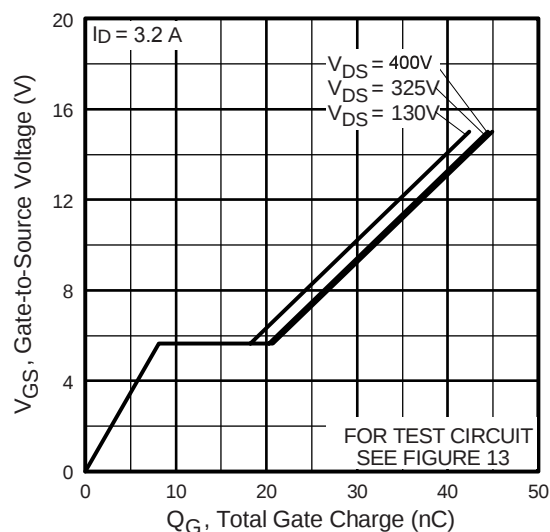




Fig. 9 - Maximum Drain Current vs. Case Temperature



Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms



Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



Fig. 12a - Unclamped Inductive Test Circuit



Fig. 12b - Unclamped Inductive Waveforms



Fig. 12c - Maximum Avalanche Energy vs. Drain Current



Fig. 12d - Typical Drain-to Source Voltage vs. Avalanche Current



Fig. 13a - Basic Gate Charge Waveform

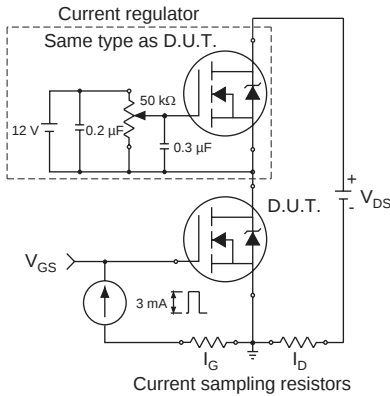


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

TO-220AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118
ECN: X12-0208-Rev. N, 08-Oct-12 DWG: 5471				

Notes

* M = 1.32 mm to 1.62 mm (dimension including protrusion)
Heatsink hole for HVM

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