



Description

The Si4532CDY uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 30V$ $I_D = 7A$

$R_{DS(ON)} < 25m\Omega$ @ $V_{GS}=10V$

$V_{DS} = -30V$ $I_D = -8.5A$

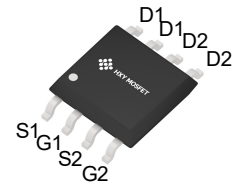
$R_{DS(ON)} < 35m\Omega$ @ $V_{GS} = -10V$

Application

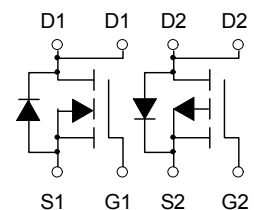
Battery protection

Load switch

Uninterruptible power supply



SOP-8
(SOIC-8)



N-Channel and P-Channel

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
Si4532CDY	SOP-8(SOIC-8)	HXY MOSFET	3000

Absolute Maximum Ratings ($T_c=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D@T_A=25^{\circ}C$	Continuous Drain Current, V_{GS} @ 10V ¹	7	-8.5	A
$I_D@T_A=100^{\circ}C$	Continuous Drain Current, V_{GS} @ 10V ¹	6	-4.6	A
I_{DM}	Pulsed Drain Current ²	20	-28	A
EAS	Single Pulse Avalanche Energy ³	72	62	mJ
I_{AS}	Avalanche Current	21	-19	A
$P_D@T_A=25^{\circ}C$	Total Power Dissipation ⁴	2.5	3.08	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^{\circ}C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	45		$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	30		$^{\circ}C/W$



N-Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	30	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1mA$	---	0.034	---	$V/^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V$, $I_D=6A$	---	18	25	$m\Omega$
		$V_{GS}=4.5V$, $I_D=5A$	---	25	31	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	1.0	1.5	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-5.8	---	$mV/^{\circ}\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=30V$, $V_{GS}=0V$, $T_J=25^{\circ}\text{C}$	---	---	1	μA
		$V_{DS}=30V$, $V_{GS}=0V$, $T_J=55^{\circ}\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=15V$, $I_D=5A$	---	10	---	S
R_g	Gate Resistance	$V_{DS}=24V$, $V_{GS}=0V$, $f=1MHz$	---	2.5	---	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=20V$, $V_{GS}=4.5V$, $I_D=6A$	---	7.2	---	nC
Q_{gs}	Gate-Source Charge		---	1.4	---	
Q_{gd}	Gate-Drain Charge		---	2.2	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=12V$, $V_{GS}=10V$, $R_G=3.3\Omega$ $I_D=5A$	---	3.9	---	ns
T_r	Rise Time		---	9.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	14.5	---	
T_f	Fall Time		---	6.0	---	
C_{iss}	Input Capacitance	$V_{DS}=25V$, $V_{GS}=0V$, $f=1MHz$	---	370	---	pF
C_{oss}	Output Capacitance		---	54	---	
C_{rss}	Reverse Transfer Capacitance		---	40	---	
EAS	Single Pulse Avalanche Energy ⁵	$V_{DD}=25V$, $L=0.1mH$, $I_{AS}=10A$	16	---	---	mJ
I_S	Continuous Source Current ^{1,6}	$V_G=V_D=0V$, Force Current	---	---	7	A
I_{SM}	Pulsed Source Current ^{2,6}		---	---	20	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=5A$, $T_J=25^{\circ}\text{C}$	---	---	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper, $t<10\text{sec}$.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V$, $V_{GS}=10V$, $L=0.1mH$, $I_{AS}=10A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The Min. value is 100% EAS tested guarantee.
- 6.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



P-Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D = -250μA	-30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -30V, V _{GS} =0V,	-	-	-1	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±20V	-	-	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D = -250μA	-1.0	-1.5	-2.5	V
R _{DS(on)}	Static Drain-Source on-Resistance note3	V _{GS} = -10V, I _D = -7A	-	26	35	mΩ
		V _{GS} = -4.5V, I _D = -4A	-	38	54	
C _{iss}	Input Capacitance	V _{DS} = -15V, V _{GS} =0V, f=1.0MHz	-	982	-	pF
C _{oss}	Output Capacitance		-	135	-	pF
C _{rss}	Reverse Transfer Capacitance		-	109	-	pF
Q _g	Total Gate Charge	V _{DS} = -15V, I _D = -4A, V _{GS} = -10V	-	10	-	nC
Q _{gs}	Gate-Source Charge		-	2	-	nC
Q _{gd}	Gate-Drain(“Miller”) Charge		-	2.7	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DD} = -15V, I _D = -7A, V _{GS} = -10V, R _{GEN} =2.5Ω	-	11	-	ns
t _r	Turn-on Rise Time		-	19	-	ns
t _{d(off)}	Turn-off Delay Time		-	45	-	ns
t _f	Turn-off Fall Time		-	26	-	ns
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	-8.5	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-28	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S = -7A	-	-0.8	-1.2	V

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$



N-Typical Characteristics

Figure1: Output Characteristics

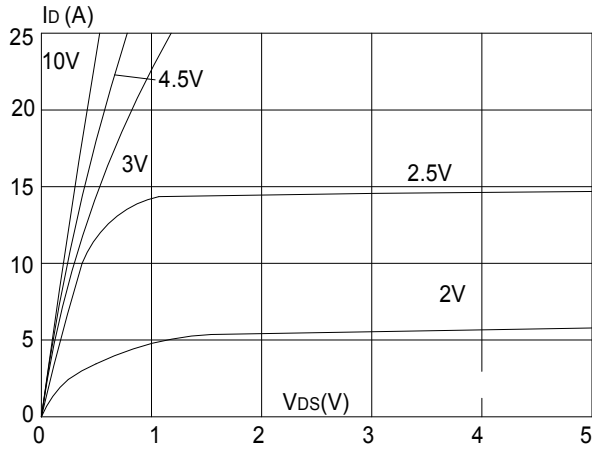


Figure 2: Typical Transfer Characteristics

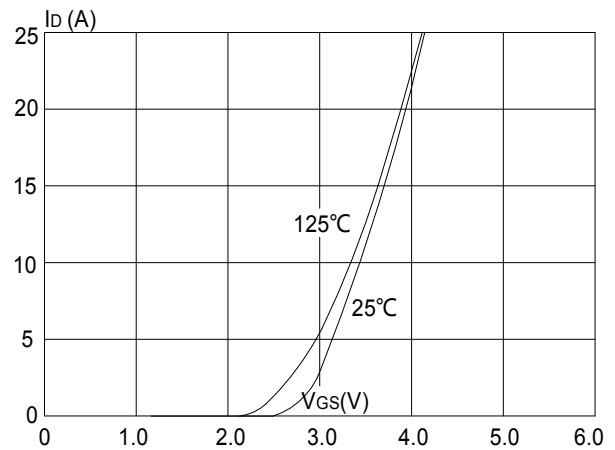


Figure 3: On-resistance vs. Drain Current

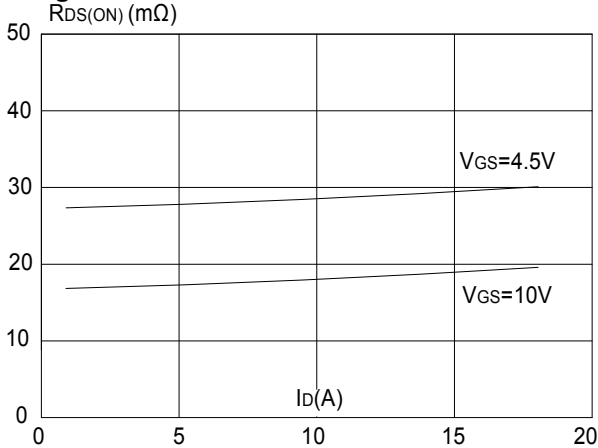


Figure 4: Body Diode Characteristics

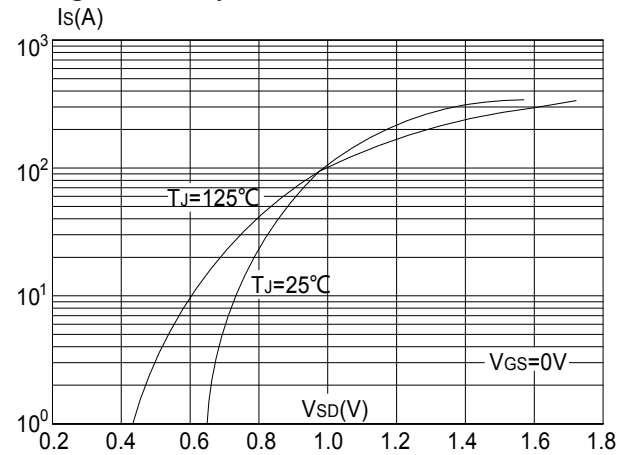


Figure 5: Gate Charge Characteristics

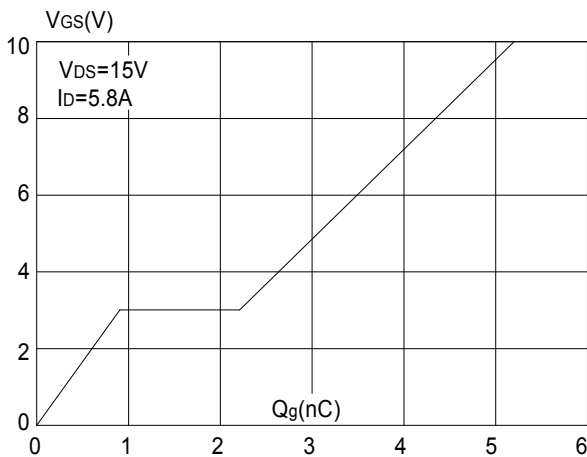


Figure 6: Capacitance Characteristics

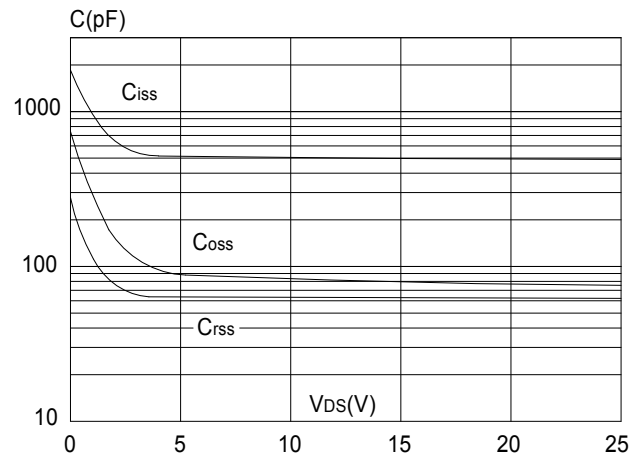




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

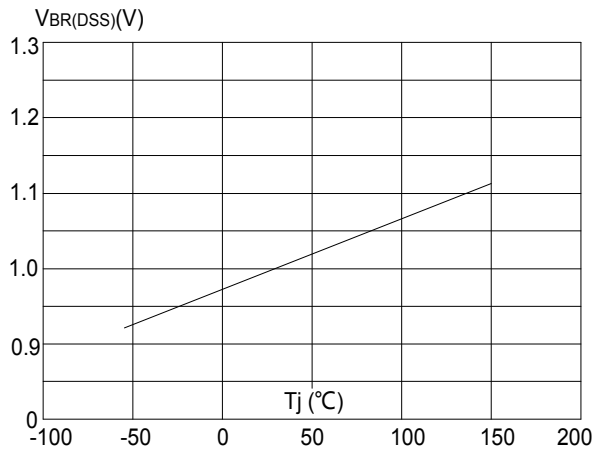


Figure 8: Normalized on Resistance vs. Junction Temperature

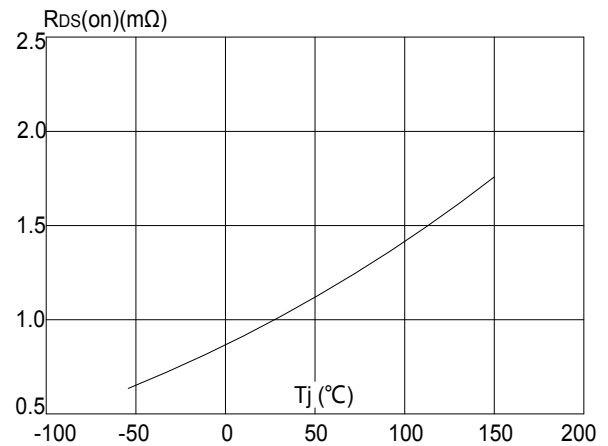


Figure 9: Maximum Safe Operating Area

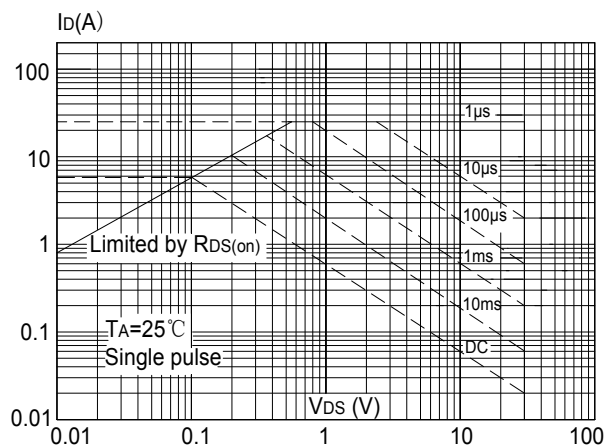


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

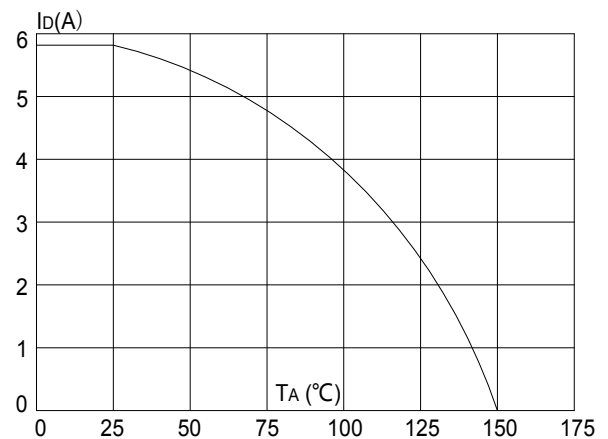
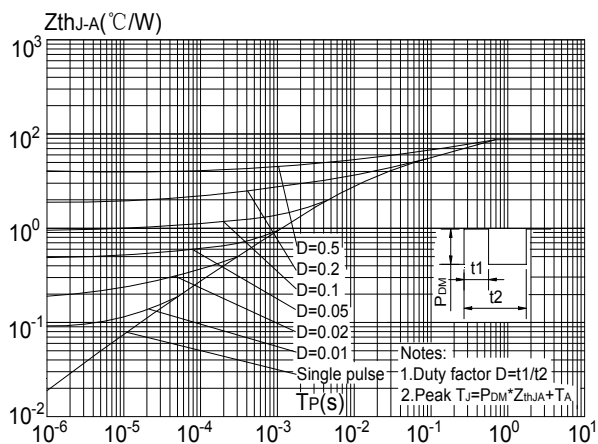


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient





P-Typical Characteristics

Figure1: Output Characteristics

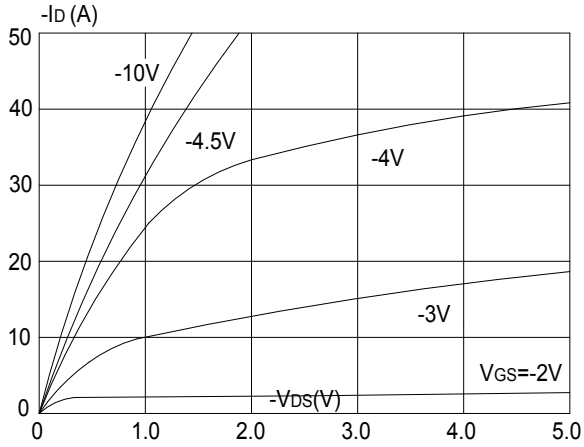


Figure 2: Typical Transfer Characteristics

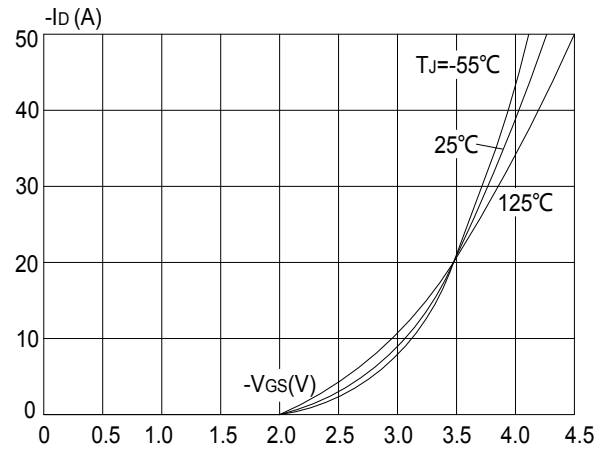


Figure 3: On-resistance vs. Drain Current

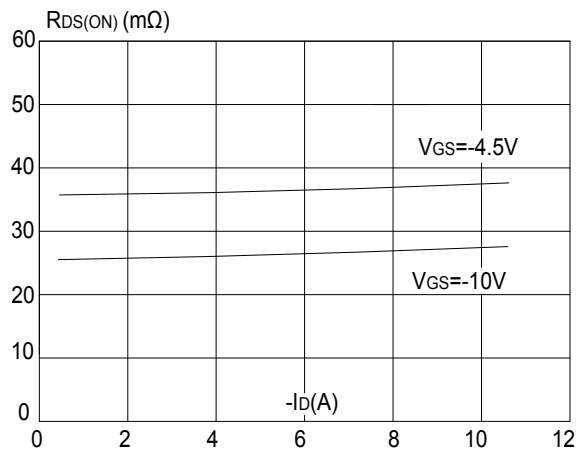


Figure 4: Body Diode Characteristics

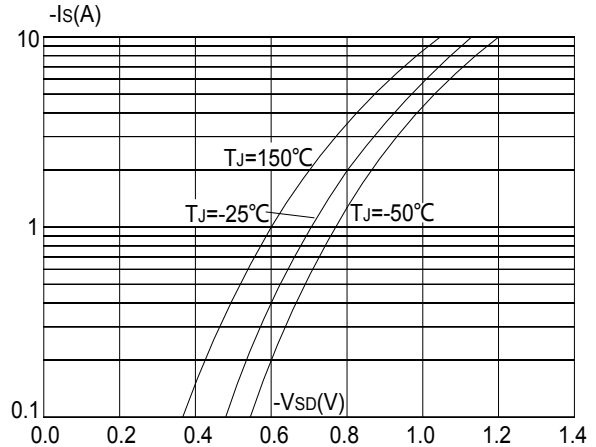


Figure 5: Gate Charge Characteristics

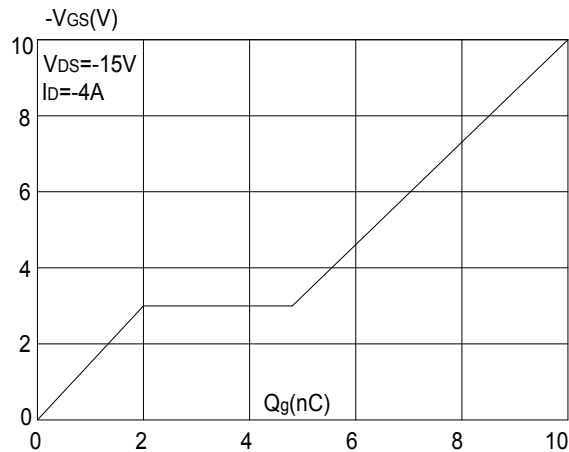


Figure 6: Capacitance Characteristics

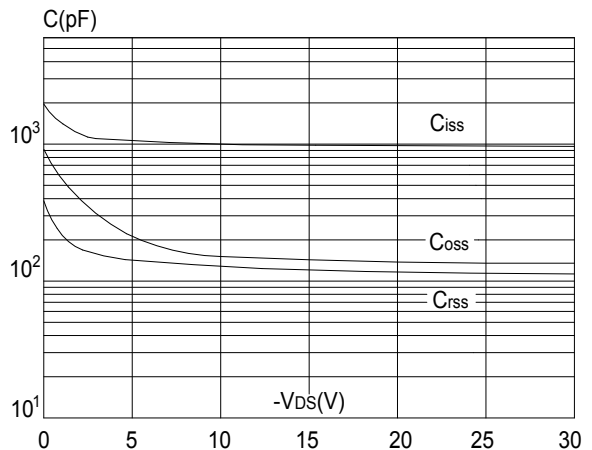




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

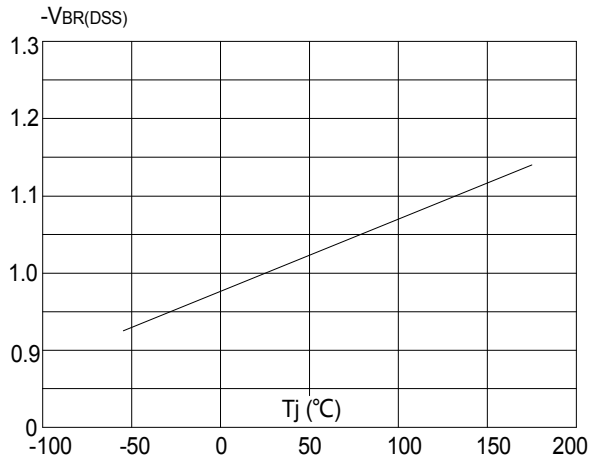


Figure 8: Normalized on Resistance vs. Junction Temperature

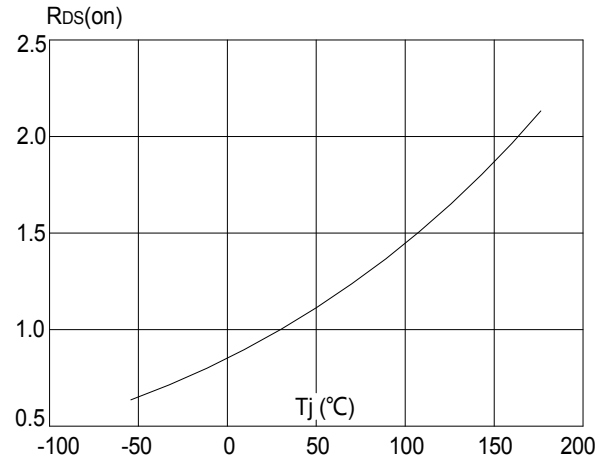


Figure 9: Maximum Safe Operating Area

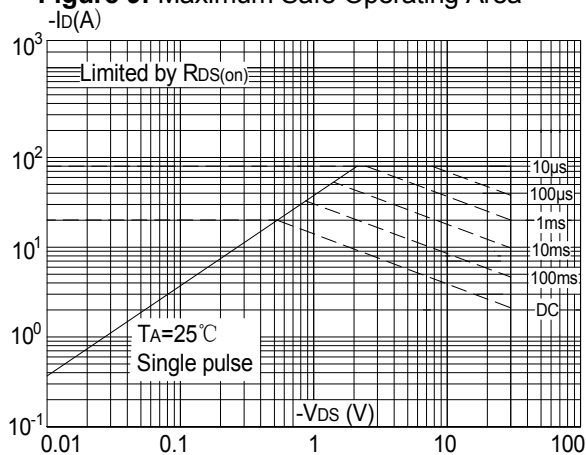


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

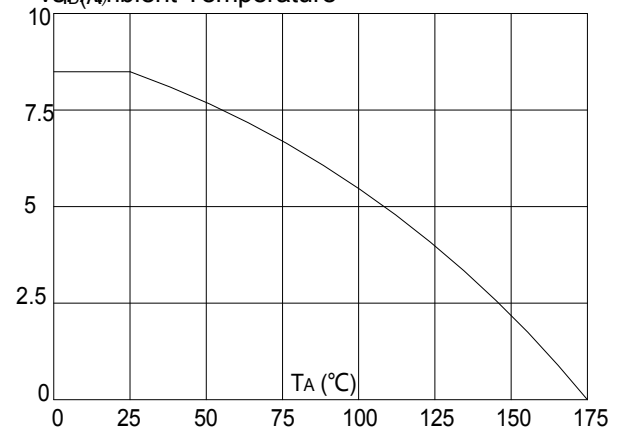
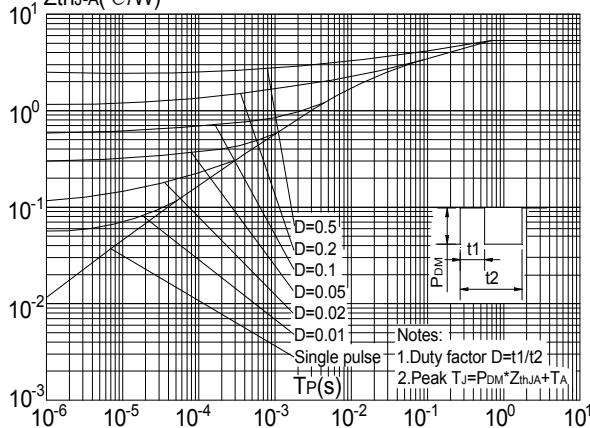
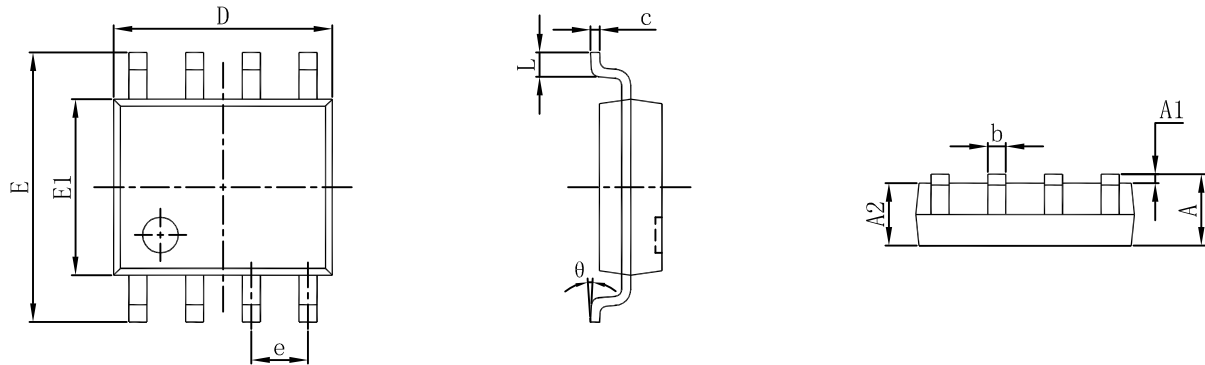


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

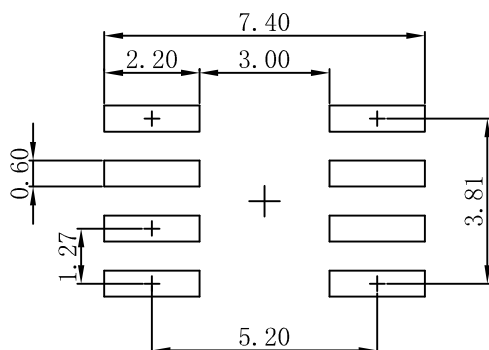




SOP-8(SOIC-8) Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:
1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.



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