300V N-Channel Enhancement Mode MOSFET

Description

The SX100N30MP is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

General Features

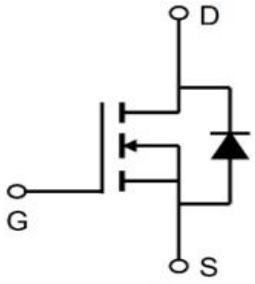
V_{DS} = 300V I_D =100A

$R_{DS(ON)}$ < 50mΩ @ V_{GS}=10V

Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



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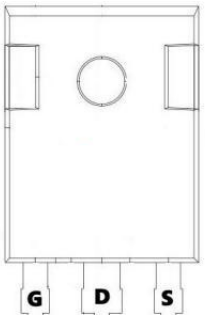


Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Value	Unit
VDSS	Drain-Source Voltage (V_{GS} = 0V)	300	V
ID	Continuous Drain Current	100	A
IDM	Pulsed Drain Current	300	A
VGSS	Gate-Source Voltage	±30	V
EAS	Single Pulse Avalanche Energy	3000	mJ
IAS	Avalanche Current	80	A
EAR	Repetitive Avalanche Energy	525	mJ
P_D	Power Dissipation (T_C = 25ºC)	800	W
TJ, Tstg	Operating Junction and Storage Temperature Range	-55~+150	ºC
RthJC	Thermal Resistance, Junction-to-Case	0.15	ºC/W
RthJA	Thermal Resistance, Junction-to-Ambient	40	ºC/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	VGS = 0V, ID = 250μA	300	330	--	V
IDSS	Zero Gate Voltage Drain Current	VDS= 300V, VGS = 0V, TJ = 25ºC	--	--	1	μA
IGSS	Gate-Source Leakage	VGS = ±30V，VDS = 0V	--	--	±100	nA
VGS(th)	Gate-Source Threshold Voltage	VDS = VGS, ID = 250μA	2.0	3.1	4.0	V
RDS(on)	Drain-Source On-Resistance	VGS = 10V, ID = 30A	--	44	50	mΩ
Ciss	Input Capacitance	VGS = 0V, VDS= 25V, f = 1.0MHz	--	19100	--	pF
Coss	Output Capacitance		--	1760	--	
Crss	Reverse Transfer Capacitance		--	490	--	
RG	Gate resistance	f=1.0MHz open drain	--	0.88	--	Ω
Qg	Total Gate Charge	VDD=240V, ID = 90A, VGS =10V	--	660	--	nC
Qgs	Gate-Source Charge		--	107	--	
Qgd	Gate-Drain Charge		--	364	--	
td(on)	Turn-on Delay Time	VDD=150V, ID=90A, RG=25Ω	--	40	--	ns
tr	Turn-on Rise Time		--	180	--	
td(off)	Turn-off Delay Time		--	174	--	
tf	Turn-off Fall Time		--	67	--	
trr	Reverse Recovery Time	VDD = 150V,IF = 30A, diF/dt =100A /μs	--	485	--	ns
Qrr	Reverse Recovery Charge		--	10	--	μC
ISD	Continuous Source Current	TC = 25 ºC	--	--	100	A
ISM	Pulsed Source Current		--	--	300	A
VSD	Body Forward Voltage	IS=30A, VGS = 0V	--	--	1.4	V

Note：

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The EAS data shows Max. rating . IAS = 80A, VDD = 50V, RG = 25 Ω, Starting TJ = 25 ºC

3、The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

4、The power dissipation is limited by 150℃junction temperature

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

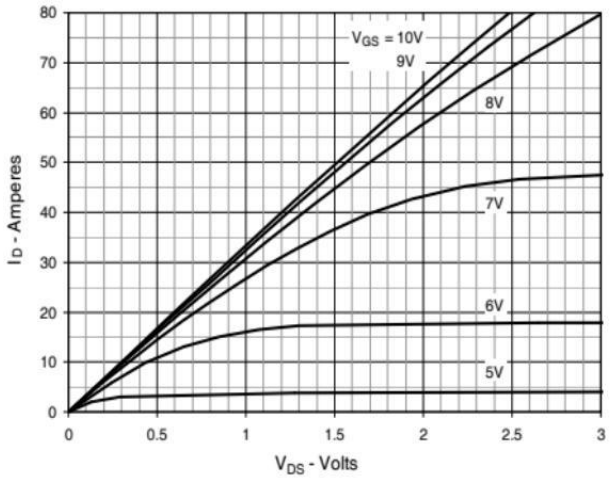


Figure 1. Output Characteristics

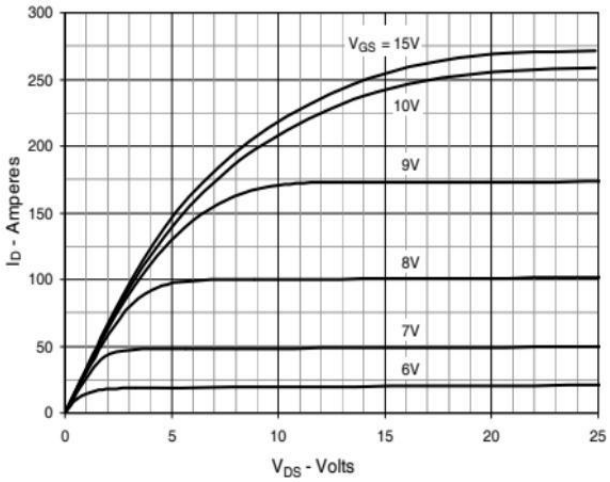


Figure 2. Extended Output Characteristics

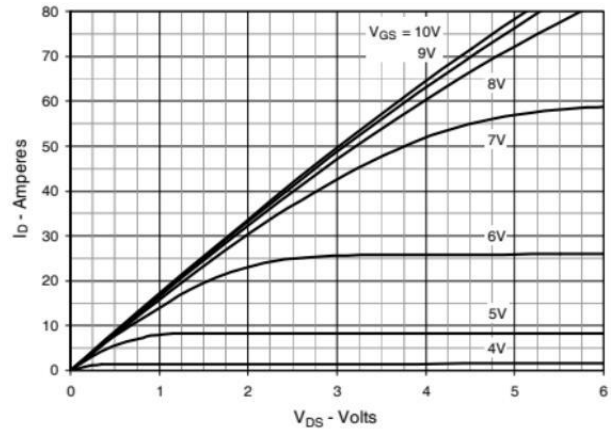


Figure3. Output Characteristics

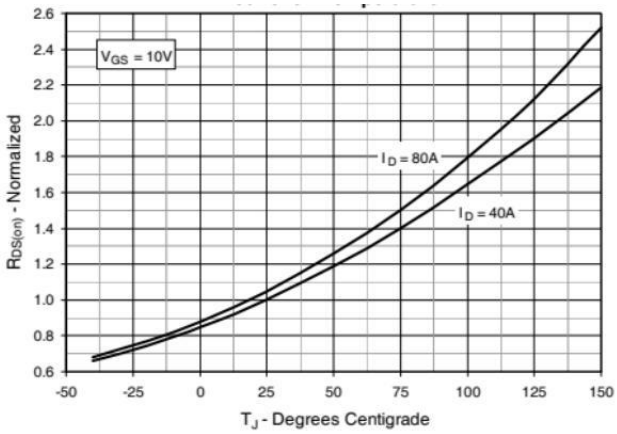


Figure4. RDS(on) Normalized to ID = 40A Valuevs.Junction TemperatureFigure

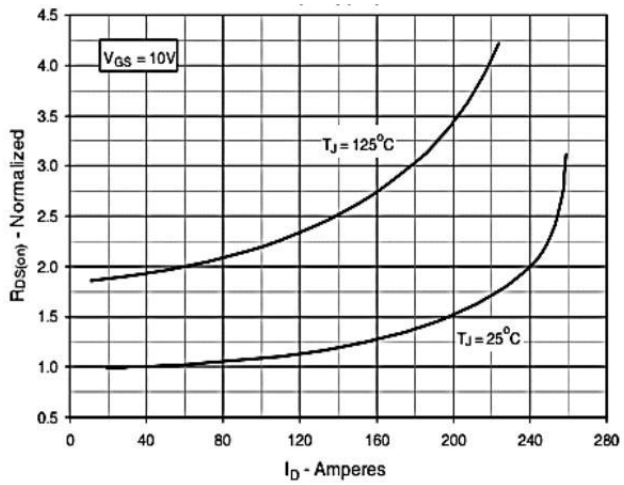


Figure5.RDS(on) Normalized to ID=40A Valuevs. Drain Curren

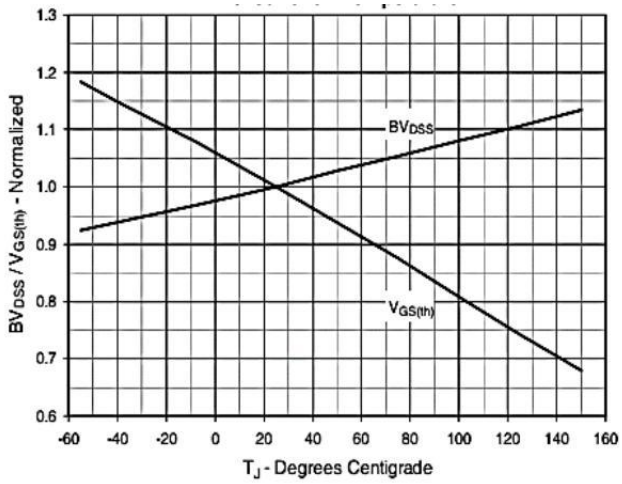


Figure 6. Normalized Breakdown & Threshold Voltagesvs. Junction Temperature

Typical Characteristics

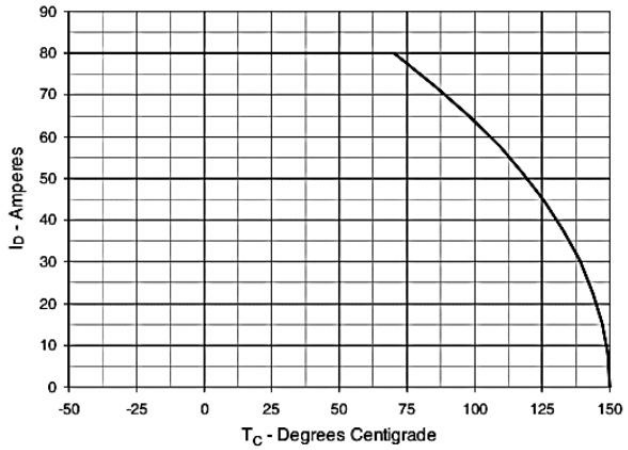


Figure7：Transconductance

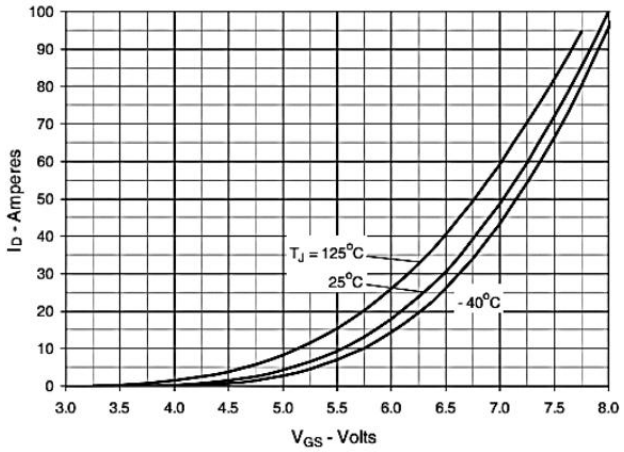


Figure8： Forward Voltage Drop of Intrinsic Diode

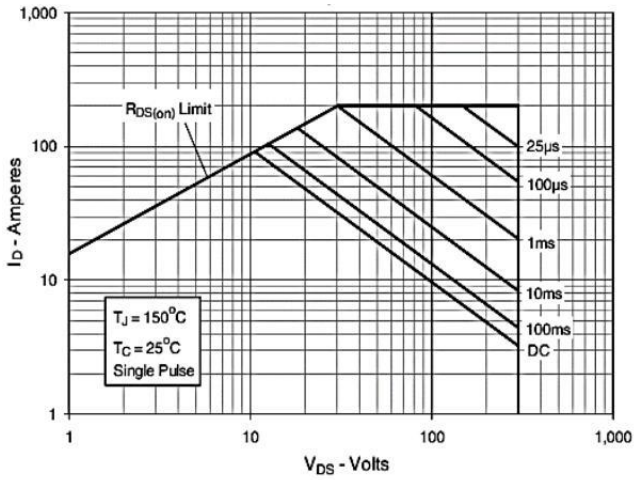


Figure9： Forward-Bias Safe Operating Area

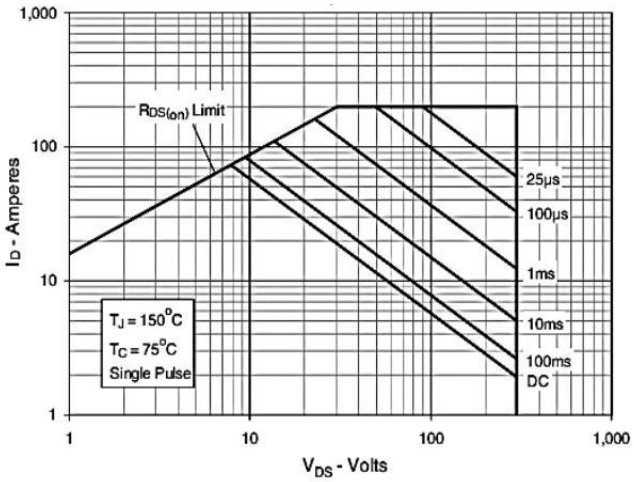


Figure10 Forward-Bias Safe Operating Area

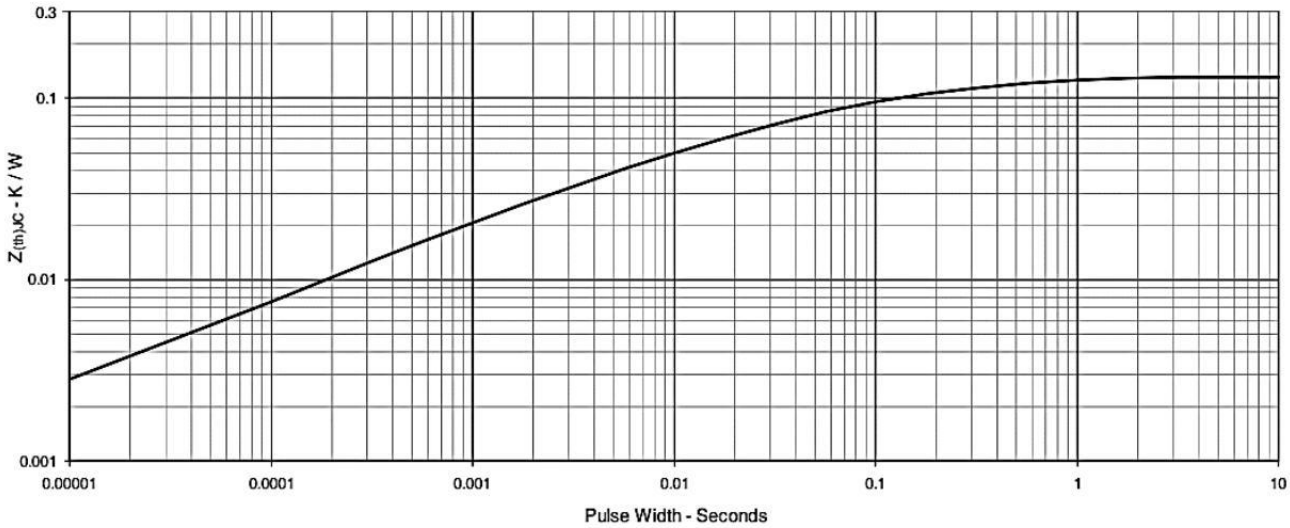
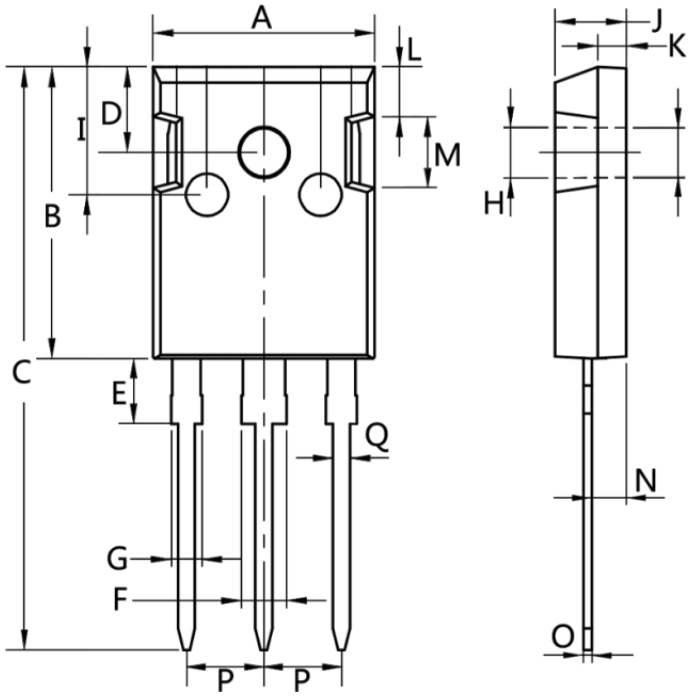


Figure11： Maximum Transient Thermal Impedance

Package Mechanical Data-TO-247-3L



Dim.	Min.	Max.
A	15.0	16. 0
B	20.0	21.0
C	41.0	42.0
D	5.0	6.0
E	4.0	5.0
F	2.5	3.5
G	1.75	2.5
H	3.0	3.5
I	8.0	10.0
J	4.9	5.1
K	1.9	2.1
L	3.5	4.0
M	4.75	5.25
N	2.0	3.0
O	0.55	0.75
P	Typ 5.08	
Q	1.2	1.3

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
TAPING	TO-247-3L		330