

MOSFET – N-Channel, SUPERFET® II

800 V, 10 A, 650 mΩ

FCPF650N80Z

Description

SUPERFET II MOSFET is onsemi's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. In addition, internal gate-source ESD diode allows to withstand over 2 kV HBM surge stress. Consequently, SUPERFET II MOSFET is very suitable for the switching power applications such as Audio, Laptop adapter, Lighting, ATX power and industrial power applications.

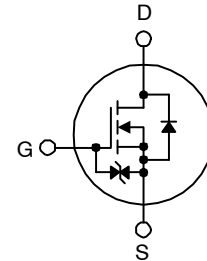
Features

- $R_{DS(on)} = 530 \text{ m}\Omega$ (Typ.)
- Ultra Low Gate Charge (Typ. $Q_g = 27 \text{ nC}$)
- Low E_{oss} (Typ. $2.8 \mu\text{J @ } 400 \text{ V}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 124 \text{ pF}$)
- 100% Avalanche Tested
- ESD Improved Capability
- RoHS Compliant

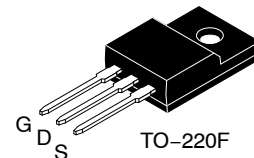
Applications

- AC-DC Power Supply
- LED Lighting

V_{DSS}	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
800 V	650 mΩ @ 10 V	10 A

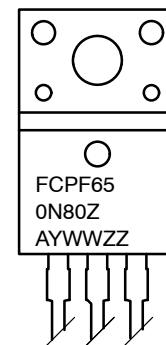


N-Channel MOSFET



TO-220 Fullpack, 3-Lead / TO-220F-3SG
CASE 221AT

MARKING DIAGRAM



FCPF650N80Z = Specific Device Code
A = Assembly Location
YWW = Date Code (Year & Work Week)
ZZ = Assembly Lot

ORDERING INFORMATION

Device	Package	Shipping
FCPF650N80Z	TO-220-3 (Pb-Free)	1000 Units / Tube

FCPF650N80Z

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter		FCPF650N80Z	Unit
V_{DSS}	Drain to Source Voltage		800	V
V_{GSS}	Gate to Source Voltage	– DC	± 20	V
		– AC ($f > 1\text{ Hz}$)	± 30	
I_D	Drain Current	– Continuous ($T_C = 25^\circ\text{C}$)	10*	A
		– Continuous ($T_C = 100^\circ\text{C}$)	6.3*	
I_{DM}	Drain Current	– Pulsed (Note 1)	24*	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		204	mJ
I_{AR}	Avalanche Current (Note 1)		1.6	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		0.305	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	30.5	W
		– Derate above 25°C	0.24	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*Drain current limited by maximum junction temperature.

1. Repetitive rating; pulse width limited by maximum junction temperature
2. $I_{AS} = 1.6\text{ A}$, $R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 10\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$

THERMAL CHARACTERISTICS

Symbol	Parameter	FCPF650N80Z	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	4.1	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

FCPF650N80Z

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	800	–	–	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C	–	0.8	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 800 V, V _{GS} = 0 V	–	–	25	μA
		V _{DS} = 640 V, V _{GS} = 0 V, T _C = 125°C	–	–	250	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	–	–	±10	μA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 0.8 mA	2.5	–	4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 4 A	–	530	650	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 4 A	–	7.8	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz	–	1178	1565	pF
C _{oss}	Output Capacitance		–	36	48	pF
C _{rss}	Reverse Transfer Capacitance		–	0.84	–	pF
C _{oss}	Output Capacitance	V _{DS} = 480 V, V _{GS} = 0 V, f = 1 MHz	–	18	–	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 480 V, V _{GS} = 0 V	–	124	–	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 640 V, I _D = 8 A, V _{GS} = 10 V (Note 4)	–	27	35	nC
Q _{gs}	Gate to Source Gate Charge		–	6	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	11	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	1.9	–	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 8 A, V _{GS} = 10 V, R _G = 4.7 Ω (Note 4)	–	17	44	ns
t _r	Turn-On Rise Time		–	11	32	ns
t _{d(off)}	Turn-Off Delay Time		–	40	90	ns
t _f	Turn-Off Fall Time		–	3.4	17	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

I _S	Maximum Continuous Drain to Source Diode Forward Current		–	–	10	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	24	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 8 A	–	–	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 8 A, dI _F / dt = 100 A/μs	–	365	–	ns
Q _{rr}	Reverse Recovery Charge		–	5.9	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics

TYPICAL PERFORMANCE CHARACTERISTICS

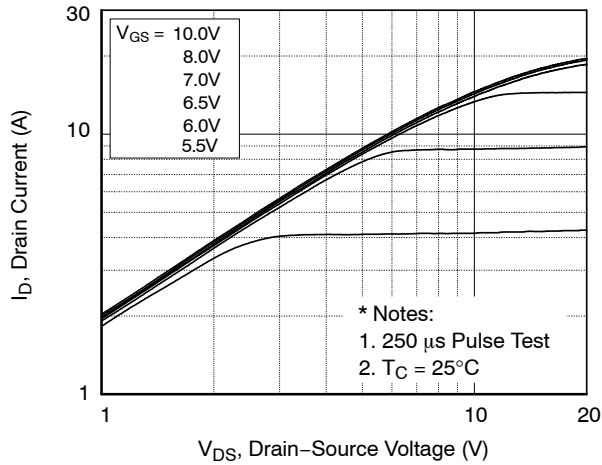


Figure 1. On-Region Characteristics

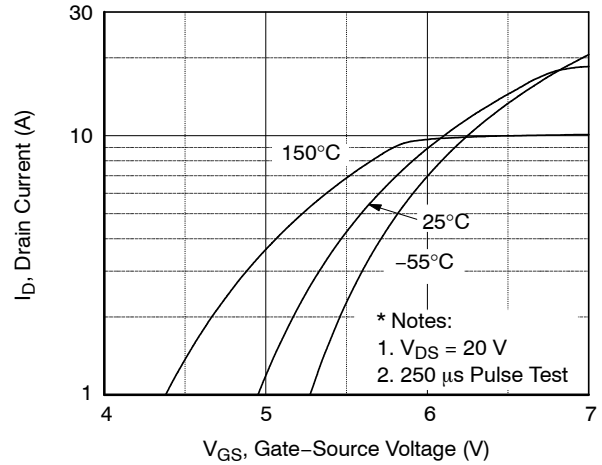


Figure 2. Transfer Characteristics

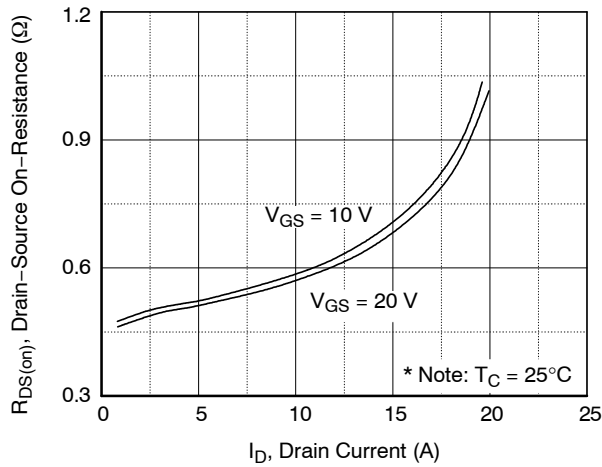


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

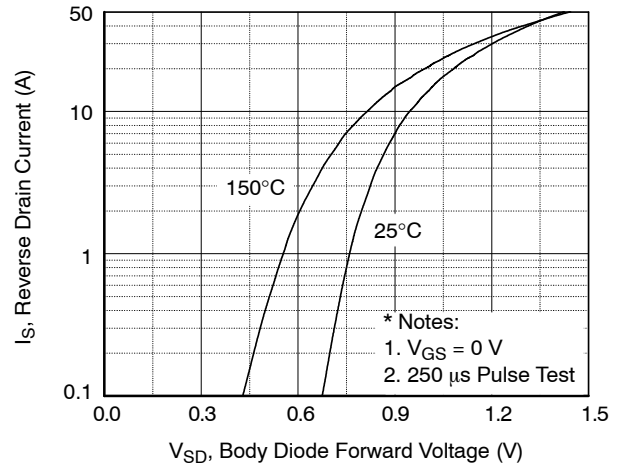


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

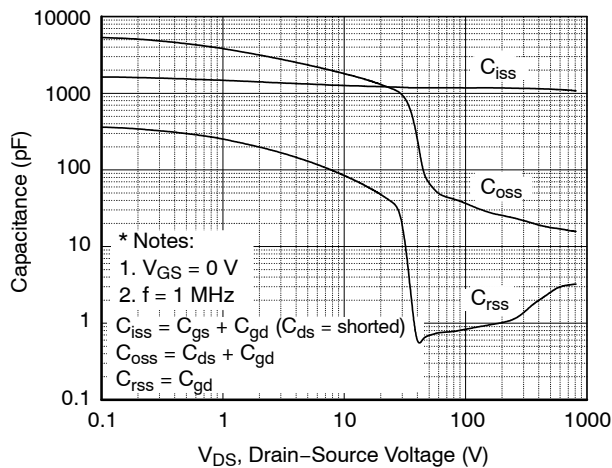


Figure 5. Capacitance Characteristics

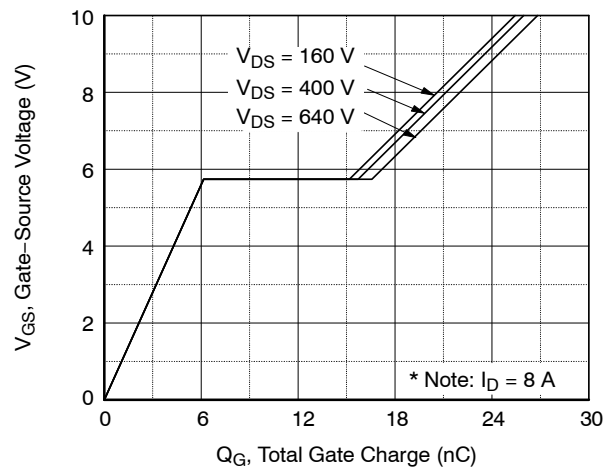


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

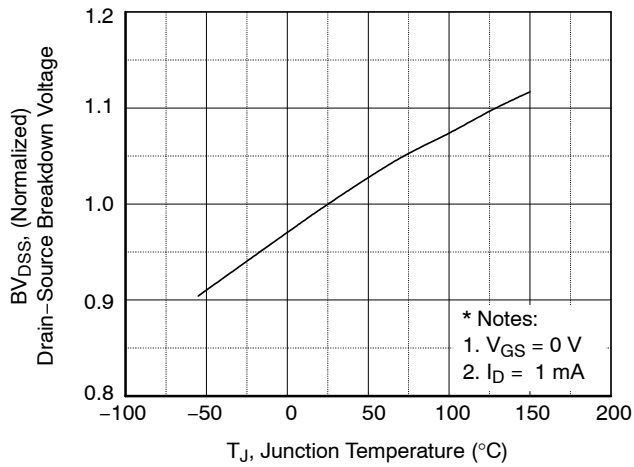


Figure 7. Breakdown Voltage Variation vs. Temperature

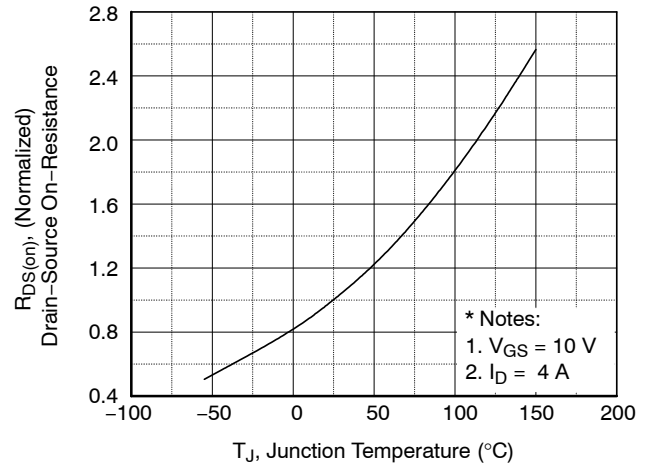


Figure 8. On-Resistance Variation vs. Temperature

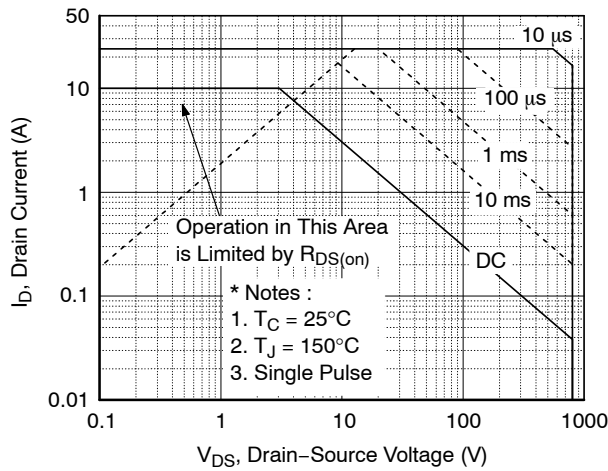


Figure 9. Maximum Safe Operating Area

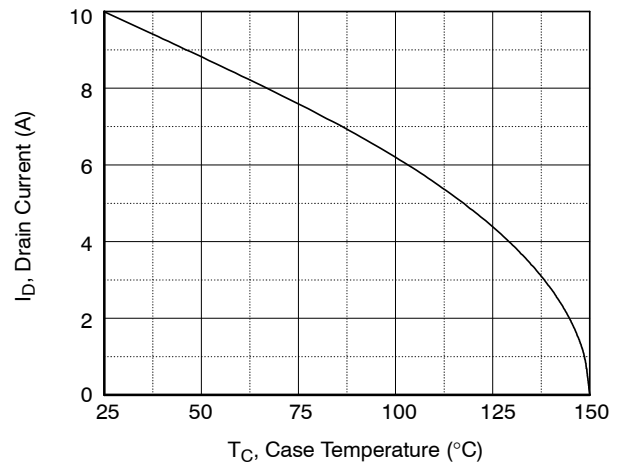


Figure 10. Maximum Drain Current vs. Case Temperature

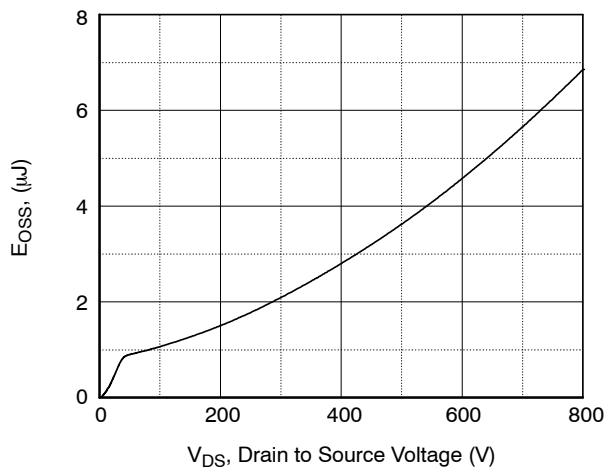


Figure 11. E_{OSS} vs. Drain to Source Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

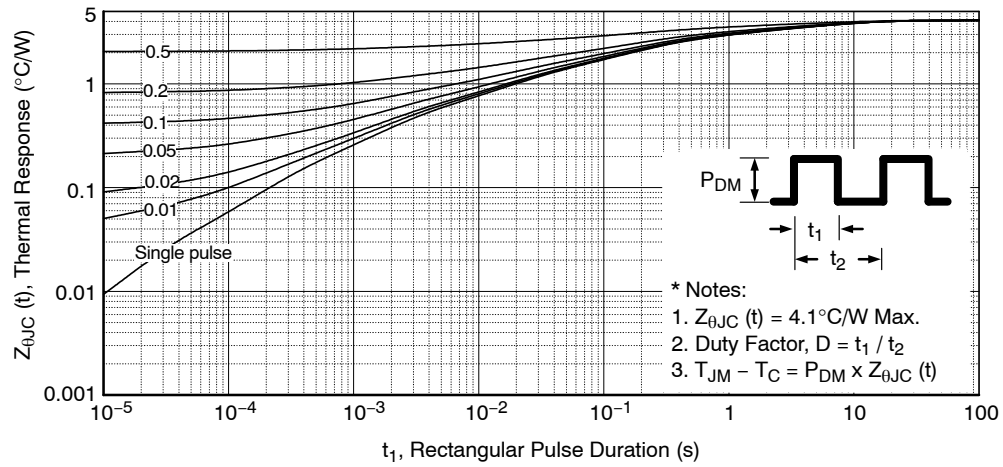


Figure 12. Transient Thermal Response Curve

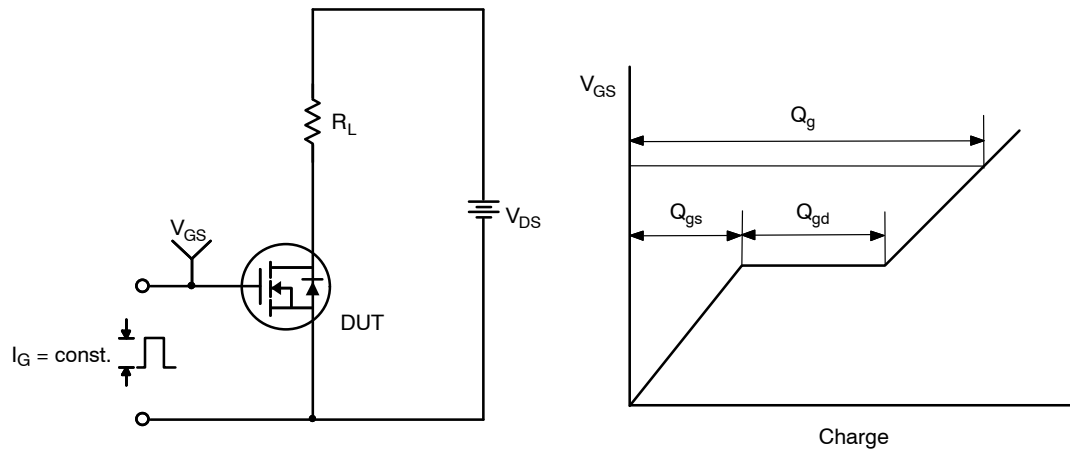


Figure 13. Gate Charge Test Circuit & Waveform

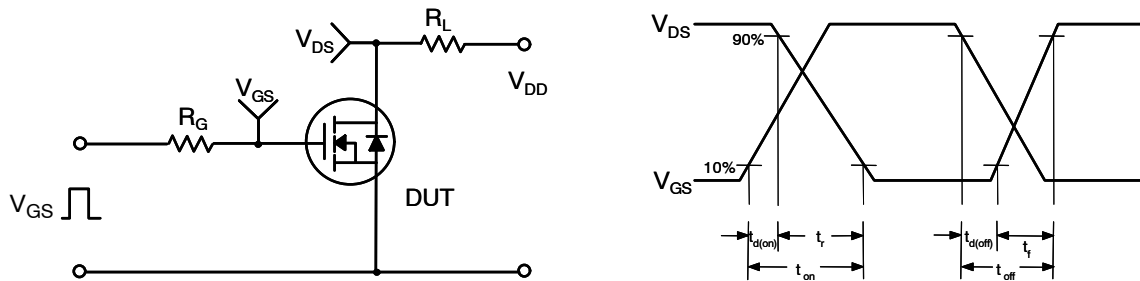


Figure 14. Resistive Switching Test Circuit & Waveforms

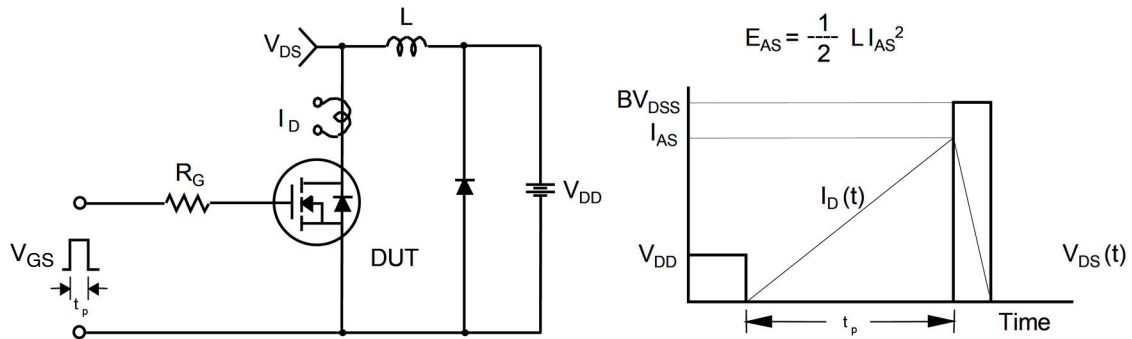


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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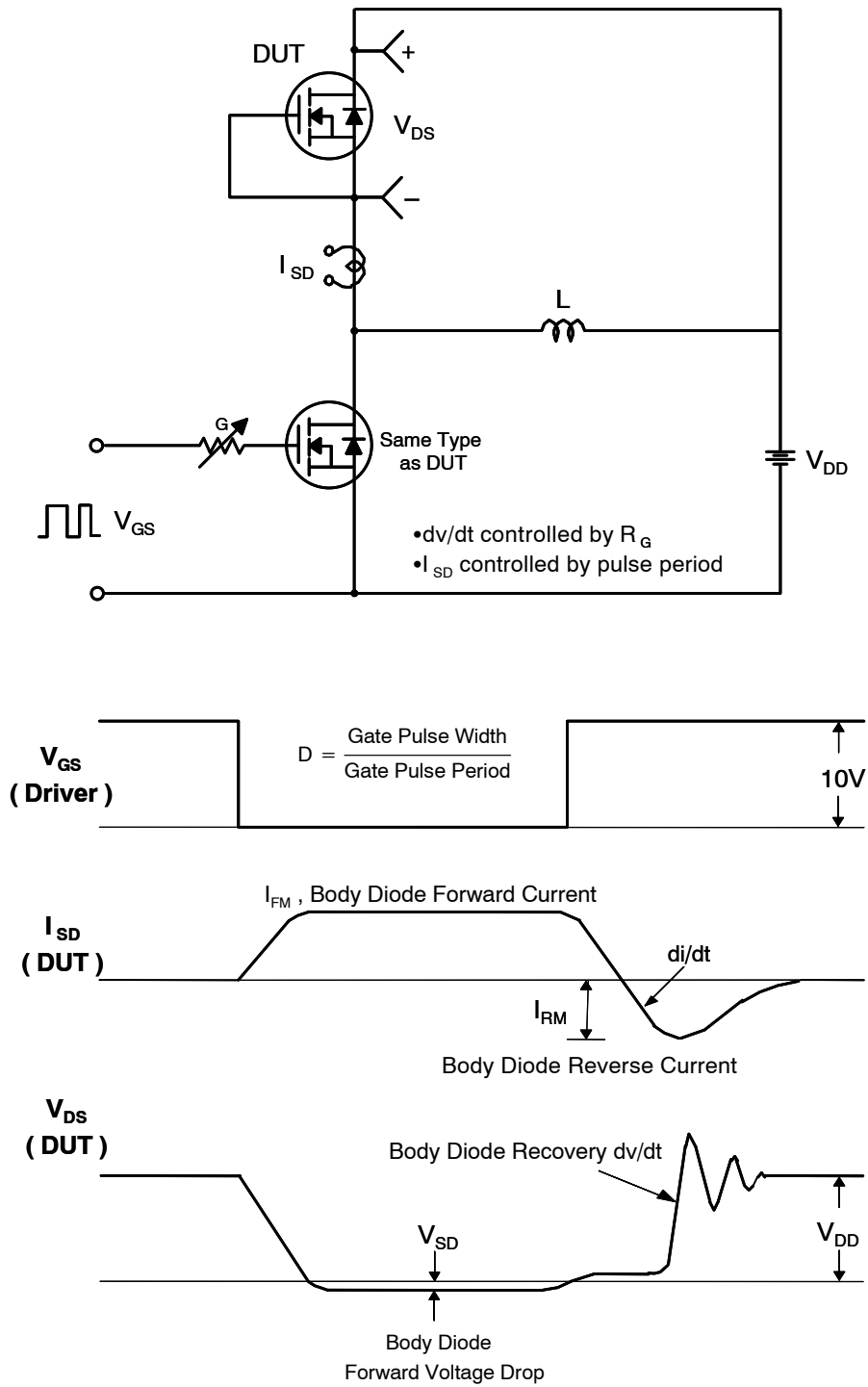


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

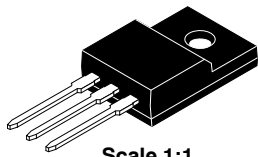
ON

TO-220 Fullpack, 3-Lead / TO-220F-3SG

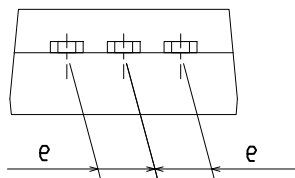
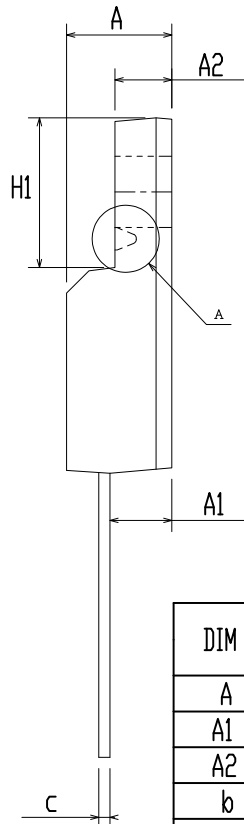
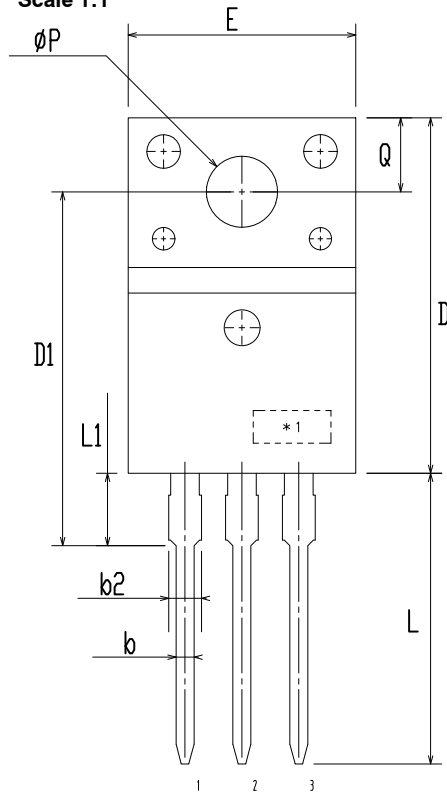
CASE 221AT

ISSUE B

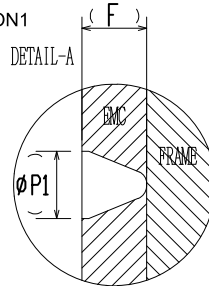
DATE 19 JAN 2021



Scale 1:1



OPTION1



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.56	2.76	2.96
A2	2.34	2.54	2.74
b	0.70	0.80	0.90
b2	~	~	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.60	15.80	16.00
E	9.96	10.16	10.36
e	2.34	2.54	2.74
F	~	0.84	~
H1	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
Ø P	2.98	3.18	3.38
Ø P1	~	1.00	~
Q	3.20	3.30	3.40

NOTES:

A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009

B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCTIONS.

C. OPTION 1 - WITH SUPPORT PIN HOLE

OPTION 2 - NO SUPPORT PIN HOLE

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