Description

The SX50N02DF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

V_{DS} = 20V I_D =53A

$R_{DS(ON)}$ < 8.5mΩ @ V_{GS}=4.5V

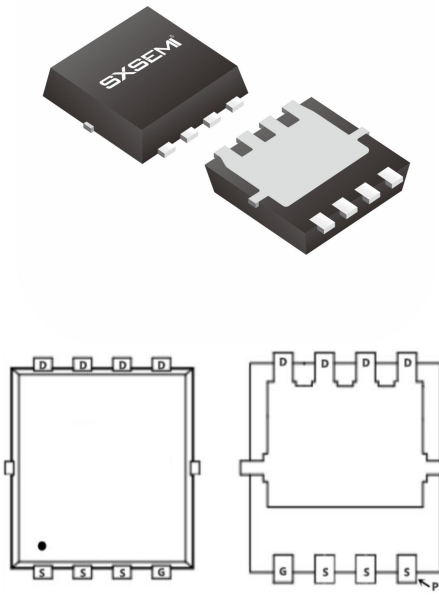
Application

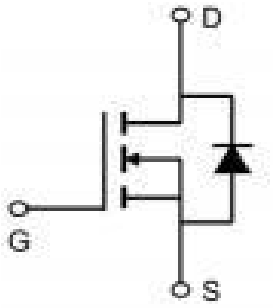
3.3V MCU Drive

Load switch

Uninterruptible power supply

PDFN3*3-8L





Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Max.	Units
VDSS	Drain-Source Voltage	20	V
VGSS	Gate-Source Voltage	±12	V
ID@TA=25℃	Continuous Drain Current, VGS @ 4.5V	50	A
ID@TA=70℃	Continuous Drain Current, VGS @ 4.5V	30	A
IDM	Pulsed Drain Current note1	120	A
EAS	Single Pulsed Avalanche Energy note2	147.6	mJ
PD@TA=25℃	Power Dissipation	37	W
TJ, TSTG	Operating and Storage Temperature Range	-55 to +175	℃
RθJA	Thermal Resistance Junction-Ambient 1	62	℃/W
RθJC	Thermal Resistance, Junction to Case	4	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	20	24	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS}=20V, V_{GS}=0V,	-	-	1.0	μA
IGSS	Gate to Body Leakage Current	V_{DS}=0V, V_{GS}=±12V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	0.4	0.7	1.1	V
RDS(on)	Static Drain-Source on-Resistance note3	V_{GS}=4.5V, I_D=25A	-	6.2	8.5	mΩ
		V_{GS}=2.5V, I_D=10A	-	8.8	13	
C_{iss}	Input Capacitance	V_{DS}=10V, V_{GS}=0V, f=1.0MHz	-	1458	-	pF
Coss	Output Capacitance		-	238	-	pF
Crss	Reverse Transfer Capacitance		-	212	-	pF
Q_g	Total Gate Charge	V_{DS}=10V, I_D=25A, V_{GS}=4.5V	-	19	-	nC
Q_{gs}	Gate-Source Charge		-	3	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	6.4	-	nC
td(on)	Turn-on Delay Time	V_{DS}=10V, I_D=10A, R_{GEN}=3Ω, V_{GS}=4.5V	-	10	-	ns
t_r	Turn-on Rise Time		-	21	-	ns
td(off)	Turn-off Delay Time		-	39	-	ns
t_f	Turn-off Fall Time		-	19	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	50	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	200	A
VSD	Drain to Source Diode Forward Voltage	V_{GS}=0V, I_S=30A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	IF=20A,dI/dt=100A/μs	-	25	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	20	-	nC

Note :

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%

3、The test condition is T_J=25℃, V_{DD}=10V, V_G=4.5V, L=0.5mH, R_G=25Ω, I_{AS}=12A

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

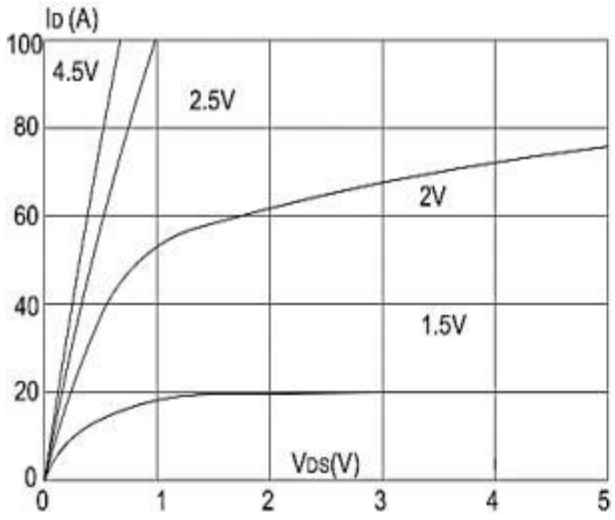


Figure1: Output Characteristics

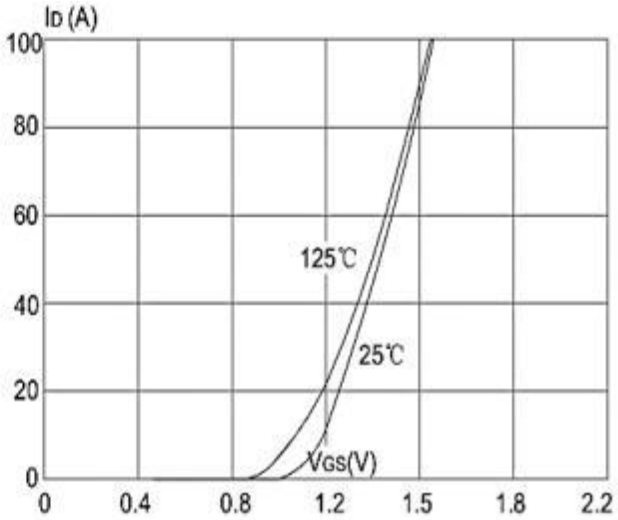


Figure 2: Typical Transfer Characteristics

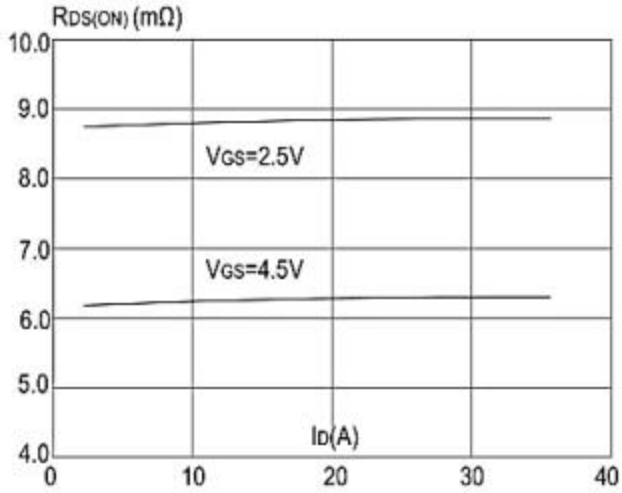


Figure 3:On-resistance vs. Drain Current

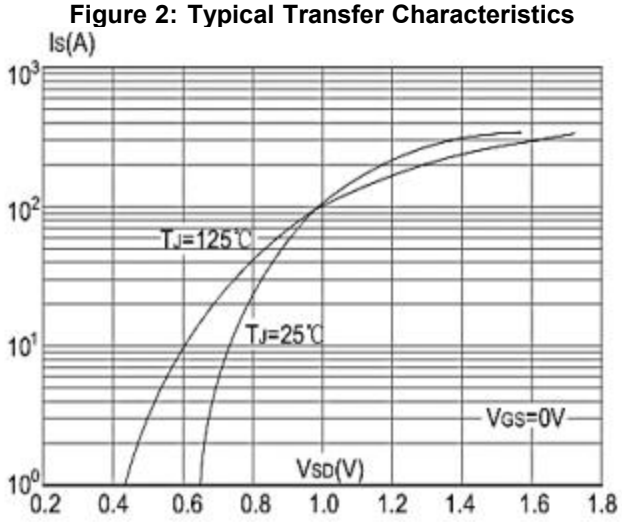


Figure 4: Body Diode Characteristics

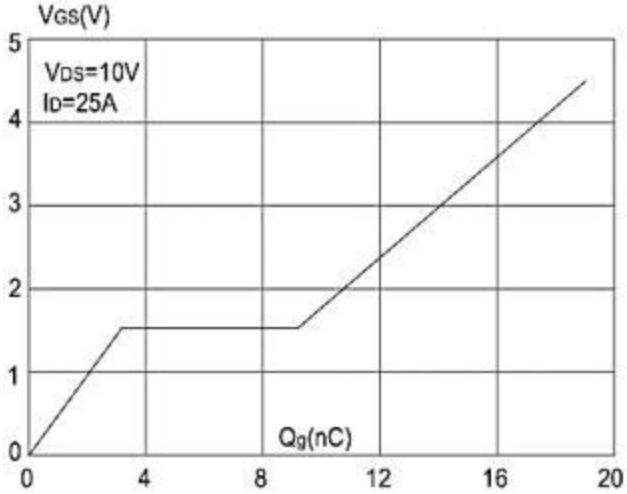


Figure 5: Gate Charge Characteristics

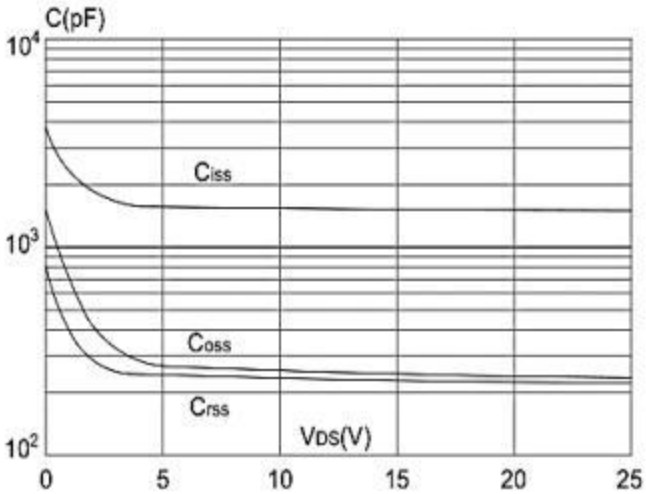


Figure 6: Capacitance Characteristics

Typical Characteristics

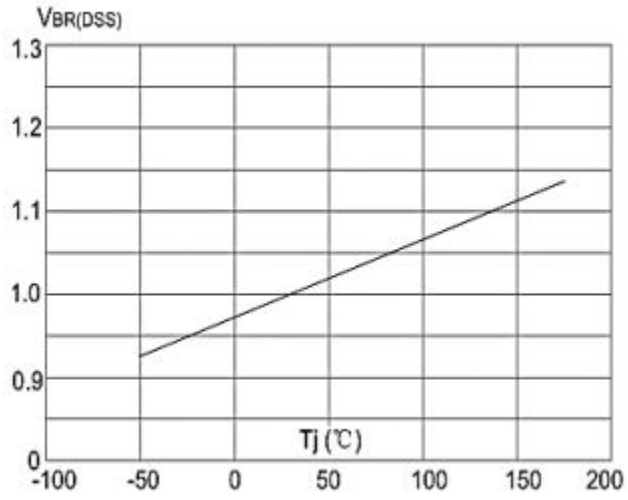


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

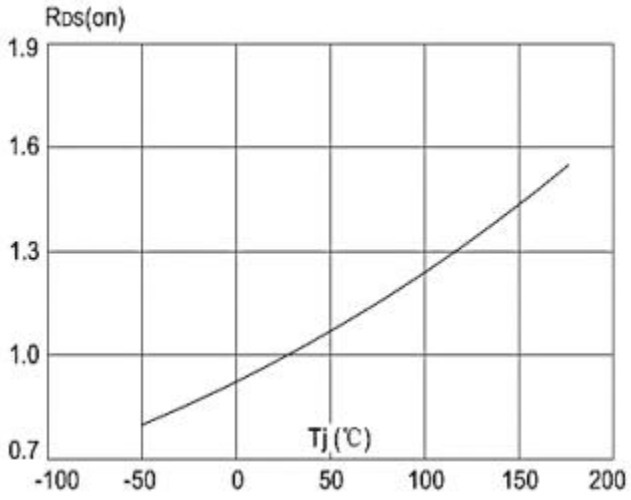


Figure 8: Normalized on Resistance vs Junction Temperature

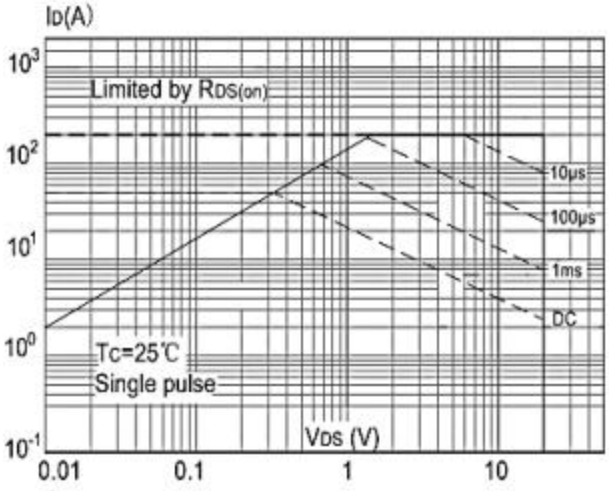


Figure 9: Maximum Safe Operating Area vs. Case Temperature

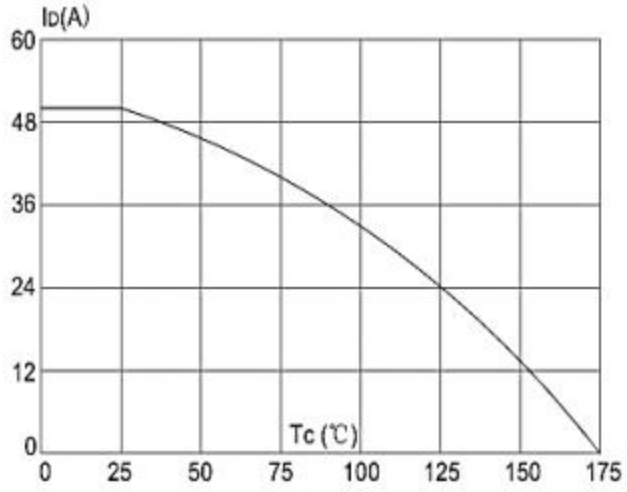


Figure 10: Maximum Continuous Drain Current

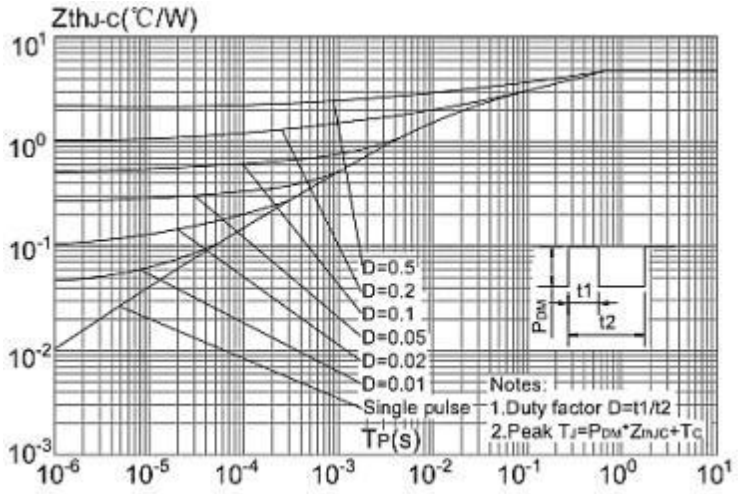
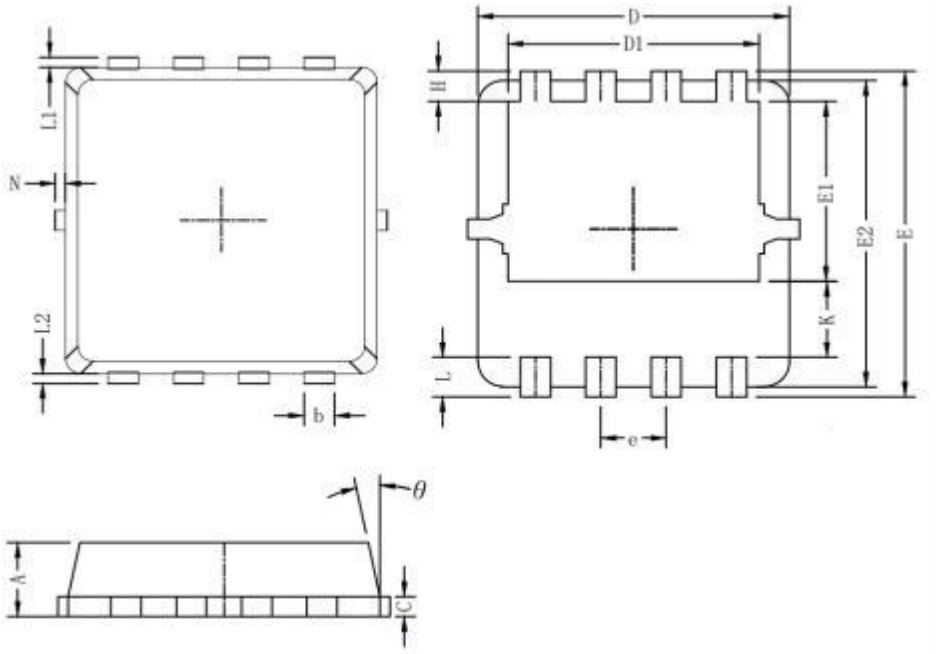


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

Package Mechanical Data-PDFN3X3-8L



Symbol	Dim in mm		
	Min	Typ	Max
A	0.6	0.75	0.9
b	0.2	0.3	0.4
C	0.15	0.2	0.25
D	3	3.1	3.2
D1	2.3	2.45	2.6
E	3.15	3.3	3.45
E1	1.43	1.73	1.93
E2	2.9	3.05	3.2
e		0.65BSC	
H	0.2	0.35	0.5
K	0.57	0.77	0.87
L	0.3	0.4	0.5
L1/L2		0.1REF	
θ	8°	10°	13°
N	0		0.15

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
TAPING	PDFN3*3-8L		5000