

N-Channel 80 V (D-S) Super Trench Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	80
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.010
$R_{DS(on)}$ (Ω) at $V_{GS} = 6$ V	0.012
I_D (A)	12
Configuration	Single

FEATURES

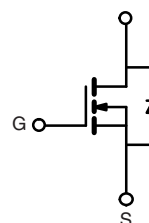
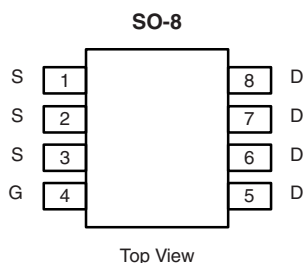
- Super Trench technology Power MOSFET
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 100 % R_g and UIS Tested

APPLICATIONS

- DC/DC Converter
- Ideal for high-frequency switching and synchronous



RoHS
COMPLIANT
HALOGEN
FREE



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	I_D	12	A
		7	
Continuous Source Current (Diode Conduction)	I_S	6	
Pulsed Drain Current ^a	I_{DM}	67	
Single Pulse Avalanche Current	I_{AS}	50	
Single Pulse Avalanche Energy	E_{AS}	125	mJ
Maximum Power Dissipation ^a	P_D	7.1	W
		2.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R_{thJA}	80	$^\circ\text{C/W}$
Junction-to-Foot (Drain)	R_{thJF}	21	

Notes

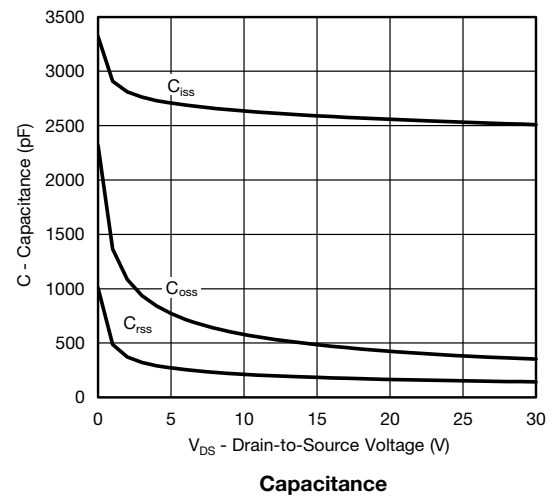
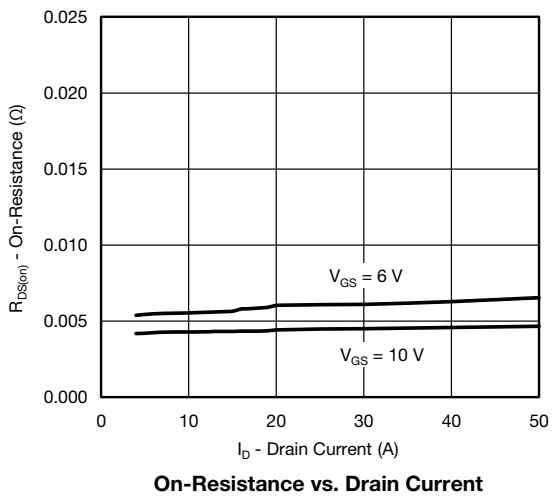
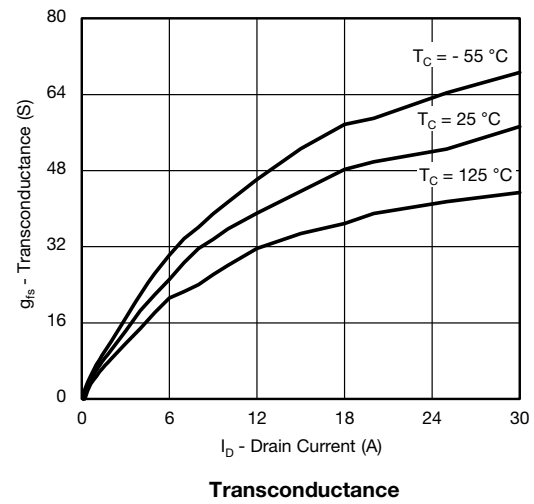
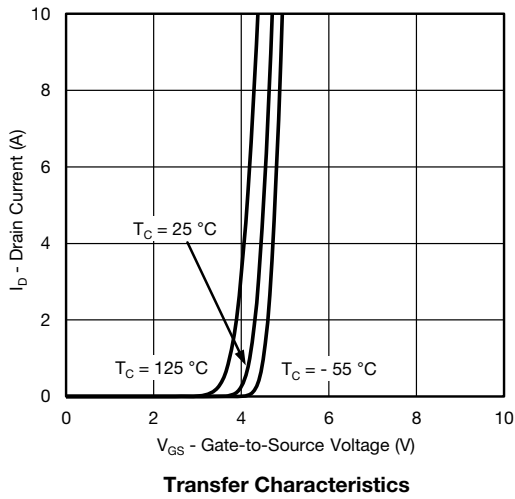
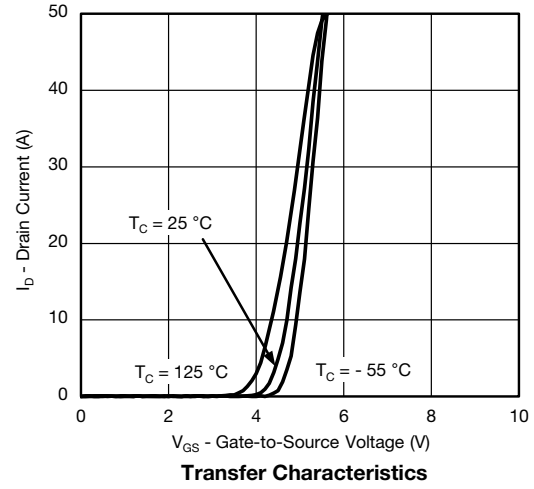
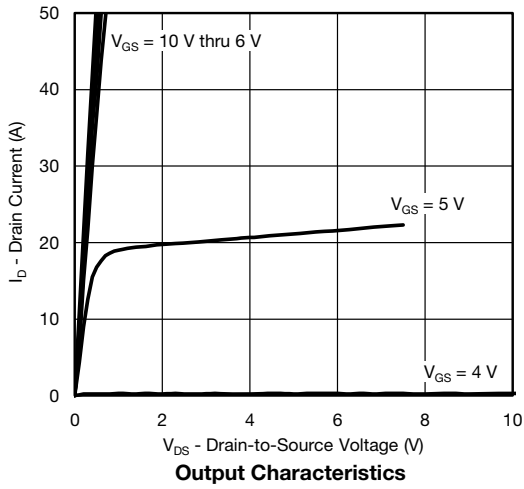
- Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- When mounted on 1" square PCB (FR-4 material).
- Parametric verification ongoing.

SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		80	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.5	3.0	3.5	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 60 V	-	-	1.0	μA
		V _{GS} = 0 V	V _{DS} = 80 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 80 V, T _J = 175 °C	-	-	250	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	30	-	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 6 A	-	0.010	-	Ω
		V _{GS} = 10 V	I _D = 6 A, T _J = 125 °C	--	0.015	-	
		V _{GS} = 10 V	I _D = 6 A, T _J = 175 °C	--	0.020	-	
		V _{GS} = 6 V	I _D = 5 A	-	0.012	-	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 6 A		-	25	-	S
Dynamic ^b							
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	-	2531	3165	pF
Output Capacitance	C _{oss}			-	382	480	
Reverse Transfer Capacitance	C _{rss}			-	153	195	
Total Gate Charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 30 V, I _D = 12 A	-	45	68	nC
Gate-Source Charge ^c	Q _{gs}			-	9.9	-	
Gate-Drain Charge ^c	Q _{gd}			-	11.2	-	
Gate Resistance	R _g	f = 1 MHz		0.40	0.87	1.30	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 30 V, R _L = 2.5 Ω I _D ≅ 12 A, V _{GEN} = 10 V, R _g = 1 Ω		-	13	20	ns
Rise Time ^c	t _r			-	12	18	
Turn-Off Delay Time ^c	t _{d(off)}			-	25	38	
Fall Time ^c	t _f			-	9	14	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I _{SM}			-	-	67	A
Forward Voltage	V _{SD}	I _F = 1.7 A, V _{GS} = 0		-	0.72	1.2	V

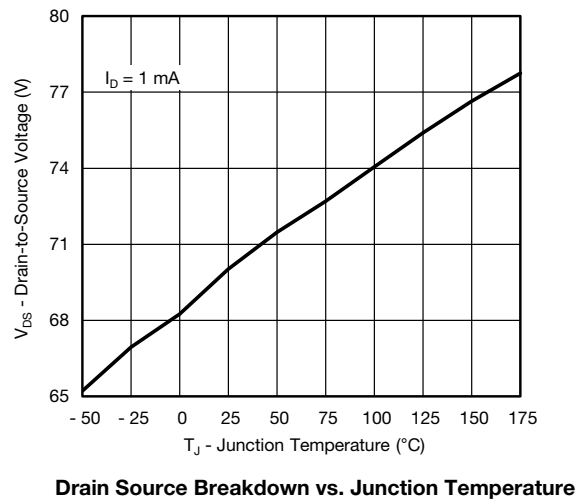
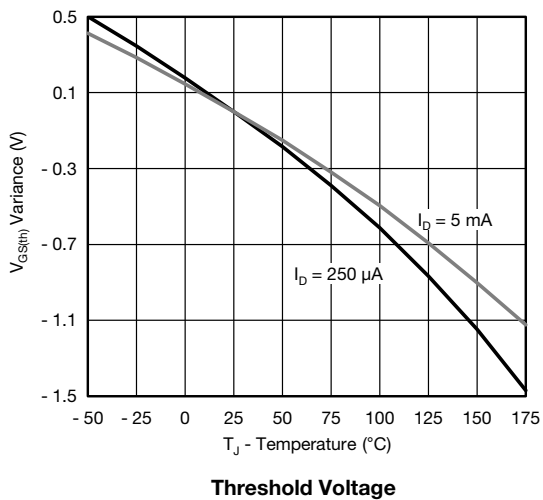
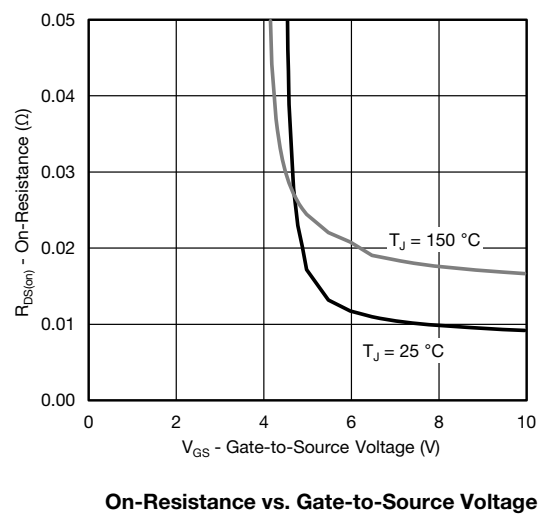
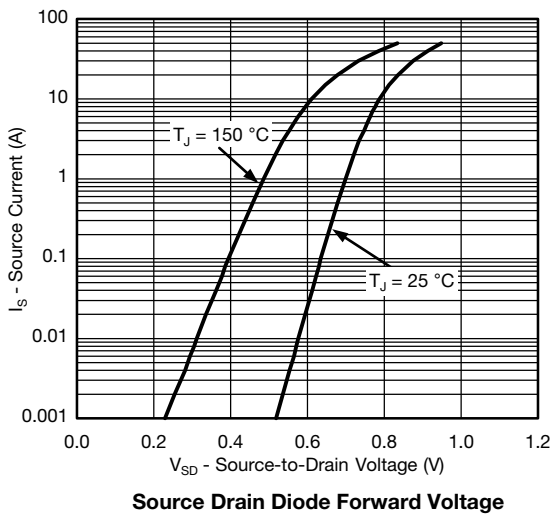
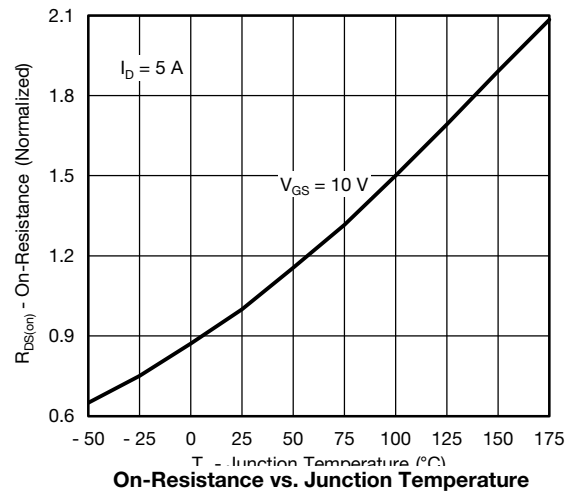
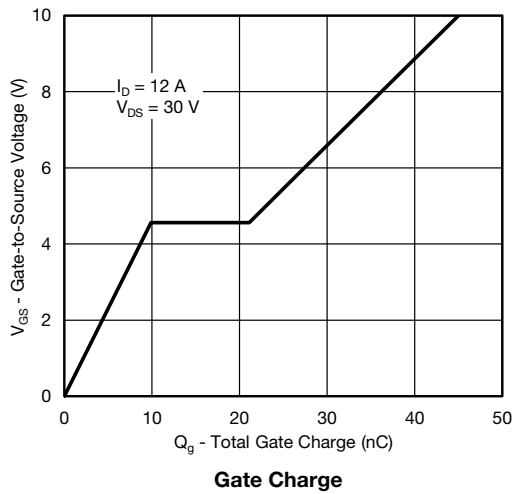
Notes

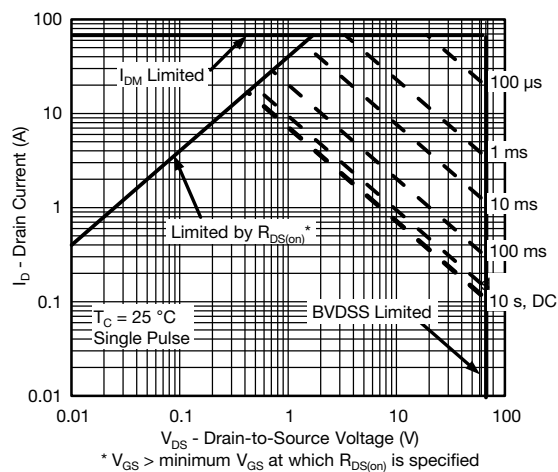
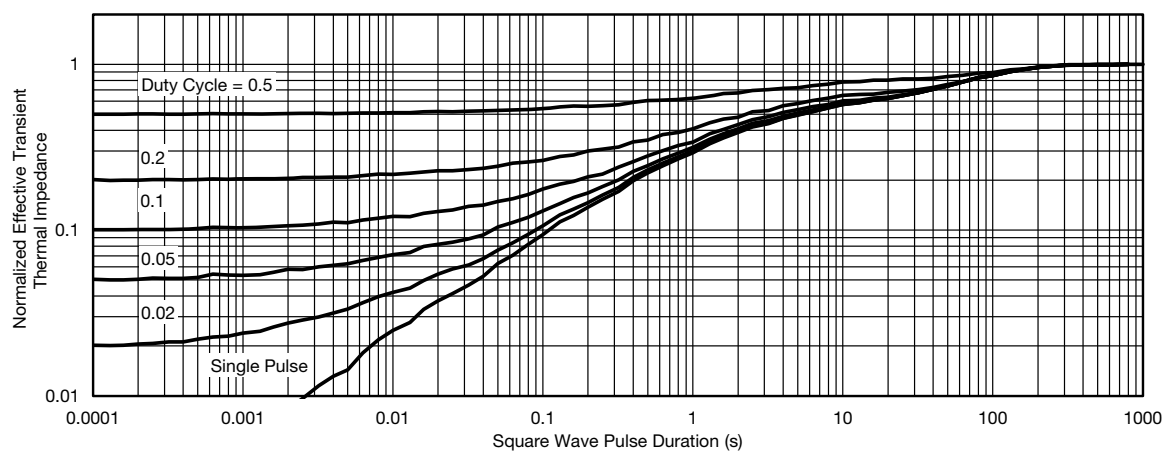
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.
 c. Independent of operating temperature.

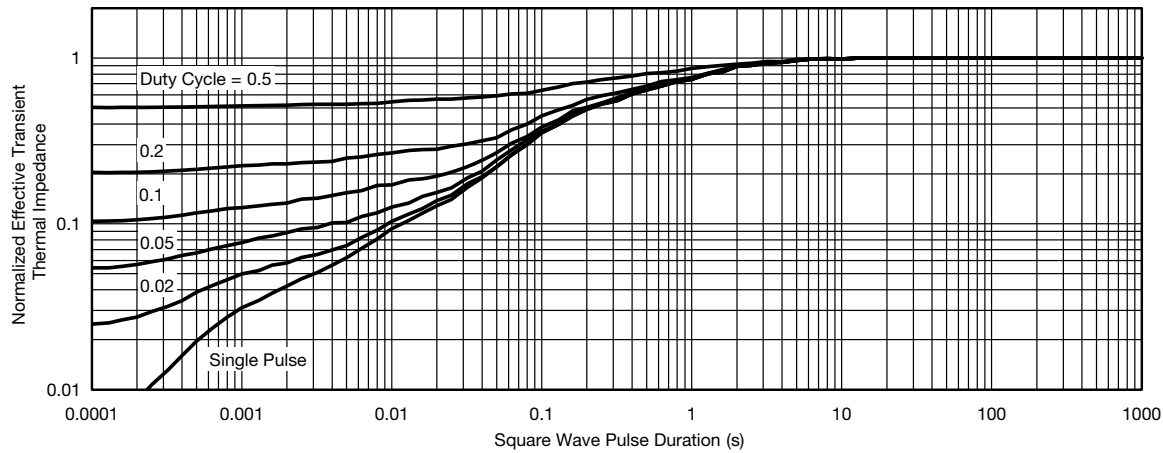
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)


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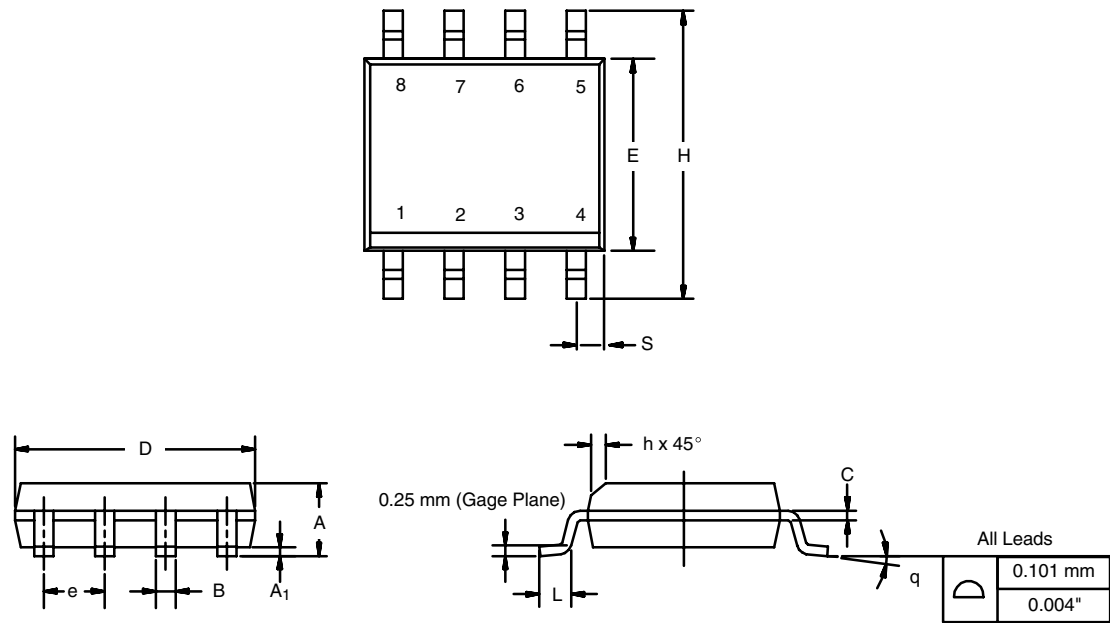


THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Safe Operating Area

Normalized Thermal Transient Impedance, Junction-to-Ambient

THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Foot
Note

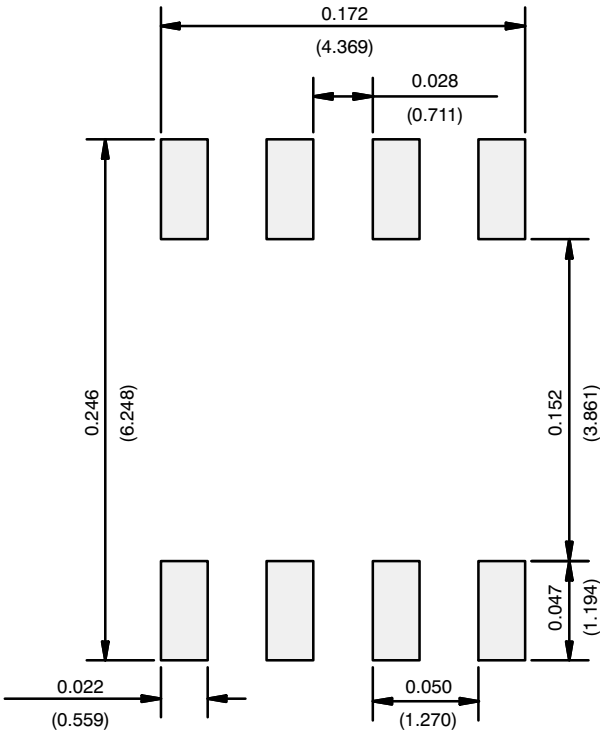
- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Foot ($25\text{ }^{\circ}\text{C}$)
 are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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