



General Description

The FDBL86063-F085 use advanced SGT MOSFET technology to provide low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. This device is specially designed to get better ruggedness.

General Features

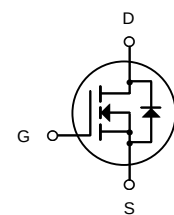
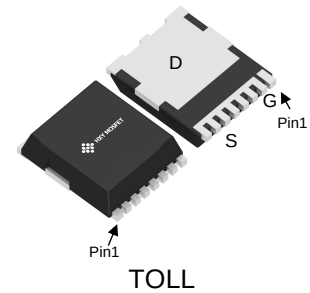
$V_{DS} = 100V$ $I_D = 300A$

$R_{DS(ON)} < 2.6m\Omega$ @ $V_{GS}=10V$

Applications

Battery Protection

Power Distribution



N-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
FDBL86063-F085	TOLL	HXY MOSFET	2000

Absolute Maximum Ratings at $T_J=25^\circ C$ unless otherwise noted

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ¹	$T_C=25^\circ C$	I_D	300	A
	$T_C=100^\circ C$		163	
Pulsed Drain Current ²		I_{DM}	1028	A
Single Pulse Avalanche Energy ³		EAS	583	mJ
Avalanche Current		I_{AS}	54	A
Total Power Dissipation	$T_C=25^\circ C$	P_D	379	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ C$
Thermal Resistance from Junction-to-Ambient ¹		$R_{\theta JA}$	59	$^\circ C/W$
Thermal Resistance from Junction-to-Case ¹		$R_{\theta JC}$	0.33	$^\circ C/W$



Electrical Characteristics (T_J = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	100	---	---	V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =1mA	---	---	---	V/°C
R _{DS(on)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =20A	---	2.0	2.6	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	2	3	4	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	---	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =100V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =100V, V _{GS} =0V, T _J =100°C	---	---	100	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =20A	---	76	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	2.3	---	Ω
Q _g	Total Gate Charge	V _{DS} =50V, V _{GS} =10V, I _D =20A	---	150	---	nC
Q _{gs}	Gate-Source Charge		---	32.5	---	
Q _{gd}	Gate-Drain Charge		---	49	---	
T _{d(on)}	Turn-On Delay Time	V _{GS} =10V, V _{DD} =50V, R _G =3Ω, I _D =20A	---	27	---	ns
T _r	Rise Time		---	78.5	---	
T _{d(off)}	Turn-Off Delay Time		---	110	---	
T _f	Fall Time		---	86	---	
C _{iss}	Input Capacitance	V _{DS} =50V, V _{GS} =0V, f=1MHz	---	9030	---	pF
C _{oss}	Output Capacitance		---	1505	---	
C _{rss}	Reverse Transfer Capacitance		---	40	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,4}	V _G =V _D =0V, Force Current	---	---	300	A
I _{SM}	Pulsed Source Current ^{2,4}		---	---	1000	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.2	V
t _{rr}	Reverse Recovery Time	IF = 20A, di/dt = 100A/μs	---	90	---	nS
Q _{rr}	Reverse Recovery Charge		---	175	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3.The EAS data shows Max. rating. The test condition is T_J = 25°C, V_{DD}=50V, V_{GS}=10V, L=0.4mH, I_{AS}=54A.
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.



Typical Characteristics

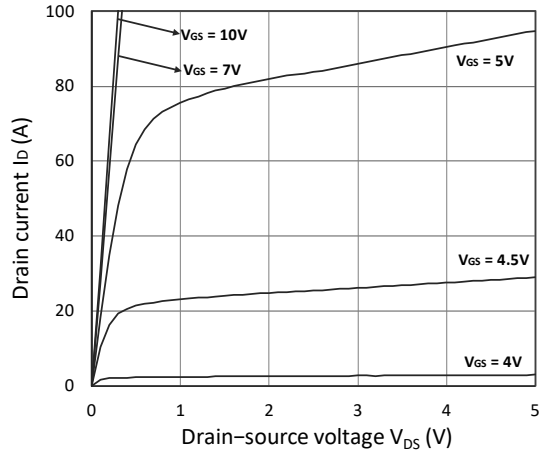


Figure 1. Output Characteristics

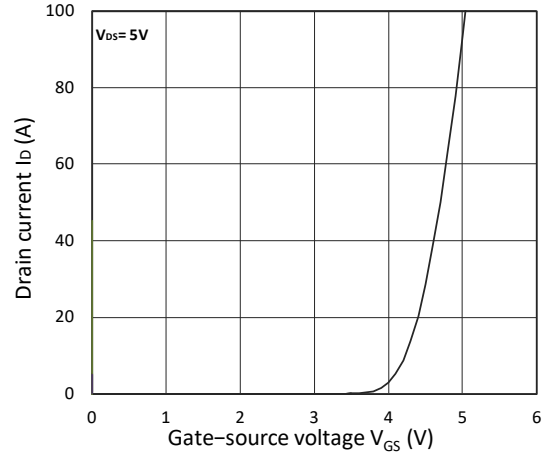


Figure 2. Transfer Characteristics

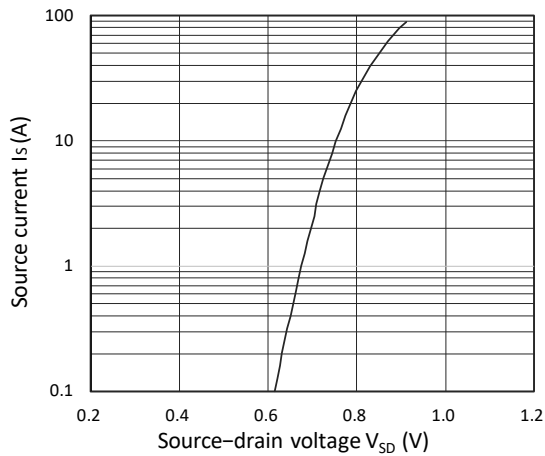


Figure 3. Forward Characteristics of Reverse

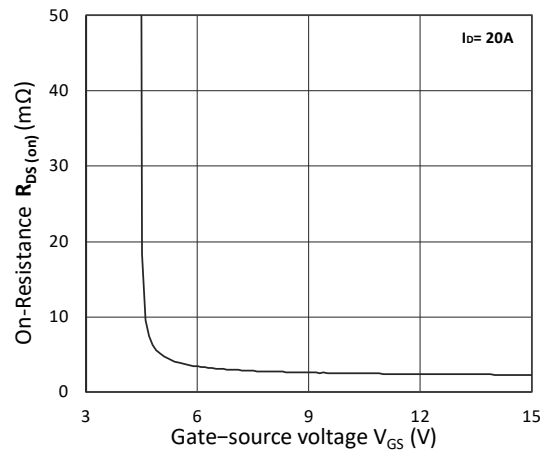


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

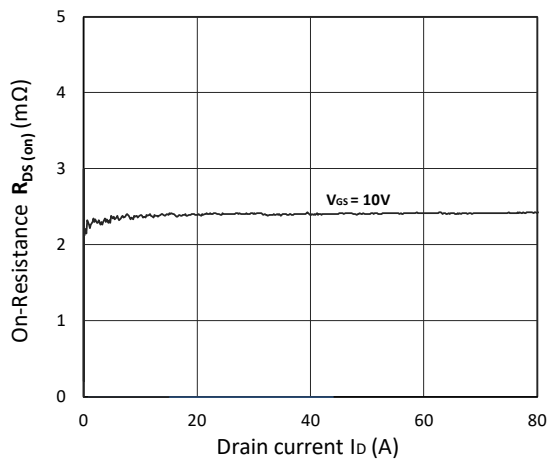


Figure 5. $R_{DS(ON)}$ vs. I_D

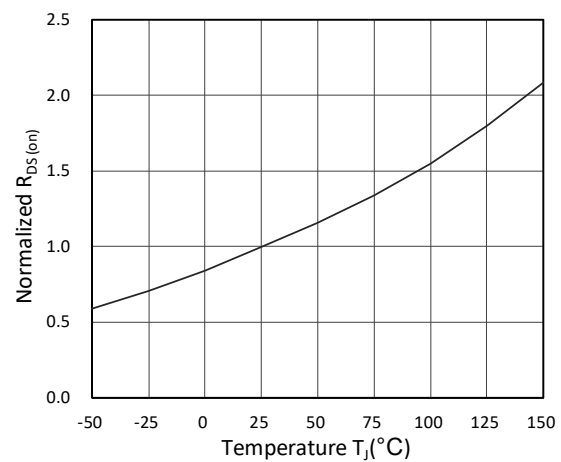


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

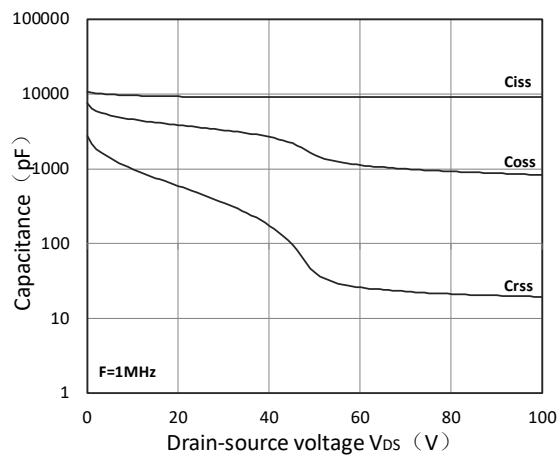


Figure 7. Capacitance Characteristics

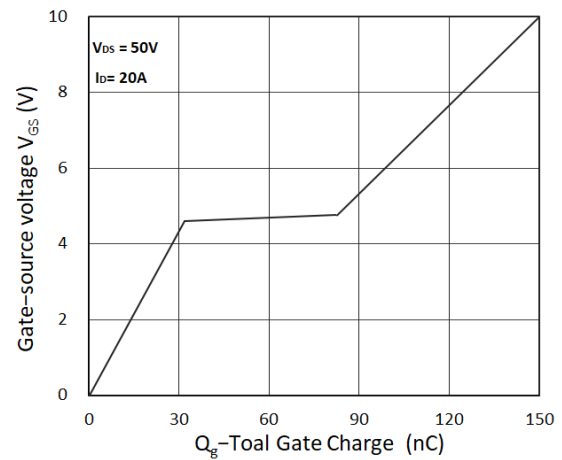


Figure 8. Gate Charge Characteristics

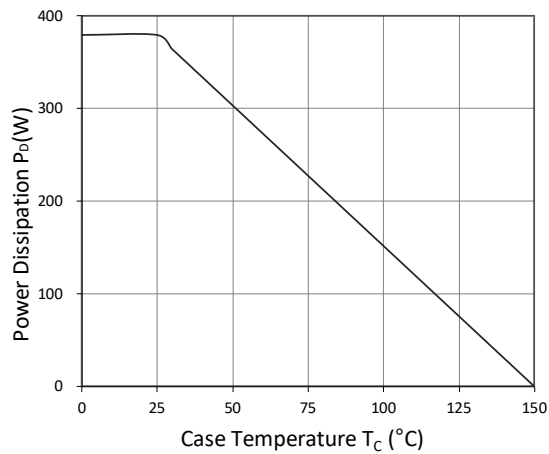


Figure 9. Power Dissipation

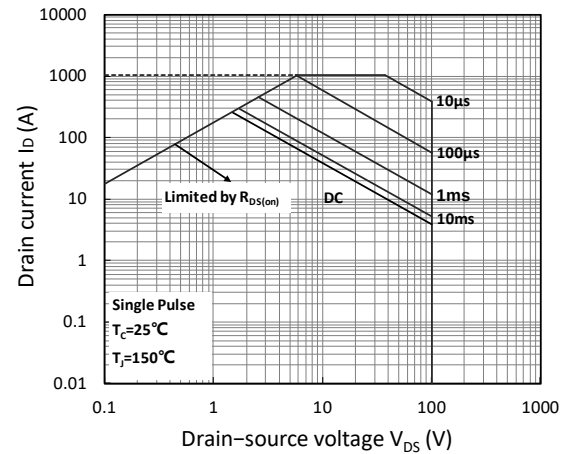


Figure 10. Safe Operating Area

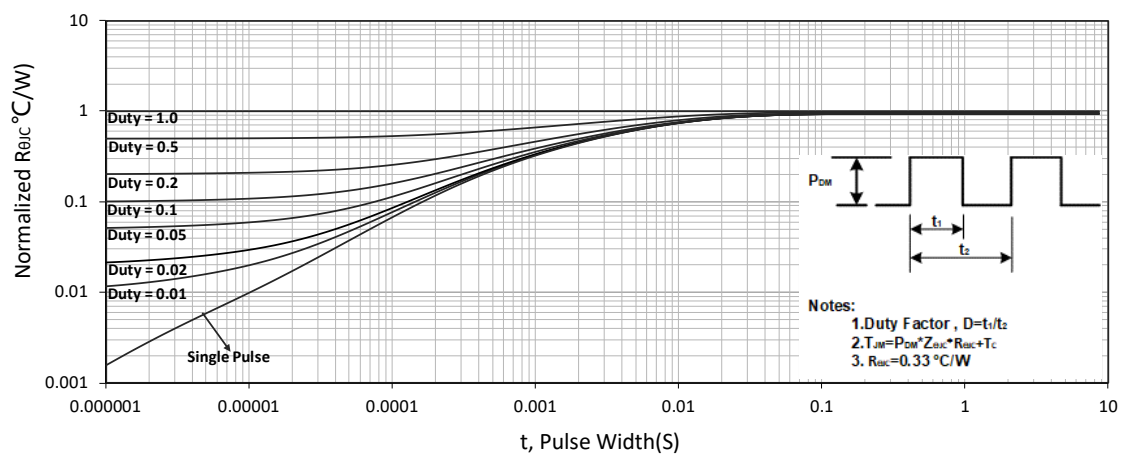


Figure 11. Normalized Maximum Transient Thermal Impedance



Test Circuit

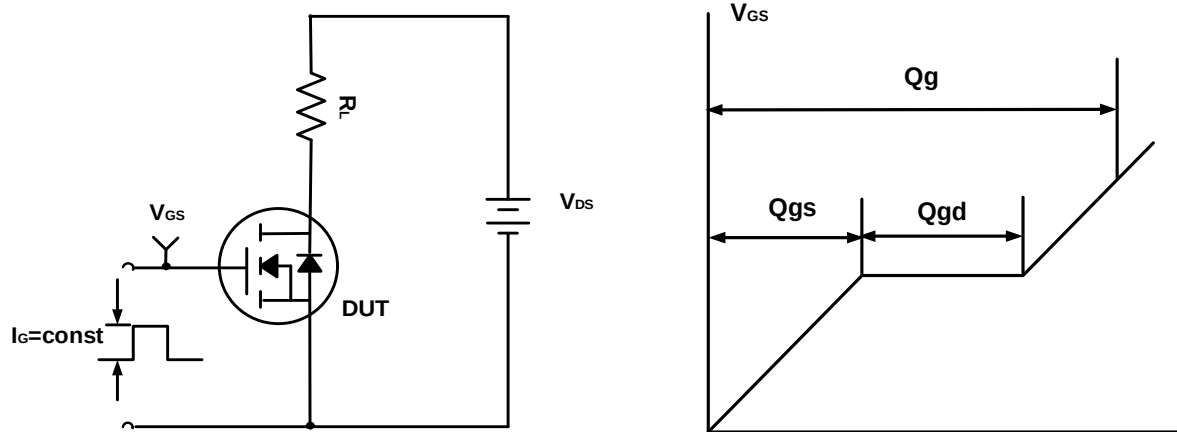


Figure A. Gate Charge Test Circuit & Waveforms

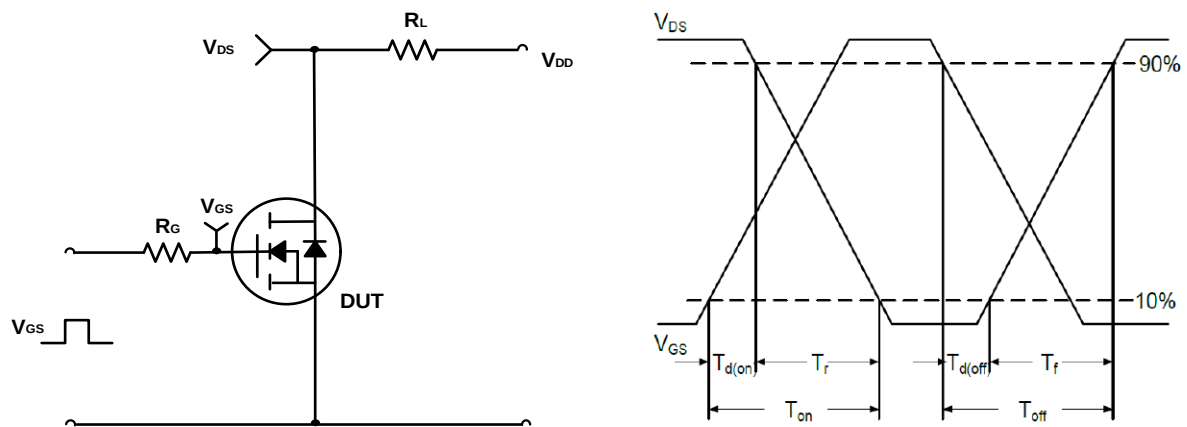
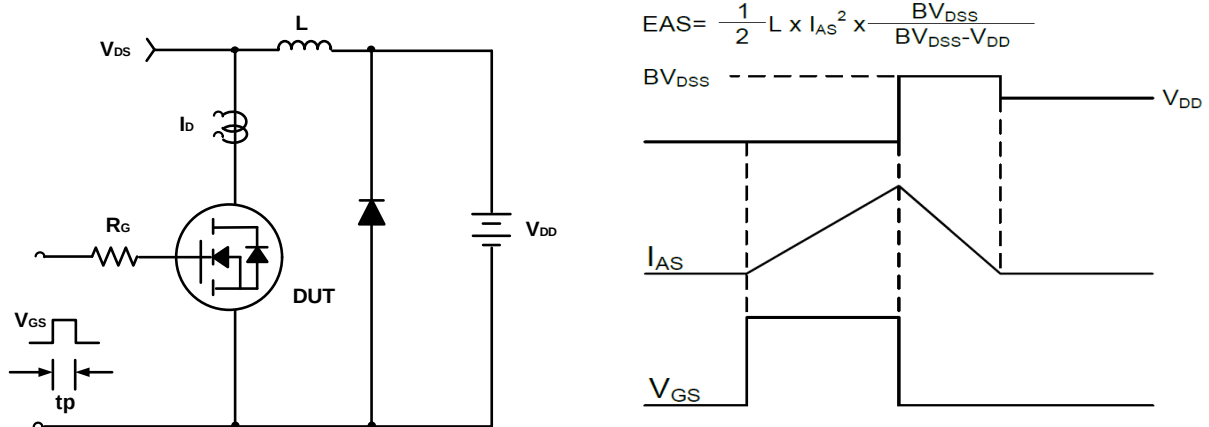
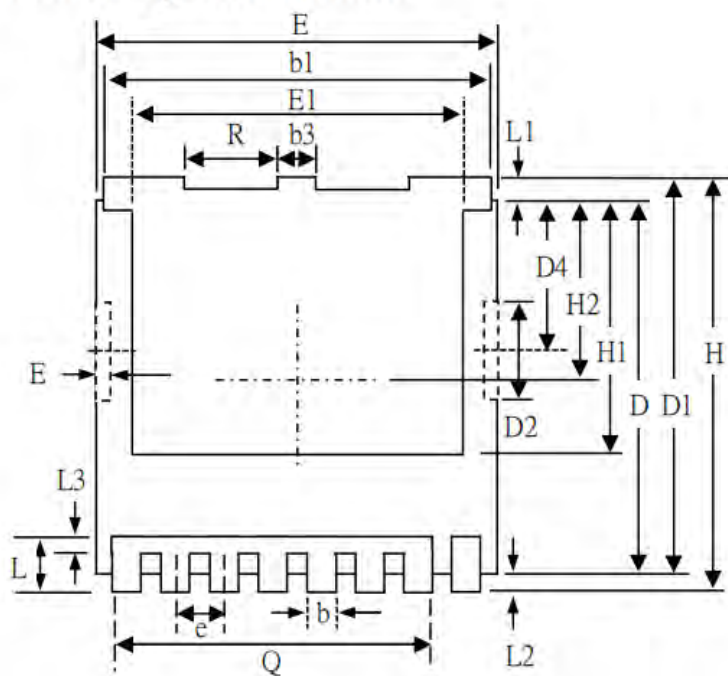


Figure B. Switching Test Circuit & Waveforms

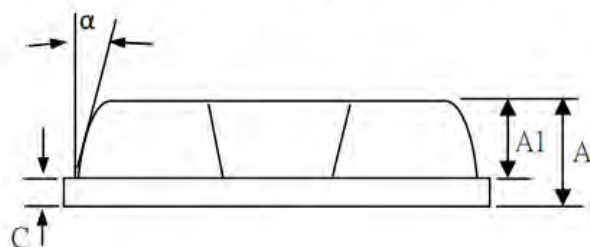




TOLL Package Information



BACKSIDE VIEW



- 1.All Dimension Are In Millimeters.
- 2.Dimension Does Not Include Mold Protrusions.

SYMBOLS	MIN	NOM	MAX
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b3	1.10	1.20	1.30
c	0.40	0.50	0.60
D	10.28	10.38	10.58
D1	9.80	11.08	11.80
D2	3.10	3.30	3.50
D4	4.37	4.55	4.77
E	9.70	9.90	10.10
E1	7.90	8.10	8.30
E2	0.50	0.70	0.90
e	1.20BCS		
H	11.48	11.68	11.88
H1	6.95BCS		
H2	5.89BCS		
L	1.40	1.90	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.30	0.70	1.30
Q	8.00 REF.		
R	2.95	3.10	3.25
α	4°		10°



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