

SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

Check for Samples: [SN74LVC1T45-Q1](#)

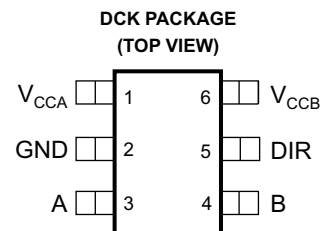
FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
 - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level H2
 - Device CDM ESD Classification Level C3B
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- DIR Input Circuit Referenced to V_{CCA}
- ± 24 -mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation

- Maximum Data Rates
 - 420 Mbps (3.3-V to 5-V Translation)
 - 210 Mbps (Translate to 3.3 V)
 - 140 Mbps (Translate to 2.5 V)
 - 75 Mbps (Translate to 1.8 V)

APPLICATIONS

- Automotive
- Logic Applications



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This single-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V. The B port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

The SN74LVC1T45-Q1 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ} .

The SN74LVC1T45-Q1 is designed so that the DIR input is powered by V_{CCA} .

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then both ports are in the high-impedance state.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION⁽¹⁾

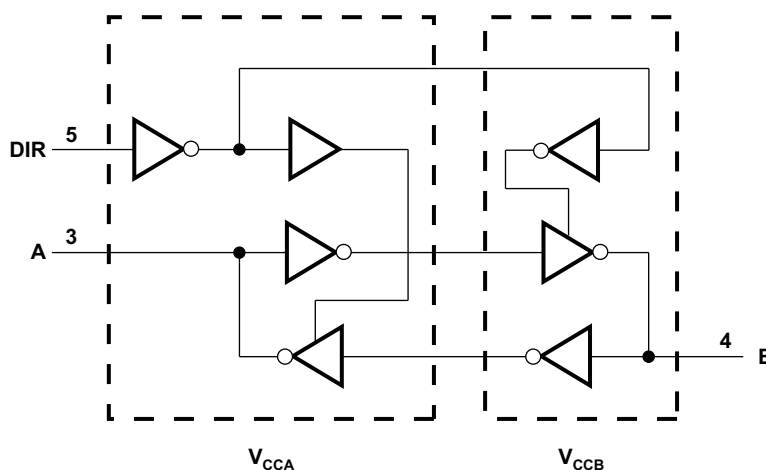
T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOT (SC-70) – DCK	Reel of 3000	SN74LVC1T45QDCKRQ1	5TR

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTION TABLE⁽¹⁾

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

- (1) Input circuits of the data I/Os always are active.

LOGIC DIAGRAM (POSITIVE LOGIC)**Absolute Maximum Ratings⁽¹⁾**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CCA} V _{CCB}	Supply voltage range	–0.5	6.5	V
V _I	Input voltage range ⁽²⁾	–0.5	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	6.5	V
V _O	Voltage range applied to any output in the high or low state ^{(2) (3)}	A port	–0.5 V _{CCA} + 0.5	V
		B port	–0.5 V _{CCB} + 0.5	
I _{IK}	Input clamp current	V _I < 0	–50	mA
I _{OK}	Output clamp current	V _O < 0	–50	mA
I _O	Continuous output current		±50	mA
	Continuous current through V _{CC} or GND		±100	mA
T _{stg}	Storage temperature range	–65	150	°C
ESD rating s	Human Body Model (HBM) AEC-Q100 Classification Level H2		2	kV
	Charged Device Model (CDM) AEC-Q100 Classification Level C3B		750	V

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The value of V_{CC} is provided in the Recommended Operating Conditions table.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		SN74LVC1T45-Q1	UNIT
		DCK	
		6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	286.8	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance ⁽³⁾	93.9	°C/W
θ_{JB}	Junction-to-board thermal resistance ⁽⁴⁾	95.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter ⁽⁵⁾	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter ⁽⁶⁾	94.7	°C/W
θ_{JCbott}	Junction-to-case (bottom) thermal resistance ⁽⁷⁾	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

Recommended Operating Conditions^{(1) (2) (3)}

Recommended operating conditions			V _{CCI}	V _{CCO}	MIN	MAX	UNIT
V _{CCA}	Supply voltage				1.65	5.5	V
V _{CCB}					1.65	5.5	
V _{IH}	High-level input voltage	Data inputs ⁽⁴⁾	1.65 V to 1.95 V		V _{CCI} × 0.65		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		V _{CCI} × 0.7		
V _{IL}	Low-level input voltage	Data inputs ⁽⁴⁾	1.65 V to 1.95 V		V _{CCI} × 0.35		V
			2.3 V to 2.7 V		0.7		
			3 V to 3.6 V		0.8		
			4.5 V to 5.5 V		V _{CCI} × 0.3		
V _{IH}	High-level input voltage	DIR (referenced to V _{CCA}) ⁽⁵⁾	1.65 V to 1.95 V		V _{CCA} × 0.65		V
			2.3 V to 2.7 V		1.7		
			3 V to 3.6 V		2		
			4.5 V to 5.5 V		V _{CCA} × 0.7		
V _{IL}	Low-level input voltage	DIR (referenced to V _{CCA}) ⁽⁵⁾	1.65 V to 1.95 V		V _{CCA} × 0.35		V
			2.3 V to 2.7 V		0.7		
			3 V to 3.6 V		0.8		
			4.5 V to 5.5 V		V _{CCA} × 0.3		
V _I	Input voltage				0	5.5	V
V _O	Output voltage				0	V _{CCO}	V
I _{OH}	High-level output current		1.65 V to 1.95 V		–4		mA
			2.3 V to 2.7 V		–8		
			3 V to 3.6 V		–24		
			4.5 V to 5.5 V		–32		
I _{OL}	Low-level output current		1.65 V to 1.95 V		4		mA
			2.3 V to 2.7 V		8		
			3 V to 3.6 V		24		
			4.5 V to 5.5 V		32		
Δt/Δv	Input transition rise or fall rate	Data inputs	1.65 V to 1.95 V		20		ns/V
			2.3 V to 2.7 V		20		
			3 V to 3.6 V		10		
			4.5 V to 5.5 V		5		
	Control inputs		1.65 V to 5.5 V		5		
T _A	Operating free-air temperature				–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.(2) V_{CCO} is the V_{CC} associated with the output port.(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.

Electrical Characteristics^{(1) (2)}

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CCA}	V _{CCB}	T _A = 25°C			T _A = –40°C to 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V _{OH}		I _{OH} = –100 μA	V _I = V _{IH}	1.65 V to 4.5 V	1.65 V to 4.5 V			V _{CCO} – 0.1	V	
		I _{OH} = –4 mA		1.65 V	1.65 V			1.2		
		I _{OH} = –8 mA		2.3 V	2.3 V			1.9		
		I _{OH} = –24 mA		3 V	3 V			2.3		
		I _{OH} = –32 mA		4.5 V	4.5 V			3.8		
V _{OL}		I _{OL} = 100 μA	V _I = V _{IL}	1.65 V to 4.5 V	1.65 V to 4.5 V			0.1	V	
		I _{OL} = 4 mA		1.65 V	1.65 V			0.45		
		I _{OL} = 8 mA		2.3 V	2.3 V			0.4		
		I _{OL} = 24 mA		3 V	3 V			0.65		
		I _{OL} = 32 mA		4.5 V	4.5 V			0.65		
I _I	DIR	V _I = V _{CCA} or GND	1.65 V to 5.5 V	1.65 V to 5.5 V			±1	±4	μA	
I _{off}	A port	V _I or V _O = 0 to 5.5 V	0 V	0 to 5.5 V			±1	±10	μA	
	B port		0 to 5.5 V	0 V			±1	±10		
I _{OZ}	A or B port	V _O = V _{CCO} or GND	1.65 V to 5.5 V	1.65 V to 5.5 V			±1	±10	μA	
I _{CCA}		V _I = V _{CCI} or GND, I _O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V				10	μA	
			5.5 V	0 V				4		
			0 V	5.5 V				–10		
I _{CCB}		V _I = V _{CCI} or GND, I _O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V				10	μA	
			5.5 V	0 V				–10		
			0 V	5.5 V				4		
I _{CCA} + I _{CCB}		V _I = V _{CCI} or GND, I _O = 0	1.65 V to 5.5 V	1.65 V to 5.5 V				20	μA	
ΔI _{CCA}	A port	A port at V _{CCA} – 0.6 V, DIR at V _{CCA} , B port = open	3 V to 5.5 V	3 V to 5.5 V				50	μA	
	DIR	DIR at V _{CCA} – 0.6 V, B port = open, A port at V _{CCA} or GND						50		
ΔI _{CCB}	B port	B port at V _{CCB} – 0.6 V, DIR at GND, A port = open	3 V to 5.5 V	3 V to 5.5 V				50	μA	
C _i	DIR	V _I = V _{CCA} or GND	3.3 V	3.3 V			2.5		pF	
C _{i0}	A or B port	V _O = V _{CCA/B} or GND	3.3 V	3.3 V			6		pF	

(1) V_{CCO} is the V_{CC} associated with the output port.

(2) V_{CCI} is the V_{CC} associated with the input port.

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$ (see [Figure 9](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3	20.7	2.2	13.3	1.7	11.3	1.4	10.2	ns
t_{PHL}			2.8	17.3	2.2	11.5	1.8	10.1	1.7	10	ns
t_{PLH}	B	A	3	20.7	2.3	19	2.1	18.5	1.9	18.1	ns
t_{PHL}			2.8	17.3	2.1	15.9	2	15.6	1.8	15.2	ns
t_{PHZ}	DIR	A	5.2	22.7	4.8	21.5	4.7	21.4	5.1	20.1	ns
t_{PLZ}			2.3	13.5	2.1	13.5	2.4	13.7	3.1	13.9	ns
t_{PHZ}	DIR	B	7.4	27.9	4.9	14.5	3.6	13.3	2.3	11.2	ns
t_{PLZ}			4.2	19	2.2	12.2	2.3	11.4	2.0	9.4	ns
$t_{PZH}^{(1)}$	DIR	A	39.7		31.2		29.9		27.5		ns
$t_{PZL}^{(1)}$			45.2		30.4		28.9		26.4		ns
$t_{PZH}^{(1)}$	DIR	B	34.2		26.8		25		24.1		ns
$t_{PZL}^{(1)}$			40.7		33		31.5		30.1		ns

(1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ (see [Figure 9](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.3	19	1.5	11.5	1.3	9.4	1.1	8.1	ns
t_{PHL}			2.1	15.9	1.4	10.5	1.3	8.4	0.9	7.6	ns
t_{PLH}	B	A	2.2	13.3	1.5	11.5	1.4	11	1	10.5	ns
t_{PHL}			2.2	11.5	1.4	10.7	1.3	10	0.9	9.2	ns
t_{PHZ}	DIR	A	3	11.1	2.1	11.1	2.3	11.1	3.2	11.1	ns
t_{PLZ}			1.3	8.9	1.3	8.9	1.3	8.9	1	8.8	ns
t_{PHZ}	DIR	B	6.5	26.7	4.1	14.4	3.0	13.2	1.9	10.1	ns
t_{PLZ}			3.5	21.9	2.2	12.6	2.5	11.4	1.6	8.3	ns
$t_{PZH}^{(1)}$	DIR	A	35.2		24.1		22.4		18.8		ns
$t_{PZL}^{(1)}$			38.2		24.9		23.2		19.3		ns
$t_{PZH}^{(1)}$	DIR	B	27.9		20.4		18.3		16.9		ns
$t_{PZL}^{(1)}$			27		21.6		19.5		18.7		ns

(1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$ (see [Figure 9](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V}$ $\pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.1	18.5	1.4	11	0.7	8.8	0.7	7.4	ns
t_{PHL}			2	15.6	1.3	10	0.8	8	0.7	7	ns
t_{PLH}	B	A	1.7	11.3	1.3	9.4	0.7	8.8	0.6	8.4	ns
t_{PHL}			1.8	10.1	1.3	8.4	0.8	8	0.7	7.5	ns
t_{PHZ}	DIR	A	2.3	10.3	2.4	10.3	1.5	10.3	2.4	10.3	ns
t_{PLZ}			1.8	8.6	1.6	8.6	1.9	8.7	2.0	8.7	ns
t_{PHZ}	DIR	B	5.4	27.5	3.9	13.1	2.9	11.8	1.7	9.8	ns
t_{PLZ}			2.3	17.5	2.1	10.8	2.4	10.1	1.5	7.9	ns
$t_{PZH}^{(1)}$	DIR	A	28.8		20.2		18.9		16.3		ns
$t_{PZL}^{(1)}$			37.6		21.5		19.8		17.3		ns
$t_{PZH}^{(1)}$	DIR	B	27.1		19.6		17.5		16.1		ns
$t_{PZL}^{(1)}$			25.9		20.3		18.3		17.3		ns

(1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$ (see [Figure 9](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V}$ $\pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.9	18.1	1	10.5	0.6	8.4	0.5	6.9	ns
t_{PHL}			1.8	15.2	0.9	9.2	0.7	7.5	0.5	6.5	ns
t_{PLH}	B	A	1.4	10.2	1	8.1	0.7	7.4	0.5	6.9	ns
t_{PHL}			1.7	10	0.9	7.6	0.7	7	0.5	6.5	ns
t_{PHZ}	DIR	A	2.1	8.4	2.0	8.4	2.2	8.5	2.0	8.4	ns
t_{PLZ}			0.9	6.8	1	6.8	1	6.7	0.9	6.7	ns
t_{PHZ}	DIR	B	4.8	26.2	2.5	14.8	1	11.5	1.7	9.5	ns
t_{PLZ}			2.6	17.8	2.0	10.4	2.5	10	1.6	7.5	ns
$t_{PZH}^{(1)}$	DIR	A	28		18.5		17.4		14.4		ns
$t_{PZL}^{(1)}$			36.2		22.4		18.5		16		ns
$t_{PZH}^{(1)}$	DIR	B	24.9		17.3		15.1		13.6		ns
$t_{PZL}^{(1)}$			23.6		17.6		16		14.9		ns

(1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.

Operating Characteristics

 $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CCA} = V_{CCB} = 1.8\text{ V}$	$V_{CCA} = V_{CCB} = 2.5\text{ V}$	$V_{CCA} = V_{CCB} = 3.3\text{ V}$	$V_{CCA} = V_{CCB} = 5\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	
C_{pdA} ⁽¹⁾	A-port input, B-port output	$C_L = 0\text{ pF}$, $f = 10\text{ MHz}$, $t_r = t_f = 1\text{ ns}$	3	4	4	4	pF
	B-port input, A-port output		18	19	20	21	
C_{pdB} ⁽¹⁾	A-port input, B-port output	$C_L = 0\text{ pF}$, $f = 10\text{ MHz}$, $t_r = t_f = 1\text{ ns}$	18	19	20	21	pF
	B-port input, A-port output		3	4	4	4	

(1) Power dissipation capacitance per transceiver

Power-Up Considerations

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

1. Connect ground before any supply voltage is applied.
2. Power up V_{CCA} .
3. V_{CCB} can be ramped up along with or after V_{CCA} .

TYPICAL CHARACTERISTICS

Figure 1. TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.8\text{ V}$

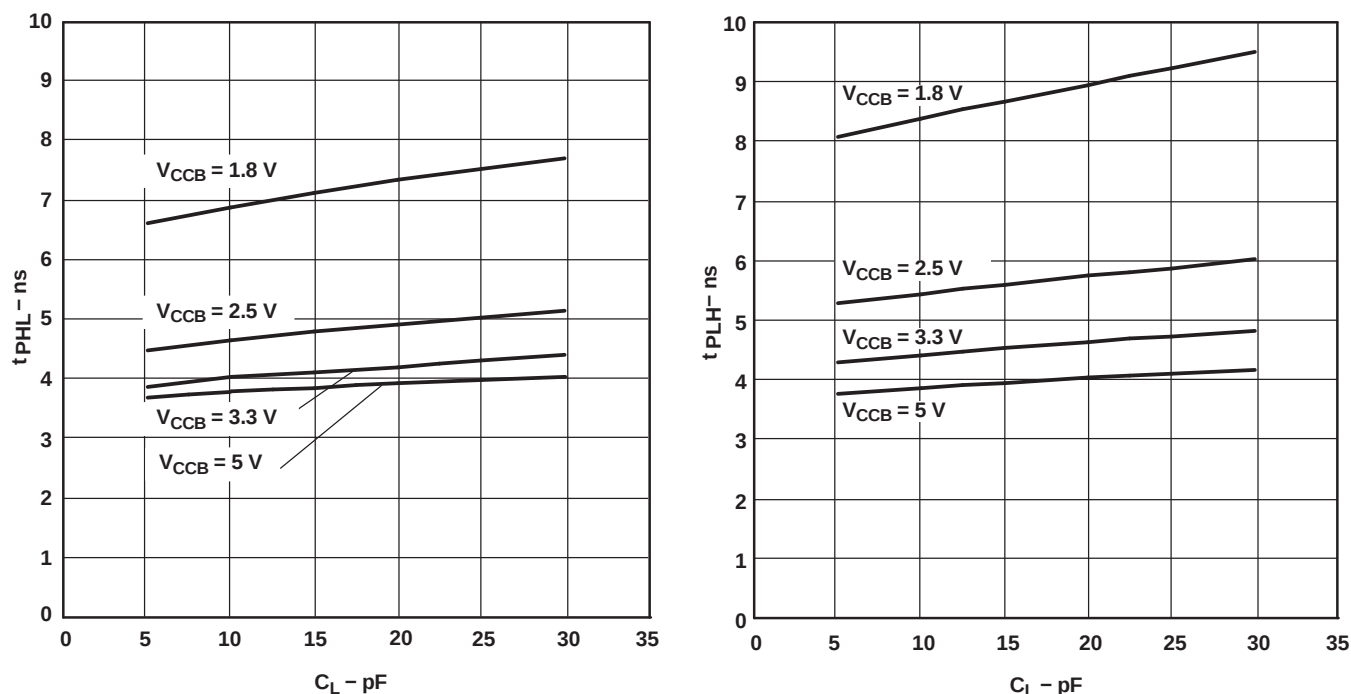
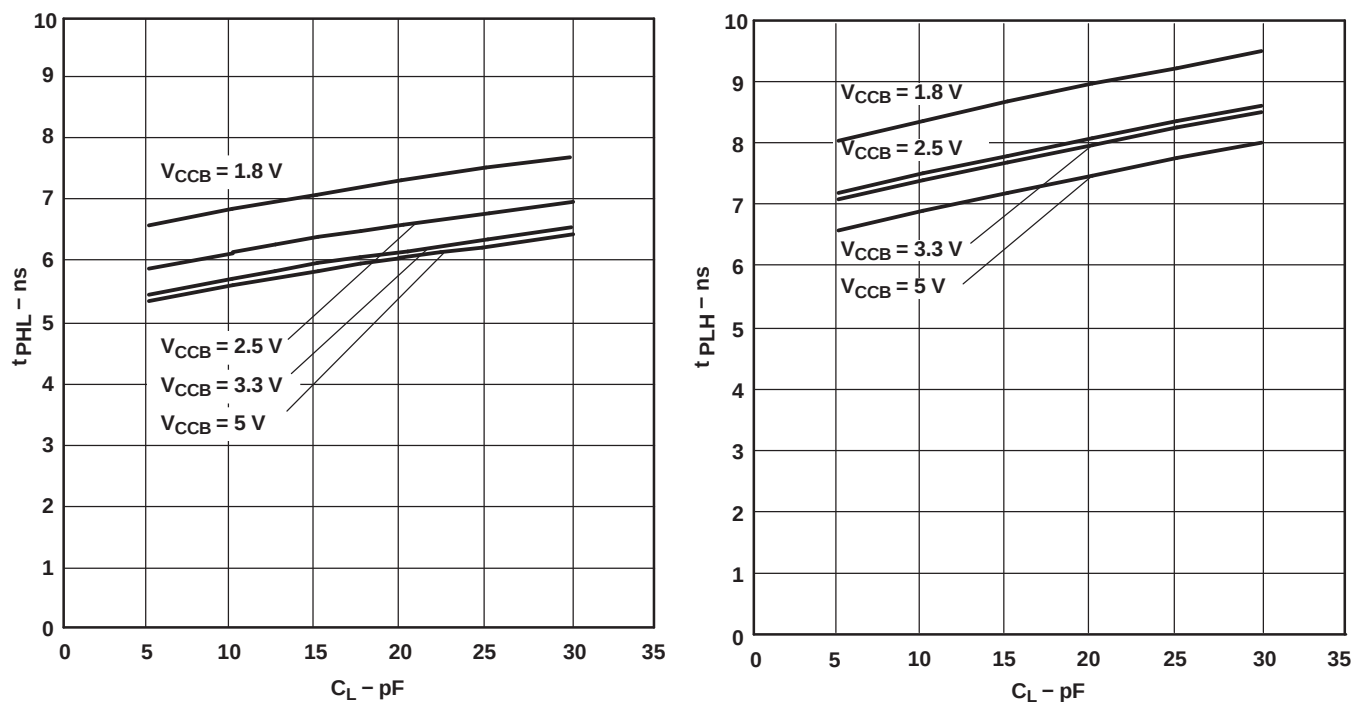


Figure 2. TYPICAL PROPAGATION DELAY (B to A) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.8\text{ V}$



TYPICAL CHARACTERISTICS (continued)
Figure 3. TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 2.5\text{ V}$

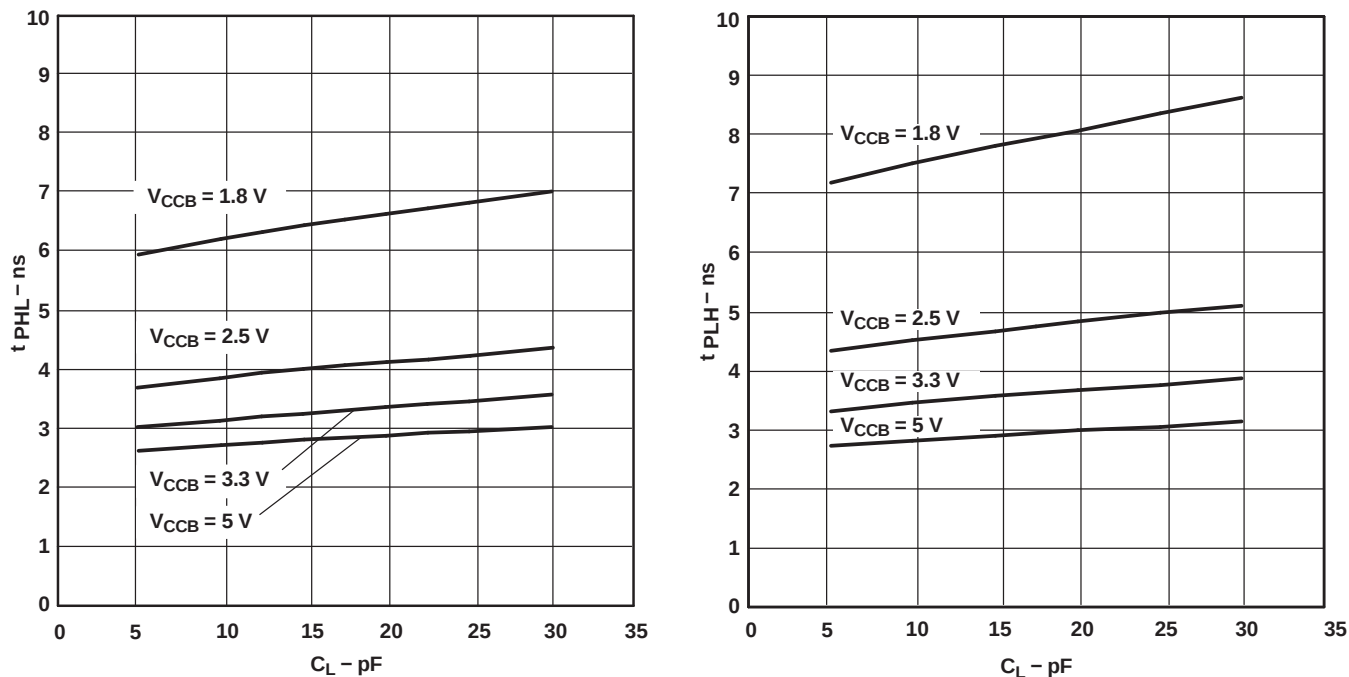
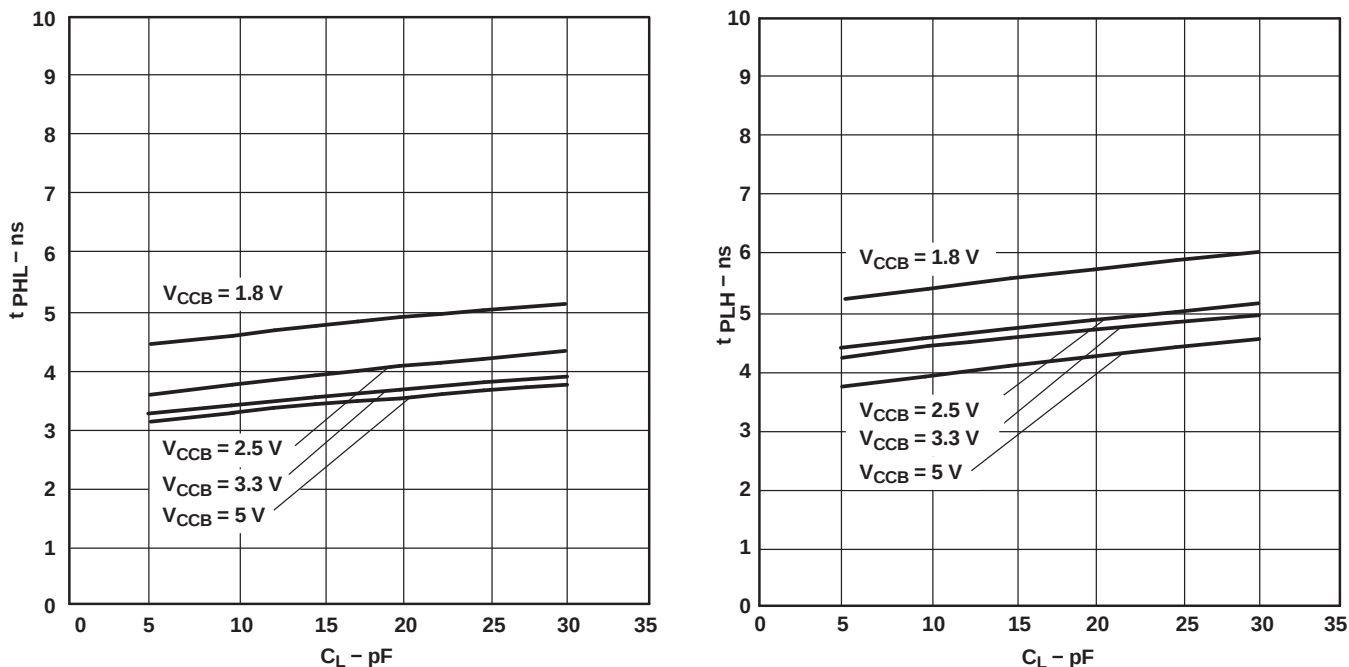


Figure 4. TYPICAL PROPAGATION DELAY (B to A) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 2.5\text{ V}$



TYPICAL CHARACTERISTICS (continued)

Figure 5. TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$

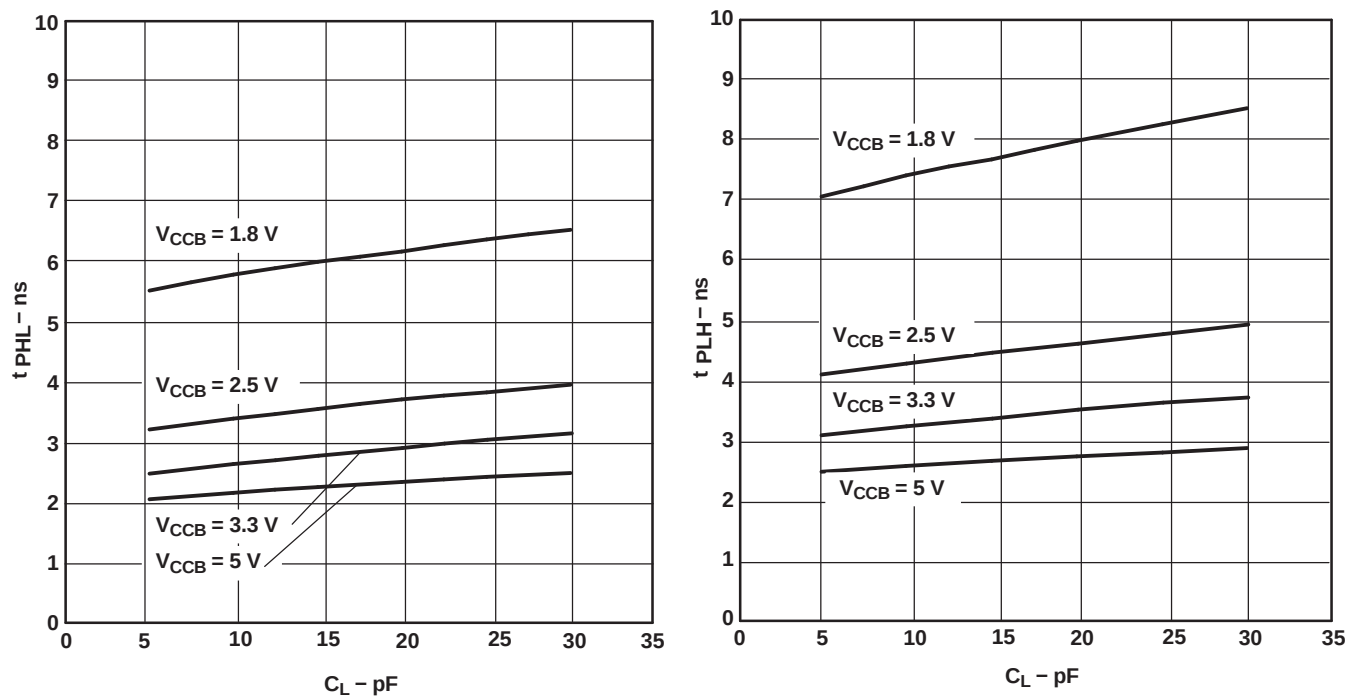
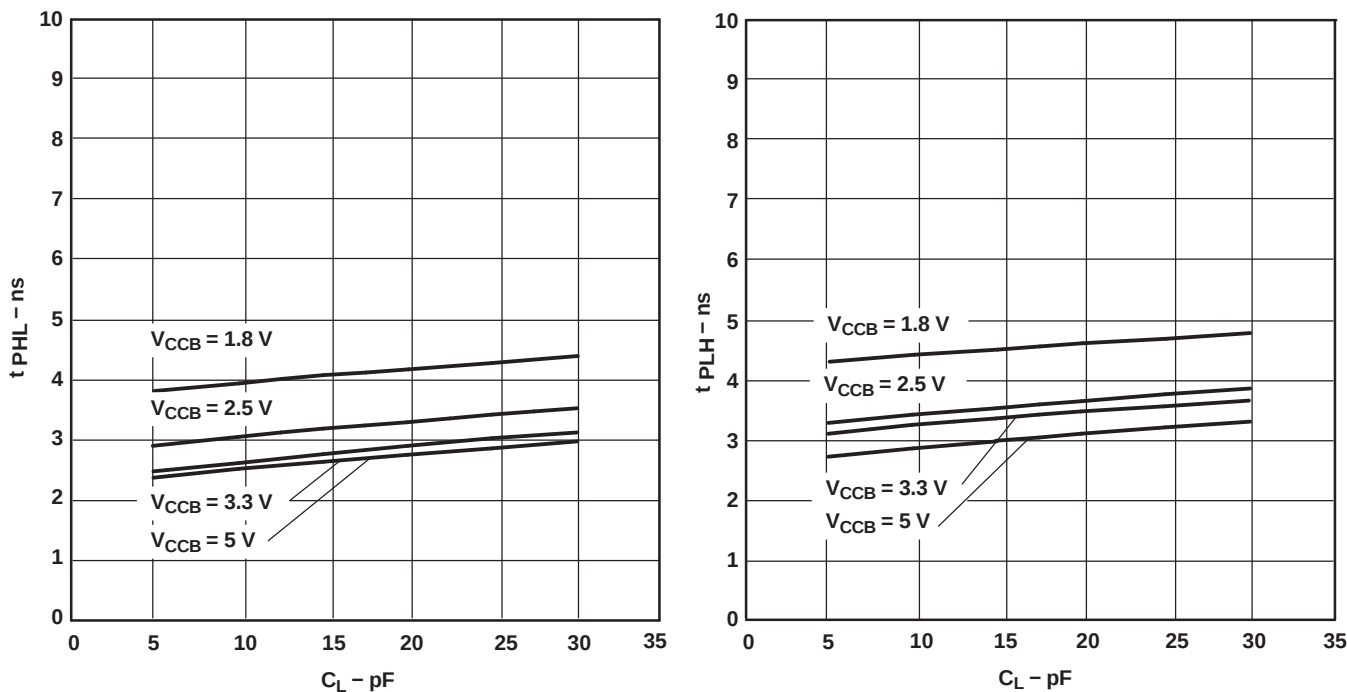


Figure 6. TYPICAL PROPAGATION DELAY (B to A) vs LOAD CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$



TYPICAL CHARACTERISTICS (continued)
Figure 7. TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 5\text{ V}$

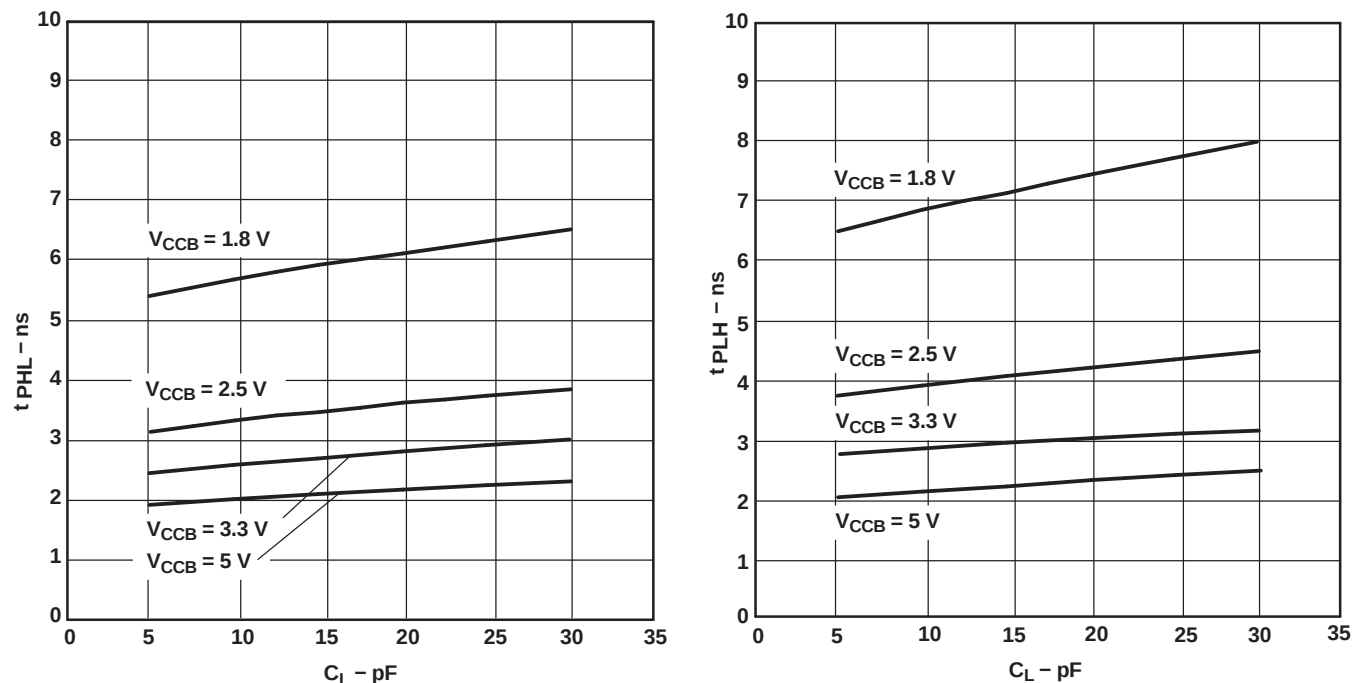
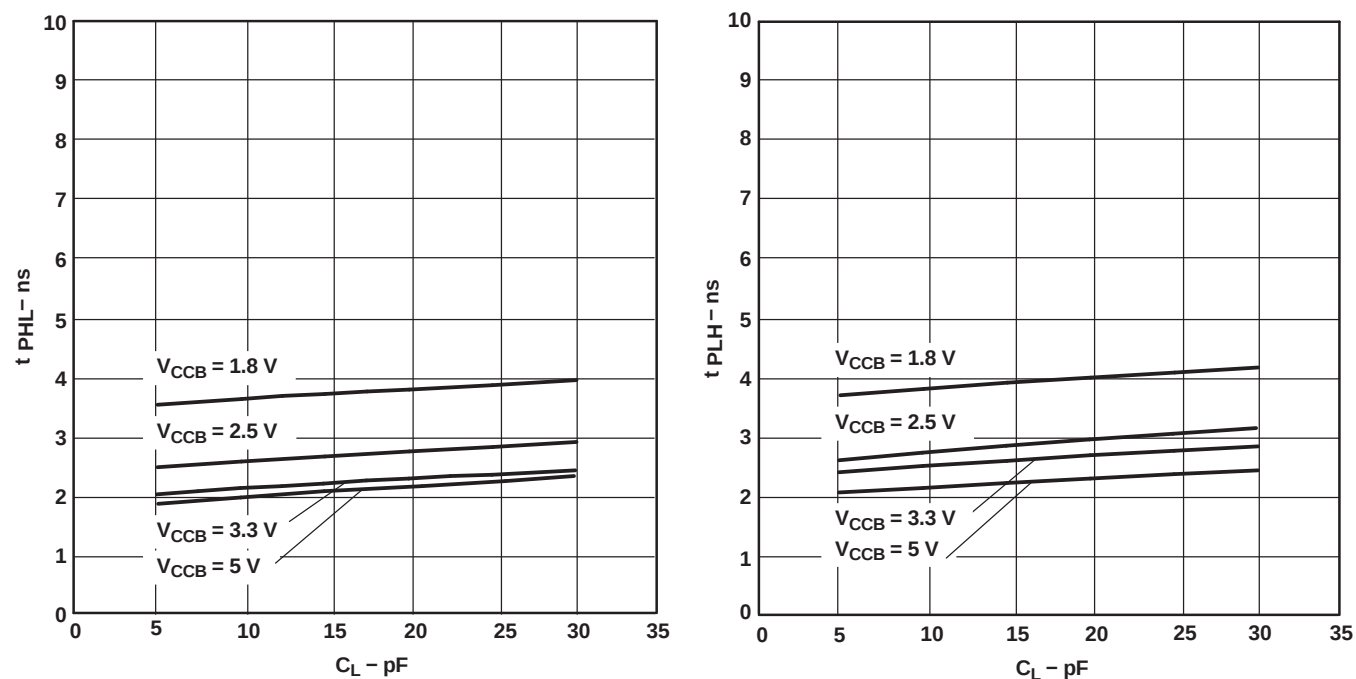
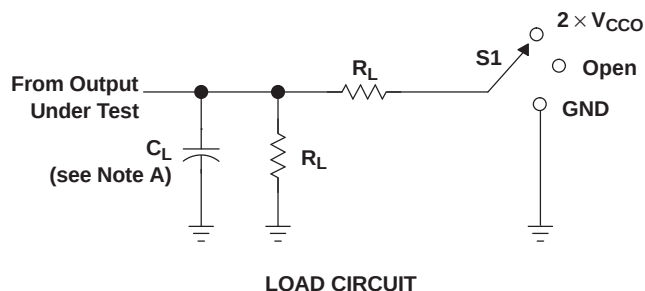


Figure 8. TYPICAL PROPAGATION DELAY (B to A) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 5\text{ V}$

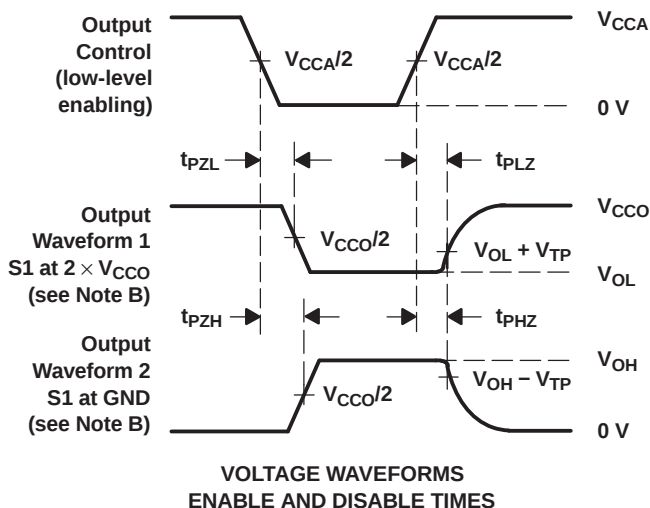
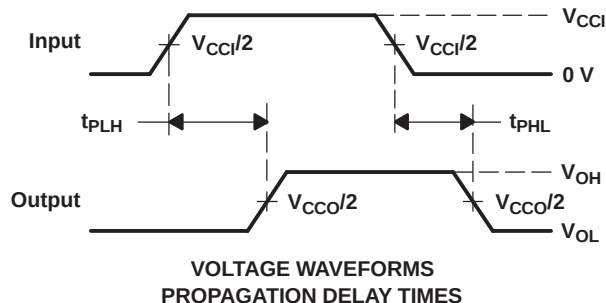
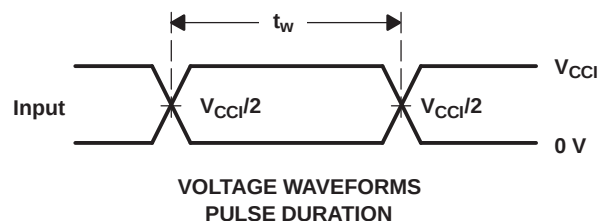


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

V_{CCO}	C_L	R_L	V_{TP}
$1.8 \text{ V} \pm 0.15 \text{ V}$	15 pF	2 k Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	15 pF	2 k Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	15 pF	2 k Ω	0.3 V
$5 \text{ V} \pm 0.5 \text{ V}$	15 pF	2 k Ω	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $dv/dt \geq 1 \text{ V/ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - V_{CCI} is the V_{CC} associated with the input port.
 - V_{CCO} is the V_{CC} associated with the output port.
 - All parameters and waveforms are not applicable to all devices.

Figure 9. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

Figure 10 shows an example of the SN74LVC1T45-Q1 being used in a unidirectional logic level-shifting application.

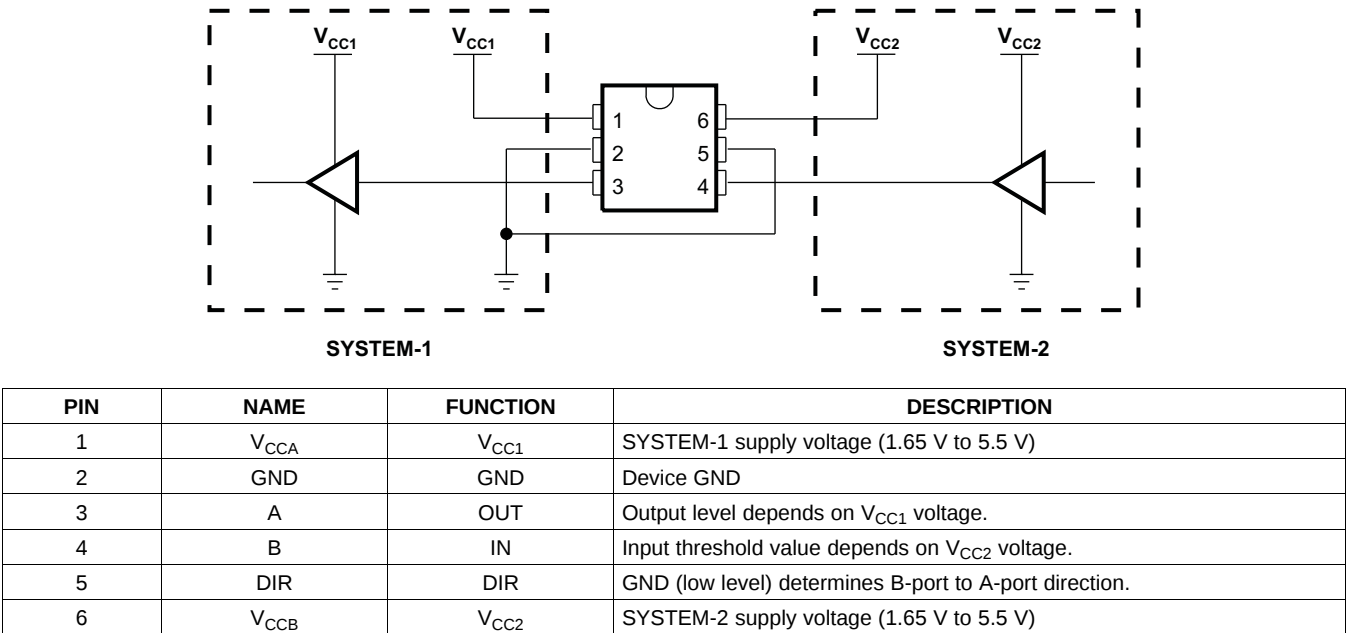
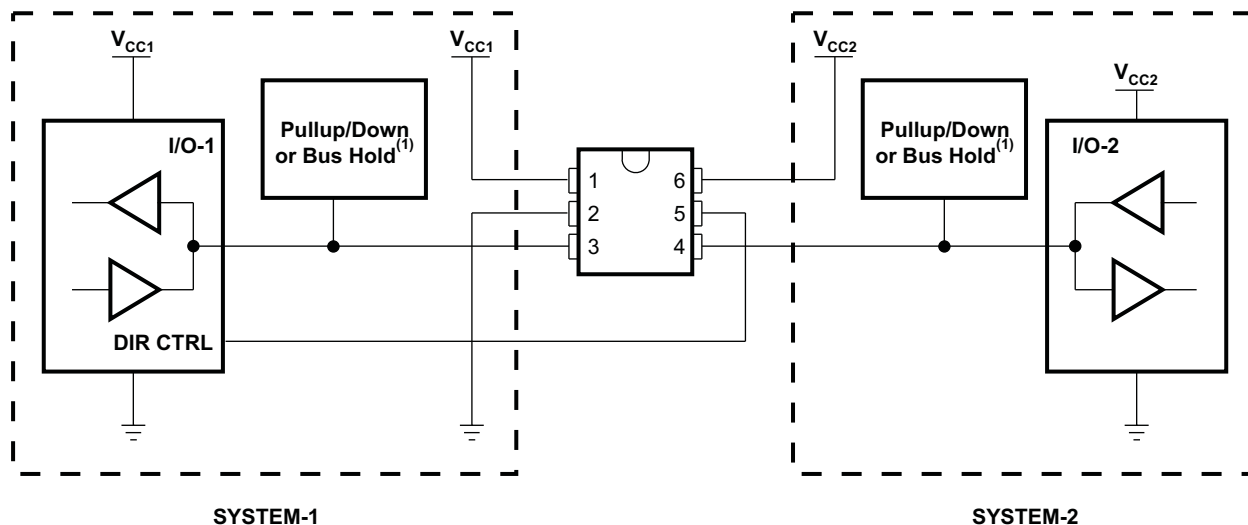


Figure 10. Unidirectional Logic Level-Shifting Application

Figure 11 shows the SN74LVC1T45-Q1 being used in a bidirectional logic level-shifting application. Because the SN74LVC1T45-Q1 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.



The following table shows data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	Out	In	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on pullup or pulldown. ⁽¹⁾
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pullup or pulldown. ⁽¹⁾
4	L	Out	In	SYSTEM-2 data to SYSTEM-1

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, i.e., both pullup or both pulldown.

Figure 11. Bidirectional Logic Level-Shifting Application

Enable Times

Calculate the enable times for the SN74LVC1T45-Q1 using the following formulas:

- $t_{PZH} \text{ (DIR to A)} = t_{PLZ} \text{ (DIR to B)} + t_{PLH} \text{ (B to A)}$
- $t_{PZL} \text{ (DIR to A)} = t_{PHZ} \text{ (DIR to B)} + t_{PHL} \text{ (B to A)}$
- $t_{PZH} \text{ (DIR to B)} = t_{PLZ} \text{ (DIR to A)} + t_{PLH} \text{ (A to B)}$
- $t_{PZL} \text{ (DIR to B)} = t_{PHZ} \text{ (DIR to A)} + t_{PHL} \text{ (A to B)}$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74LVC1T45-Q1 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LVC1T45QDCKRQ1	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1T45TDCKRQ1	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC1T45-Q1 :

● Catalog: [SN74LVC1T45](#)

● Enhanced Product: [SN74LVC1T45-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1T45QDCKRQ1	SC70	DCK	6	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3
SN74LVC1T45TDCKRQ1	SC70	DCK	6	3000	180.0	8.4	2.25	2.4	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

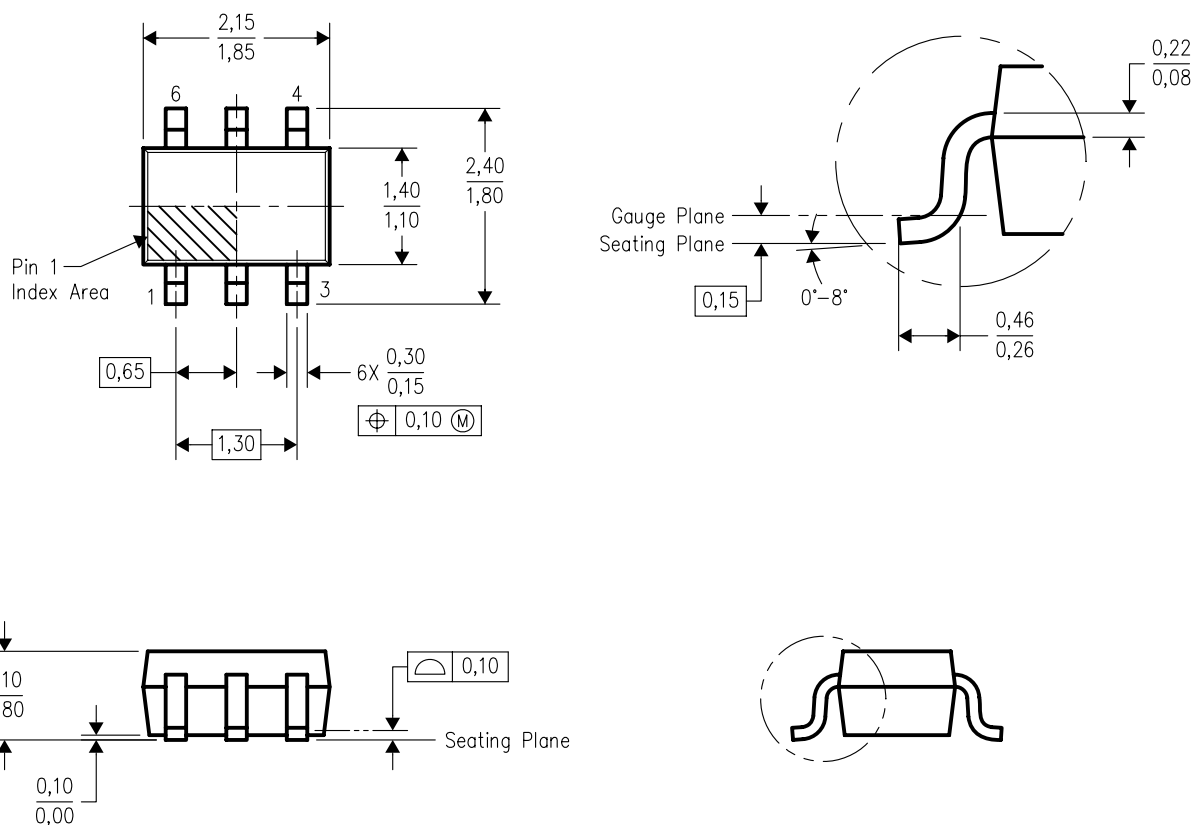


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1T45QDCKRQ1	SC70	DCK	6	3000	202.0	201.0	28.0
SN74LVC1T45TDCKRQ1	SC70	DCK	6	3000	202.0	201.0	28.0

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-4/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AB.

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