DELKIN DEVICES®

# COEM CFexpress

## Engineering Specification

**Document Number: 401-0546-00**

**Revision: A**

# Product Overview

- **Capacities**
  - 128GB & 256GB
- **Form Factor**
  - CFEXPRESS
- **PCIe Interface**
  - NVMe PCIe Gen 3 x 2
- **Compliance**
  - NVMe 1.3
  - PCI Express Base 3.1
- **Performance[1]**
  - Read: up to 1700 MB/s
  - Write: up to 1100 MB/s
- **Reliability**
  - Mean Time Between Failure (MTBF) More than 1.5 million hours
  - Uncorrectable Bit Error Rate (UBER) < 1 sector per 1016 bits read
- **Advanced Flash Management**
  - Static and Dynamic Wear Leveling
  - Bad Block Management
  - TRIM
  - SMART
  - Over-Provisioning
  - Firmware Update Capability
- **Power Management**
  - Support APST
  - Support ASPM
  - Support L1.2
- **Power Consumption[2]**
  - See table 4.2
- **Temperature Range[3]**
  - Operation: 0°C ~ 70°C
  - Storage: -40°C ~ 85°C
- **RoHS-Compliant**
- **Features Support List:**
  - End to end data path protection
  - Thermal throttling
  - LDPC + RAID ECC
  - SmartRefresh™
  - Drive log
  - Support of TCG OPAL[4]
  - Support of TCG Pyrite[5]

NOTES:

1. Refer to Chapter 2 Section 1.1 for more details
2. Refer to Chapter 4, Section 4.2 Power Consumption for more details.
3. The operation temperature means th e case temperature, in which can be decided via the S.M.A.R.T.
4. Supported by a separate firmware version. Further information available upon request.
5. Supported by a separate firmware version. Further information available upon request.

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# 1. INTRODUCTION

## 1.1. General Description

Delkin's CFexpress delivers all the advantages of flash disk technology with PCIe Gen3 x 2 interface. The CFexpress is available in the capacity range of 128GB & 256GB and can reach up to 1770 MB/s read, as well as 1100 MB/s write high performance. Its lower power consumption makes it an ideal storage choice for high performance embedded platforms.

## 1.2. Product Block Diagram

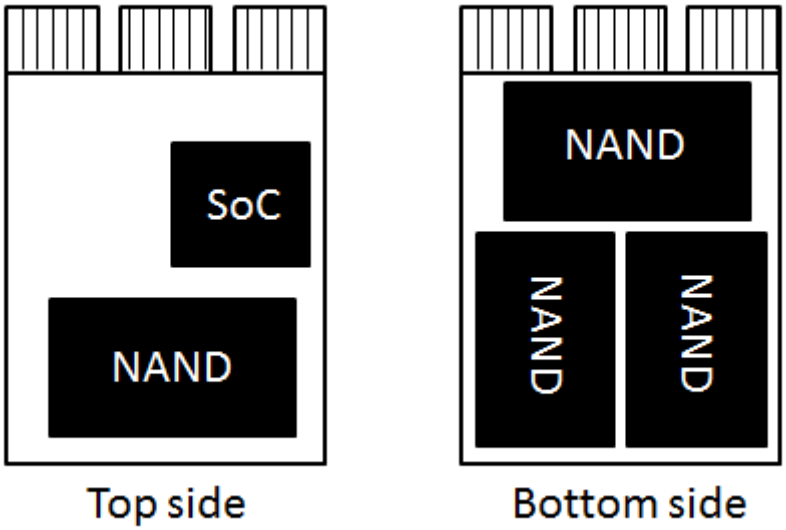



**Figure 1-1 CFexpress Product Block Diagram**

## 1.3. Flash Management

### 1.3.1. Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. However, Delkin's CFexpress PCIe SSD applies the LDPC (Low Density Parity Check) and RAID ECC algorithm,, which can detect and correct data errors to ensure data being read correctly, and protects data from corruption.

### 1.3.2. Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, when flash media is not used evenly, some blocks get updated more frequently than others and the lifetime of device would be reduced significantly. Thus, wear leveling is applied to extend the lifespan of NAND flash by evenly distributing write and erase cycles across the media.

Delkin provides advanced wear leveling algorithms, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static wear leveling algorithms, the life expectancy of the NAND flash is greatly improved.

### 1.3.3. Bad Block Management

Bad blocks are blocks that do not function properly or contain more invalid bits causing stored data unstable, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Delkin implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages bad blocks that appear with use. This practice prevents data being stored into bad blocks and further improves the data reliability.

### 1.3.4. TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD so that blocks of data that are no longer in use can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks at all time.

### 1.3.5. SMART

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a solid state drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users impending failures while there is still time to perform proactive actions, such as save data to another device.

### 1.3.6. Over-Provisioning

Over Provisioning refers to the inclusion of extra NAND capacity in a SSD, which is not visible to users nor usable by users. Therefore, it allows a SSD controller to utilize additional space for better performance and WAF. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

### 1.3.7. Firmware Upgrade

Firmware can be considered as a set of instructions on how the device communicates with the host. Firmware can be upgraded when new features are added, compatibility issues are fixed, or read/write performance gets improved.

### 1.3.8. Thermal Throttling

The purpose of thermal throttling is to prevent components in a SSD from over-heating during read and write operations. Delkin's CFexpress is designed with an on-die thermal sensor and with its accuracy, firmware can apply different levels of throttling to achieve the purpose of protection efficiently and proactively via SMART reading.

## 1.4. Advanced Device Security Features

#### 1.4.1. Secure Erase

Secure Erase is a standard NVMe format command and will write all "0xFF" to all cells, to fully wipe all the data on hard drives and SSDs. When this command is issued, SSD controller will erase its storage blocks and return to its factory default settings.

#### 1.4.2. Crypto Erase

Crypto Erase is a feature that erases all data of an OPAL-activated SSD or a "SED" (Security-Enabled Disk) drive by resetting the cryptographic key of the disk. Since the key is modified, the previously encrypted data will become useless, achieving the purpose of data security.

### 1.4.3. Physical Presence SID (PSID)

Physical Presence SID (PSID) is defined by TCG OPAL as a 32-character string and the purpose is to revert SSD back to its manufacturing setting when the drive is still OPAL-activated. PSID code can printed on a SSD label when an OPAL-activated SSD supports PSID revert feature.

## 1.5. SSD Lifetime Management

### 1.5.1. Terabytes Written (TBW)

TBW (Terabytes Written) is a measurement of SSDs' expected lifespan, which represents the amount of data written to the device. To calculate the TBW of a SSD, the following equation is applied:

***TBW = [(NAND Endurance) x (SSD Capacity)] / [WAF]***

NAND Endurance: NAND endurance refers to the P/E (Program/Erase) cycle rating of a NAND flash, per the manufacturer's specification.

SSD Capacity: The SSD capacity is the specific capacity in total of a SSD.

WAF: Write Amplification Factor (WAF) is a numerical value representing the ratio between the amount of data that a SSD controller writes to the flash and the amount of data that the host's flash controller writes. A better WAF, which is near 1, guarantees better endurance and lower frequency of data written to flash memory.

TBW in this document is based on JEDEC 218/219 workload.

### 1.5.2. Media Wear Indicator

Actual life indicator reported by SMART Attribute byte index [5], Percentage Used, recommends User to replace drive when reaching to 100%.

### 1.5.3. Read Only Mode (End of Life)

When a drive is aged by accumulated program/erase cycles, media worn-out may cause increasing numbers of later bad blocks. When the number of usable good blocks falls outside a defined usable range, the drive will notify the Host through AER event and Critical Warning to enter Read Only Mode to prevent further data corruption. This acts as notice to the user to replace the drive with another one immediately.

## 1.6. Adaptive Approach to Performance Tuning

### 1.6.1. Throughput

Based on the available space of the disk, Delkin's SSD will regulate the read/write speed and manage the throughput performance. When significant free space remains, the firmware will continuously perform read/write action. At this stage, there is still no need to implement garbage collection to allocate and release memory, which will accelerate the read/write process to improve the performance. However, when the free space is used up, the controller will slow down the read/write processing and implement garbage collection to release memory. Hence, read/write performance will become slower.

### 1.6.2. Predict & Fetch

Normally, when the Host tries to read data from the PCIe SSD, the PCIe SSD will only perform one read action after receiving one command. However, Delkin's controller applies ***Predict & Fetch*** to improve the read speed. When the host issues sequential read commands to the PCIe SSD, the PCIe SSD will automatically expect that the following will also be read commands. Thus, before receiving the next command, flash has already prepared the data. Accordingly, this accelerates the data processing time, and the host does not need to wait so long to receive data.

### 1.6.3. SLC Caching

Delkin's controller firmware design currently adopts dynamic caching to deliver better performance for better endurance and consumer user experience.

# 2. PRODUCT SPECIFICATIONS

- **Capacity**
  - 128GB & 256GB
  - Supports 32-bit addressing mode
- **Electrical/Physical Interface**
  - PCIe Interface
  - Compliant with NVMe 1.3
  - PCIe Express Base Ver 3.1
  - PCIe Gen 3 x 2 lane & backward compatible to PCIe Gen 2 and Gen 1
  - Support up to QD 128 with queue depth of up to 64K
  - Support power management
- **ECC Scheme**
  - Delkin CFexpress applies the LDPC (Low Density Parity Check) and RAID ECC algorithm
- **Sector Size Support**
  - 512B
  - 4KB
- **UART/ GPIO**
- **Supports SMART and TRIM commands**
- **LBA Range**
  - IDEMA standard

### 1.1. Performance

| Capacity | Sequential (CDM) | | Random (8GB Burst) | |
|---|---|---|---|---|
| | Read (MB/s) | Write (MB/s) | Read (KIOPS) | Write (KIOPS) |
| 128GB | 1550 | 1000 | 70K | 120K |
| 256GB | 1700 | 1100 | 150K | 250K |

NOTES:

1. Performance may differ according to flash configuration and platform.
2. Performance is measured with the following conditions
   (a) CrystalDiskMark 6.0, 1GB range, QD=32T1
   (b) IOMeter, 1GB range, 4K data size, QD=32T8
   (c) ATTO, transfer Size 64MB
3. OS Version: Win10 (64bit), version 1709

- Part Numbers

| Capacity | Operating Temperature |
|---|---|
| | Commercial (0 to 70˚C) |
| 128GB | CFXCOEM-128GB |
| 256GB | CFXCOEM-256GB |

# 3. ENVIRONMENTAL SPECIFICATIONS

## 3.1. Environmental Conditions

### 3.1.1. Temperature and Humidity

**Table 3-1 High Temperature**

| | Temperature | Humidity |
|---|---|---|
| **Operation** | 70°C | 0% RH |
| **Storage** | 85°C | 0% RH |

**Table 3-2 Low Temperature**

| | Temperature | Humidity |
|---|---|---|
| **Operation** | 0°C | 0% RH |
| **Storage** | -40°C | 0% RH |

**Table 3-3 High Humidity**

| | Temperature | Humidity |
|---|---|---|
| **Operation** | 40°C | 90% RH |
| **Storage** | 40°C | 93% RH |

**Table 3-4 Temperature Cycling**

| | Temperature |
|---|---|
| **Operation** | 0°C |
| | 70°C[1] |
| **Storage** | -40°C |
| | 85°C |

NOTES:

1. Operation temperature is measured by device temperature sensor. Airflow is suggested and it will allow device to be operated in at appropriate temperature for each component during heavy workload environments.

### 3.1.2. Shock

**Table 3-5 Shock**

| | Acceleration Force |
|---|---|
| **Non-operational** | 1500G |

### 3.1.3. Vibration

**Table 3-6 Vibration**

| | Condition | |
|---|---|---|
| | **Frequency/Displacement** | **Frequency/Acceleration** |
| **Non-operational** | 20Hz~80Hz/1.52mm | 80Hz~2000Hz/20G |

### 3.1.4. Drop

**Table 3-7 Drop**

| | Height of Drop | Number of Drop |
|---|---|---|
| **Non-operational** | 80cm free fall | 6 face of each unit |

### 3.1.5. Bending

**Table 3-8 Bending**

| | Force | Action |
|---|---|---|
| **Non-operational** | ≥ 20N | Hold 1min/5 times |

### 3.1.6. Torque

**Table 3-9 Torque**

| | Force | Action |
|---|---|---|
| **Non-operational** | 0.5N-m or ±2.5 deg | Hold 1min/5 times |

### 3.1.7. Electrostatic Discharge (ESD)

**Table 3-10 ESD**

| Specification | +/- 4KV |
|---|---|
| EN 55024, CISPR 24<br>EN 61000-4-2 and IEC 61000-4-2 | Device functions are affected, but EUT will be back to its normal or operational state automatically. |

### 3.1.8. EMI Compliance

**Table 3-11 EMI**

| Specification |
|---|
| EN 55032, CISPR 32(CE) |
| AS/NZS CISPR 32(CE) |
| ANSI C63.4 (FCC) |
| VCCI-CISPR 32 (VCCI) |
| CNS 13438 (BSMI) |

## 3.2. MTBF

MTBF, Mean Time Between Failures, is a measure of a device's reliability. Its value represents the average time between a repair and the next failure. The unit of MTBF is in hours. The higher the MTBF value, the higher the reliability of the device. The predicted result of Delkin's CFexpress is more than 1.5 million hours at 0°C.

Our MTBF result is based on Telcordia methodology. Please note that a lower MTBF should be expected for higher capacity drives, and we apply the lowest MTBF for all capacities.

## 3.3. Certification & Compliance

- RoHS
- WHQL
- PCI Express Base 3.1
- UNH-IOL NVM Express Logo

# 4. ELECTRICAL SPECIFICATIONS

## 4.1. Supply Voltage

**Table 4-1 Supply Voltage**

| Parameter | Rating |
|---|---|
| Operating Voltage | Min = 3.14V<br>Max = 3.47 V |
| Rise Time (Max/Min) | 100 ms / 0.1 ms |
| Fall Time (Max/Min) | 5s / 1 ms |
| Min. Off Time[1] | 1s |

NOTE:

1. Minimum time between power removed from SSD (Vcc < 100 mW) and power re-applied to the drive.

## 4.2. Power Consumption

**Table 4-2 Power Consumption in mW**

| Capacity | Read (Max) | Write (Max) | Read (Avg.) | Write (Avg.) |
|---|---|---|---|---|
| 128GB | 2310 | 1600 | 2290 | 1550 |
| 256GB | 2470 | 2320 | 2450 | 2260 |

NOTES:

1. Based on ambient temperature.
2. Use CrystalDiskMark 6.0 with the setting of 1000MB. Sequentially read and write the disk for 5 times, and measure power consumption during sequential Read [1/5]~[5/5] or sequential Write [1/5]~[5/5]
3. Power Consumption may differ according to flash configuration and platform.
4. The measured power voltage is 3.3V.

**Table 4-3 Power Consumption in mW**

| Capacity | Seq. Write | | | PS3 | PS4 |
|---|---|---|---|---|---|
| | PS0 | PS1 | PS2 | | |
| 128GB | 1550 | 1250 | 1140 | 30 | 5 |
| 256GB | 2260 | 1380 | 1200 | 30 | 5 |

NOTES:

1. Based on ambient temperature.
2. The average value of power consumption is achieved based on 100% conversion efficiency.
3. The measured power voltage is 3.3V.
4. The temperature of a storage device in PS1 should remain constant or should slightly decrease for all workloads so the actual power in PS1 should be lower than PS0.
5. The temperature of a storage device in PS2 should decrease sharply for all workloads so the actual power in PS2 should be lower than PS1.

Power Save Modes - PS0 Default Operational, PS1 Light Throttle, PS2 Heavy Throttle, PS3 Non-operational with fast recover, PS4 Lowest non-zero power state.

# 5. INTERFACE

## 5.1. Pin Assignment and Descriptions

Table 5-1 lists the pin assignment of the media.

The I/O column indicates the signal direction viewed from the media: “I” indicates the signal input to the media and “O” indicates the signal output from the media. In the Connection column, “R” indicates the signal is required, “Opt” indicates the signal is optional, and “NC” indicates the signal shall not be connected.

**Table 5-1 Pin Assignment and Description of CFexpress**

| Pin No. | Signal | I/O | Media | Host | Notes |
|---|---|---|---|---|---|
| 21 | GND | | R | R | |
| 20 | PETp0 | I | R | R | |
| 19 | PETn0 | I | R | R | |
| 18 | GND | | R | R | |
| 17 | PERp0 | O | R | R | |
| 16 | PERn0 | O | R | R | |
| 15 | GND | | R | R | |
| 14 | REFCLK+ | I | R | R | |
| 13 | REFCLK- | I | R | R | |
| 12 | INS# | O | R | R | 1 |
| 11 | CLKREQ# | O | R | Opt | 2 |
| 10 | +3.3V | | R | R | |
| 9 | PERST# | I | R | R | |
| 8 | Reserved | | NC | NC | |
| 7 | Reserved | | NC | NC | 4 |
| 6 | PETp1 | I | Opt | Opt | |
| 5 | PETn1 | I | Opt | Opt | |
| 4 | GND | | R | Opt | 3 |
| 3 | PERp1 | O | Opt | Opt | |
| 2 | PERn1 | O | Opt | Opt | |
| 1 | GND | | R | R | |

1. A host pull-up resistor in the range of 100kΩ-200kΩ is required on this pin.
2. A host pull-up resistor (≥5kΩ) is required on this pin.
3. If the PCI Express Transmitter differential pair Lane 1 and Receiver differential pair Lane 1 are implemented, this pin shall be connected to ground.
4. Note that this pin is assigned to USBEN in XQD specification.

**Table 5-2 Signal / Pin Descriptions of CFexpress**

| Category | Signal Name | Description |
|---|---|---|
| PCI Express | PETp0<br>PETn0<br>PERp0<br>PERn0<br>PETp1<br>PETn1<br>PERp1<br>PERn1 | PCI Express 8 GT/s two Lane. 2 transmitter differential pairs and 2 receiver differential pairs. |
| Auxiliary | REFCLK+<br>REFCLK- | PCI Express differential (and spread-spectrum) reference clock. |
| | PERST# | PCI Express functional reset. |
| | INS# | This signal is used for media detection and power control. |
| | CLKREQ# | This signal is used to indicate when REFCLK is needed for the PCI Express interface. |
| Power Source | +3.3V | 3.3V power |
| Ground | GND | Ground |

# 6. SUPPORTED COMMANDS

## 6.1. NVMe Command List

**Table 6-1 Admin Commands**

| Opcode | Command Description |
|---|---|
| 00h | Delete I/O Submission Queue |
| 01h | Create I/O Submission Queue |
| 02h | Get Log Page |
| 04h | Delete I/O Completion Queue |
| 05h | Create I/O Completion Queue |
| 06h | Identify |
| 08h | Abort |
| 09h | Set Features |
| 0Ah | Get Features |
| 0Ch | Asynchronous Event Request |
| 10h | Firmware Activate |
| 11h | Firmware Image Download |

**Table 6-2 Admin Commands – NVM Command Set Specific**

| Opcode | Command Description |
|---|---|
| 80h | Format NVM |
| 81h | Security Send |
| 82h | Security Receive |

**Table 6-3 NVM Commands**

| Opcode | Command Description |
|---|---|
| 00h | Flush |
| 01h | Write |
| 02h | Read |
| 04h | Write Uncorrectable |
| 08h | Write Zeroes |
| 09h | Dataset Management |

## 6.2. Identify Device Data

The following table details the sector data returned by the IDENTIFY DEVICE command.

**Table 6-4 Identify Controller Data Structure**

| Bytes | O/M | Description | Default Value |
|---|---|---|---|
| 01:00 | M | PCI Vendor ID (VID) | 0x1E33 |
| 03:02 | M | PCI Subsystem Vendor ID (SSVID) | 0x1E33 |
| 23:04 | M | Serial Number (SN) | SN |
| 63:24 | M | Model Number (MN) | Model Number |
| 71:64 | M | Firmware Revision (FR) | FW Name |
| 72 | M | Recommended Arbitration Burst (RAB) | 0x01 |
| 75:73 | M | IEEE OUI Identifier (IEEE) | 0x000000 |
| 76 | O | Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC) | 0x00 |
| 77 | M | Maximum Data Transfer Size (MDTS) | 0x09 |
| 79:78 | M | Controller ID (CNTLID) | 0x0000 |
| 83:80 | M | Version (VER) | 0x00010300 |
| 87:84 | M | RTD3 Resume Latency (RTD3R) | TBD |
| 91:88 | M | RTD3 Entry Latency (RTD3E) | TBD |
| 95:92 | M | Optional Asynchronous Events Supported (OAES) | 0x00000100 |
| 99:96 | M | Controller Attributes (CTRATT) | 0x00000002 |
| 111:100 | | Reserved | 0x00 |
| 127:112 | | FRU Globally Unique Identifier (FGUID) | 0x00 |
| 239:128 | - | Reserved | 0x00 |
| 255:240 | - | Refer to the NVMe Management Interface Specification for definition | 0 |
| 257:256 | M | Optional Admin Command Support (OACS) | 0x0017 |
| 258 | M | Abort Command Limit (ACL) | 0x00 |
| 259 | M | Asynchronous Event Request Limit (AERL) | 0x03 |
| 260 | M | Firmware Updates (FRMW) | 0x12 (TBD) |
| 261 | M | Log Page Attributes (LPA) | 0x06 |
| 262 | M | Error Log Page Entries (ELPE) | 0x0F |
| 263 | M | Number of Power States Support (NPSS) | 0x04 |
| 264 | M | Admin Vendor Specific Command Configuration (AVSCC) | 0x01 |
| 265 | O | Autonomous Power State Transition Attributes (APSTA) | 0x01 |
| 267:266 | M | Warning Composite Temperature Threshold (WCTEMP) | (TBD) |
| 269:268 | M | Critical Composite Temperature Threshold (CCTEMP) | (TBD) |
| 271:270 | O | Maximum Time for Firmware Activation (MTFA) | 0x0000 |

| | | | |
|---|---|---|---|
| 275:272 | O | Host Memory Buffer Preferred Size (HMPRE) | (TBD) |
| 279:276 | O | Host Memory Buffer Minimum Size (HMMIN) | (TBD) |
| 295:280 | O | Total NVM Capacity (TNVMCAP) | non-zero |
| 311:296 | O | Unallocated NVM Capacity (UNVMCAP) | 0 |
| 315:312 | O | Replay Protected Memory Block Support (RPMBS) | (TBD) |
| 317:316 | O | Extended Device Self test Time (EDSTT) | 0x001E |
| 318 | O | Device Self test Options (DSTO) | 0x01 |
| 319 | M | Firmware Update Granularity (FWUG) | 0x1 |
| 321:320 | M | Keep Alive Support (KAS) | 0x0001 |
| 323:322 | O | Host Controlled Thermal Management Attributes (HCTMA) | 1 |
| 325:324 | O | Minimum Thermal Management Temperature (MNTMT) | (TBD) |
| 327:326 | O | Maximum Thermal Management Temperature (MXTMT) | (TBD) |
| 331:328 | O | Sanitize Capabilities (SANICAP) | 0x00000006 |
| 511:316 | - | Reserved | 0x0 |
| **NVM Command Set Attributes** | | | |
| 512 | M | Submission Queue Entry Size (SQES) | 0x66 |
| 513 | M | Completion Queue Entry Size (CQES) | 0x44 |
| 515:514 | - | Reserved | 0x0080 |
| 519:516 | M | Number of Namespaces (NN) | 0x00000001 |
| 521:520 | M | Optional NVM Command Support (ONCS) | 0x005F |
| 523:522 | M | Fused Operation Support (FUSES) | 0 |
| 524 | M | Format NVM Attributes (FNA) | 0x01 |
| 525 | M | Volatile Write Cache (VWC) | 0x01 |
| 527:526 | M | Atomic Write Unit Normal (AWUN) | 0x00FF |
| 529:528 | M | Atomic Write Unit Power Fail (AWUPF) | 0x0000 |
| 530 | M | NVM Vendor Specific Command Configuration (NVSCC) | 0x01 |
| 531 | M | Reserved | 0x00 |
| 533:532 | O | Atomic Compare & Write Unit (ACWU) | 0x0000 |
| 535:534 | M | Reserved | 0x0000 |
| 539:536 | O | SGL Support (SGLS) | 0x00000000 |
| 767:540 | M | Reserved | 0x0 |
| **IO Command Set Attributes** | | | |
| 2047:704 | M | Reserved | 0x0 |
| 2078:2048 | M | Power State 0 Descriptor | (TBD) |
| 2111:2080 | O | Power State 1 Descriptor | (TBD) |
| 2143:2112 | O | Power State 2 Descriptor | (TBD) |
| 2175:2144 | O | Power State 3 Descriptor | (TBD) |
| 2207:2176 | O | Power State 4 Descriptor | (TBD) |

| | | | |
|---|---|---|---|
| … | - | (N/A) | 0 |
| 3071:3040 | O | Power State 31 Descriptor | (TBD) |
| **Vendor Specific** | | | |
| 4095:3072 | O | Vendor Specific (VS) | Reserved |

**Table 6-5 Identify Namespace Data Structure & NVM Command Set Specific**

| Bytes | Description |
|---|---|
| 7:0 | Namespace Size (NSZE) |
| 15:8 | Namespace Capacity (NCAP) |
| 23:16 | Namespace Utilization (NUSE) |
| 24 | Namespace Features (NSFEAT) |
| 25 | Number of LBA Formats (NLBAF) |
| 26 | Formatted LBA Size (FLBAS) |
| 27 | Metadata Capabilities (MC) |
| 28 | End-to-end Data Protection Capabilities (DPC) |
| 29 | End-to-end Data Protection Type Settings (DPS) |
| 30 | Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC) |
| 31 | Reservation Capabilities (RESCAP) |
| 32 | Format Progress Indicator (FPI) |
| 33 | Deallocate Logical Block Features (DLFEAT) |
| 35:34 | Namespace Atomic Write Unit Normal (NAWUN) |
| 37:36 | Namespace Atomic Write Unit Power Fail (NAWUPF) |
| 39:38 | Namespace Atomic Compare & Write Unit (NAWWU) |
| 41:40 | Namespace Atomic Boundary Size Normal (NABSN) |
| 43:42 | Namespace Atomic Boundary Offset (NABO) |
| 45:44 | Namespace Atomic Boundary Size Power Fail (NABSPF) |
| 47:46 | Namespace Atomic Optimal IO Boundary (NOIOB) |
| 63:48 | NVM Capacity (NVMCAP) |
| 103:64 | Reserved |
| 119:104 | Namespace Globally Unique Identifier (NGUID) |
| 127:120 | IEEE Extended Unique Identifier (EUI64) |
| 131:128 | LBA Format 0 Support (LBAF0) |
| 135:132 | LBA Format 1 Support (LBAF1) |
| 139:136 | LBA Format 2 Support (LBAF2) |
| 143:140 | LBA Format 3 Support (LBAF3) |
| 147:144 | LBA Format 4 Support (LBAF4) |
| 151:148 | LBA Format 5 Support (LBAF5) |
| 155:152 | LBA Format 6 Support (LBAF6) |
| 159:156 | LBA Format 7 Support (LBAF7) |
| 163:160 | LBA Format 8 Support (LBAF8) |
| 167:164 | LBA Format 9 Support (LBAF9) |
| 171:168 | LBA Format 10 Support (LBAF10) |
| 175:172 | LBA Format 11 Support (LBAF11) |

| | |
|---|---|
| 179:176 | LBA Format 12 Support (LBAF12) |
| 183:180 | LBA Format 13 Support (LBAF13) |
| 187:184 | LBA Format 14 Support (LBAF14) |
| 191:188 | LBA Format 15 Support (LBAF15) |
| 383:192 | Reserved |
| 4095:384 | Vendor Specific (VS) |

**Table 6-6 List of Identify Namespace Data Structure for Each Capacity**

| **Capacity (GB)** | **Byte[7:0]: Namespace Size (NSZE)** |
|---|---|
| 128 | EE7C2B0 |
| 256 | 1DCF32B0 |

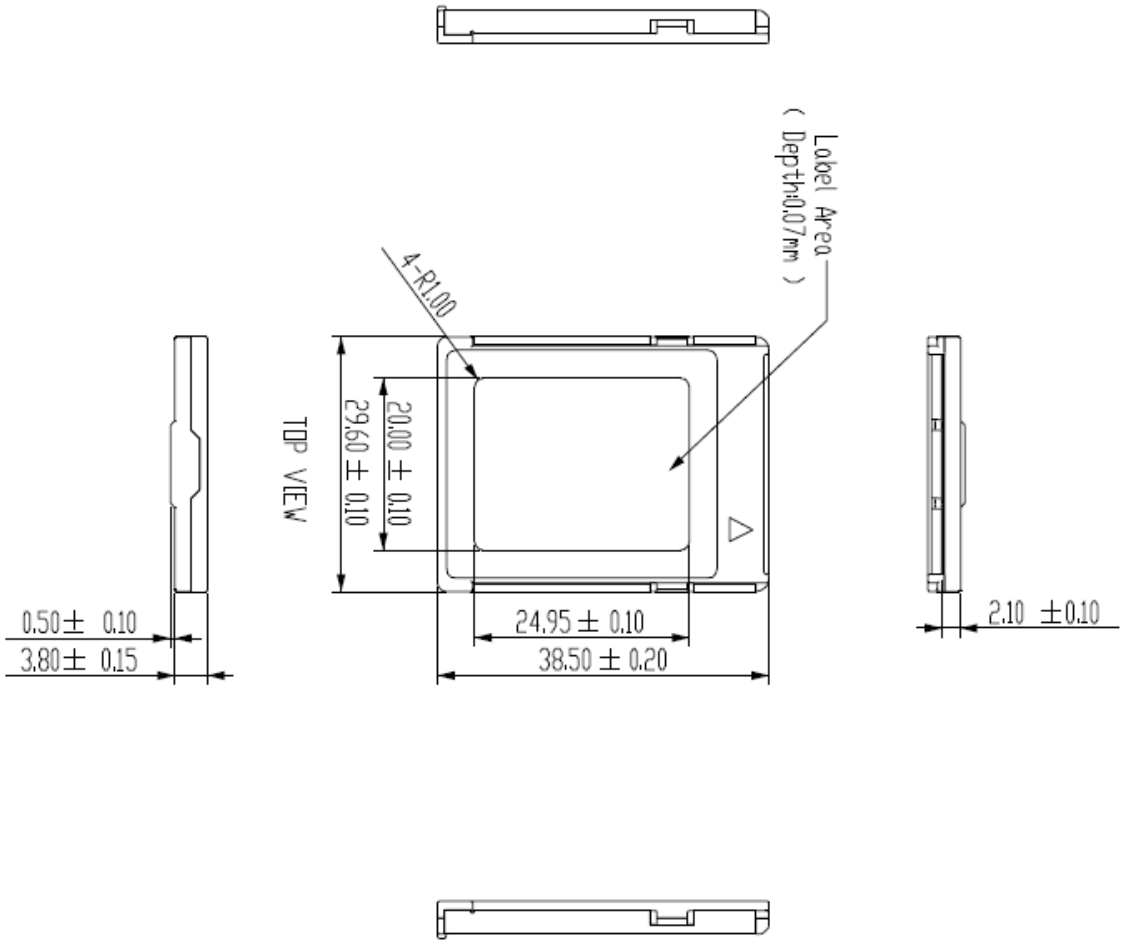
## 6.3. SMART Attributes

**Table 6-7 SMART Attributes (Log Identifier 02h)**

| Bytes Index | Bytes | Description |
|---|---|---|
| [0] | 1 | Critical Warning |
| [2:1] | 2 | Composite Temperature |
| [3] | 1 | Available Spare |
| [4] | 1 | Available Spare Threshold |
| [5] | 1 | Percentage Used |
| [31:6] | 26 | Reserved |
| [47:32] | 16 | Data Units Read |
| [63:48] | 16 | Data Units Written |
| [79:64] | 16 | Host Read Commands |
| [95:80] | 16 | Host Write Commands |
| [111:96] | 16 | Controller Busy Time |
| [127:112] | 16 | Power Cycles |
| [143:128] | 16 | Power On Hours |
| [159:144] | 16 | Unsafe Shutdowns |
| [175:160] | 16 | Media and Data Integrity Errors |
| [191:176] | 16 | Number of Error Information Log Entries |
| [195:192] | 4 | Warning Composite Temperature Time |
| [199:196] | 4 | Critical Composite Temperature Time |
| [201:200] | 2 | Temperature Sensor 1 |
| [203:202] | 2 | Temperature Sensor 2 |
| [205:204] | 2 | Temperature Sensor 3 |
| [207:206] | 2 | Temperature Sensor 4 |

# 7. PHYSICAL DIMENSION

CFexpress : 38.50mm (L) x 29.60mm (W) x 3.8mm (H)




**WARNING: This product may contain chemicals known to the State of California to cause cancer, birth defects, or other reproductive harm. For more information go to www.p65warnings.ca.gov.**