

74HC173; 74HCT173

Quad D-type flip-flop; positive-edge trigger; 3-state

Rev. 3 — 8 November 2016

Product data sheet

1. General description

The 74HC173; 74HCT173 is a quad positive-edge triggered D-type flip-flop. The device features clock (CP), master reset (MR), two input enable ($\overline{E1}$, $\overline{E2}$) and two output enable ($\overline{OE1}$, $\overline{OE2}$) inputs. When the input enables are LOW, the outputs Qn will assume the state of their corresponding Dn inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A HIGH on either input enable will cause the device to go into a hold mode, outputs hold their previous state independently of clock and data inputs. A HIGH on MR forces the outputs LOW independently of clock and data inputs. A HIGH on either output enable pin causes the outputs to assume a high-impedance OFF-state. Operation of the output enable inputs does not affect the state of the flip-flops. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

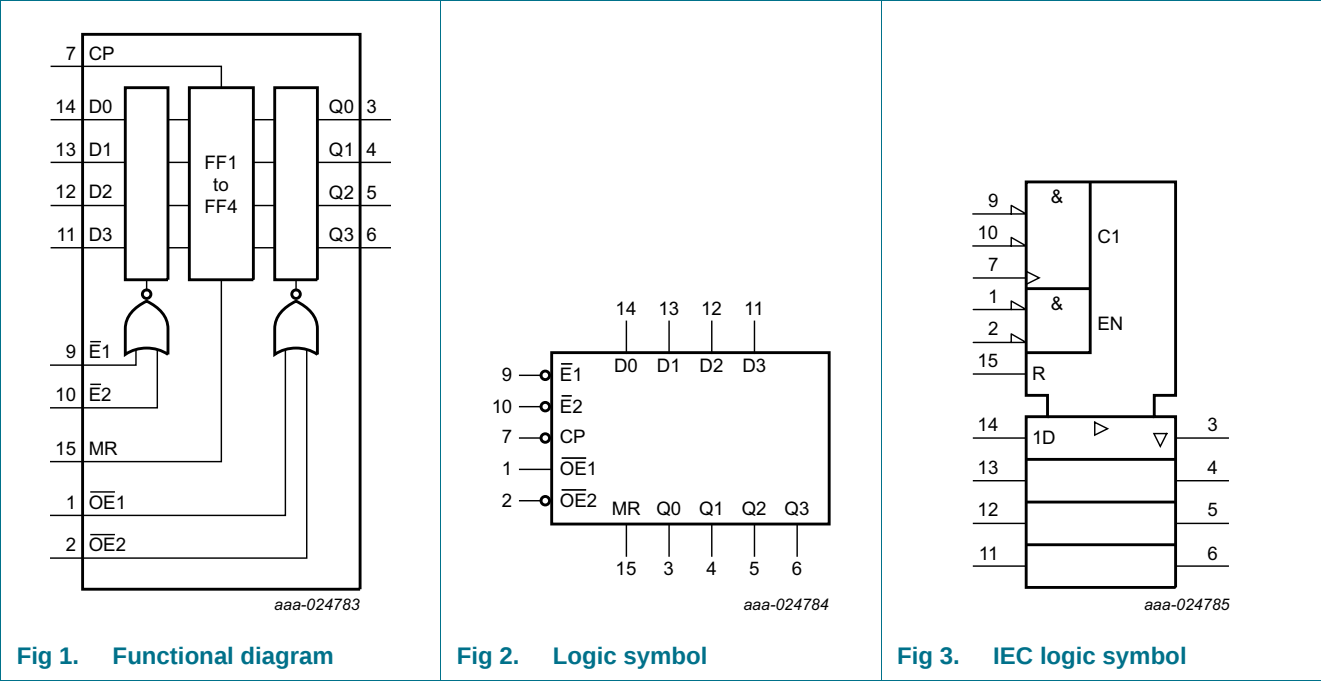
- Complies with JEDEC standard no. 7A
- Input levels:
 - ◆ For 74HC173: CMOS level
 - ◆ For 74HCT173: TTL level
- Gated input enable for hold (do nothing) mode
- Gated output enable control mode
- Edge-triggered D-type register
- Asynchronous master reset
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

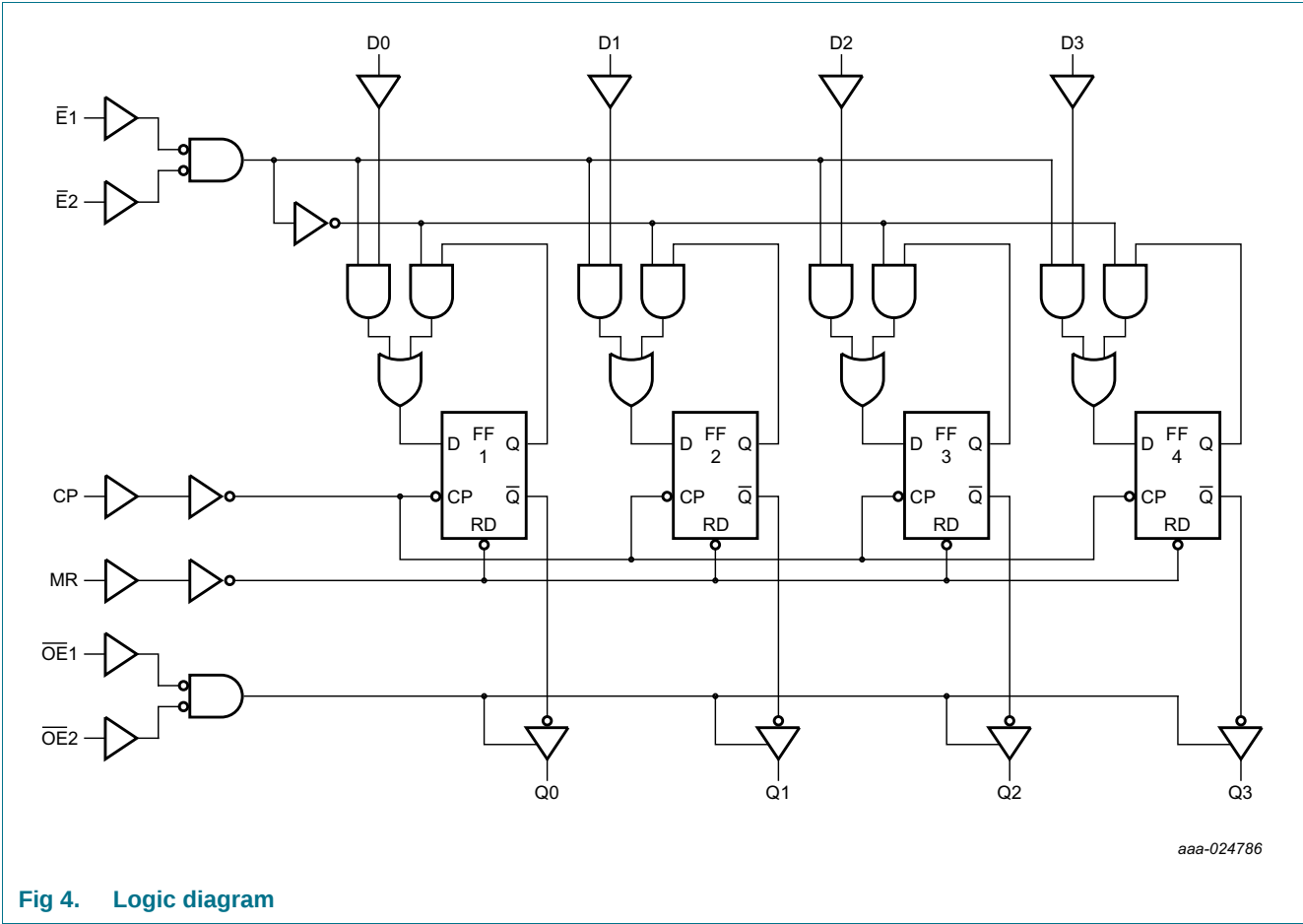
3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC173D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT173D				
74HC173DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT173DB				
74HC173PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

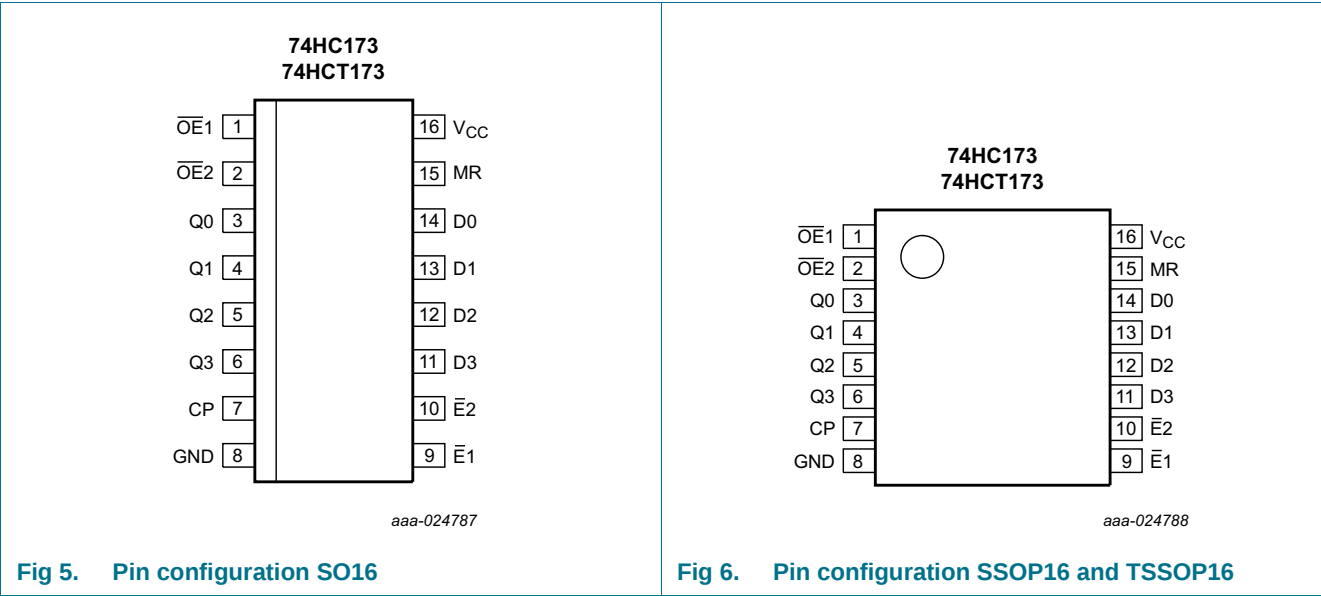
4. Functional diagram





5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}1, \overline{OE}2$	1, 2	output enable input (active LOW)
Q0, Q1, Q2, Q3	3, 4, 5, 6	3-state flip-flop output
CP	7	clock input (LOW-to-HIGH, edge triggered)
GND	8	ground (0 V)
$\overline{E}1, \overline{E}2$	9, 10	data enable input (active LOW)
D0, D1, D2, D3	14, 13, 12, 11	data input
MR	15	asynchronous master reset (active HIGH)
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table^[1]

Register operating mode	Inputs					Outputs
	MR	CP	$\overline{E1}$	$\overline{E2}$	Dn	Qn (register)
Reset (clear)	H	X	X	X	X	L
Parallel load	L	↑	L	L	L	L
	L	↑	L	L	h	H
Hold (do nothing)	L	X	h	X	X	q _n
	L	X	X	h	X	q _n

Table 4. Function table^[1]

3-state buffer operating mode	Inputs			Outputs			
	Qn (register)	$\overline{OE1}$	$\overline{OE2}$	Q0	Q1	Q2	Q3
Read	L	L	L	L	L	L	L
	H	L	L	H	H	H	H
Disabled	X	H	X	Z	Z	Z	Z
	X	X	H	Z	Z	Z	Z

- [1] H = HIGH voltage level;
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
 L = LOW voltage level;
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
 q_n = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CP transition;
 X = don't care;
 Z = high impedance OFF-state;
 ↑ = LOW-to-HIGH clock transition.

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		−0.5	+7.0	V
I _{IK}	input clamping current	V _I < −0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output clamping current	V _O < −0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	−0.5 V < V _O < V _{CC} + 0.5 V	-	±35	mA
I _{CC}	supply current		-	+70	mA
I _{GND}	ground current		−70	-	mA
T _{stg}	storage temperature		−65	+150	°C
P _{tot}	total power dissipation	SO16 and (T)SSOP16 package ^[1]	-	500	mW

- [1] For SO16 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.
 For (T)SSOP16 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.

8. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC173			74HCT173			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC173										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = −20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = −20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = −20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = −6.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = −7.8 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 6.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 7.8 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 6.0 V; V _O = V _{CC} or GND	-	-	±0.5	-	±5.0	-	±10	μA

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	8	-	80	-	160	μ A
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT173										
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5$ V								
		$I_O = -20$ μ A	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -6.0$ mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5$ V								
		$I_O = 20$ μ A	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 6.0$ mA	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	± 0.1	-	± 1.0	-	± 1.0	μ A
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND	-	-	± 0.5	-	± 5.0	-	± 10	μ A
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V; $I_O = 0$ A	-	-	8.0	-	80	-	160	μ A
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; $V_{CC} = 4.5$ V to 5.5 V; $I_O = 0$ A								
		$\overline{OE}1, \overline{OE}2$	-	50	180	-	225	-	245	μ A
		MR	-	60	216	-	270	-	294	μ A
		$\overline{E}1, \overline{E}2$	-	40	144	-	180	-	196	μ A
		Dn	-	25	90	-	112.5	-	122.5	μ A
		CP	-	100	360	-	450	-	490	μ A
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 11](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC173										
t _{pd}	propagation delay	CP to Qn; see Figure 7 [1]								
		V _{CC} = 2.0 V	-	55	175	-	220	-	265	ns
		V _{CC} = 4.5 V	-	20	35	-	44	-	53	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	17	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	16	30	-	37	-	45	ns
t _{PHL}	High to LOW propagation delay	MR to Qn; see Figure 8								
		V _{CC} = 2.0 V	-	44	150	-	190	-	225	ns
		V _{CC} = 4.5 V	-	16	30	-	38	-	45	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	13	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	13	26	-	33	-	38	ns
t _{en}	enable time	$\overline{OEn}$ to Qn; see Figure 9 [2]								
		V _{CC} = 2.0 V	-	52	150	-	190	-	225	ns
		V _{CC} = 4.5 V	-	19	30	-	38	-	45	ns
		V _{CC} = 6.0 V	-	15	26	-	33	-	38	ns
t _{dis}	disable time	$\overline{OEn}$ to Qn; see Figure 9 [3]								
		V _{CC} = 2.0 V	-	52	150	-	190	-	225	ns
		V _{CC} = 4.5 V	-	19	30	-	38	-	45	ns
		V _{CC} = 6.0 V	-	15	26	-	33	-	38	ns
t _t	transition time	see Figure 7 [4]								
		V _{CC} = 2.0 V	-	14	60	-	75	-	90	ns
		V _{CC} = 4.5 V	-	5	12	-	15	-	18	ns
		V _{CC} = 6.0 V	-	4	10	-	13	-	15	ns
t _w	pulse width	CP HIGH or LOW; see Figure 7								
		V _{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	4	-	17	-	20	-	ns
		MR HIGH; see Figure 8								
		V _{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	4	-	17	-	20	-	ns
t _{rec}	recovery time	MR to CP; see Figure 8								
		V _{CC} = 2.0 V	60	–8	-	75	-	90	-	ns
		V _{CC} = 4.5 V	12	–3	-	15	-	18	-	ns
		V _{CC} = 6.0 V	10	–2	-	13	-	15	-	ns

Table 8. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 11](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{su}	set-up time	$\overline{En}$ to CP; see Figure 10								
		$V_{CC} = 2.0$ V	100	33	-	125	-	150	-	ns
		$V_{CC} = 4.5$ V	20	12	-	25	-	30	-	ns
		$V_{CC} = 6.0$ V	17	10	-	21	-	26	-	ns
		Dn to CP; see Figure 10								
		$V_{CC} = 2.0$ V	60	17	-	75	-	90	-	ns
		$V_{CC} = 4.5$ V	12	6	-	15	-	18	-	ns
		$V_{CC} = 6.0$ V	10	5	-	13	-	15	-	ns
t_h	hold time	$\overline{En}$ to CP; see Figure 10								
		$V_{CC} = 2.0$ V	0	–17	-	0	-	0	-	ns
		$V_{CC} = 4.5$ V	0	–6	-	0	-	0	-	ns
		$V_{CC} = 6.0$ V	0	–5	-	0	-	0	-	ns
		Dn to CP; see Figure 10								
		$V_{CC} = 2.0$ V	1	–11	-	1	-	1	-	ns
		$V_{CC} = 4.5$ V	1	–4	-	1	-	1	-	ns
		$V_{CC} = 6.0$ V	1	–3	-	1	-	1	-	ns
f_{max}	maximum frequency	CP; see Figure 7								
		$V_{CC} = 2.0$ V	6	26	-	4.8	-	4	-	MHz
		$V_{CC} = 4.5$ V	30	80	-	24	-	20	-	MHz
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	88	-	-	-	-	-	MHz
		$V_{CC} = 6.0$ V	35	95	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$; $V_{CC} = 5$ V; $f_i = 1$ MHz [5]	-	20	-	-	-	-	-	pF
74HCT173										
t_{pd}	propagation delay	CP to Qn; see Figure 7 [1]								
		$V_{CC} = 4.5$ V	-	20	40	-	50	-	60	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	17	-	-	-	-	-	ns
t_{PHL}	High to LOW propagation delay	MR to Qn; see Figure 8								
		$V_{CC} = 4.5$ V	-	20	37	-	46	-	56	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	17	-	-	-	-	-	ns
t_{en}	enable time	$\overline{OEn}$ to Qn; $V_{CC} = 4.5$ V; see Figure 9 [2]	-	20	35	-	44	-	53	ns
t_{dis}	disable time	$\overline{OEn}$ to Qn; $V_{CC} = 4.5$ V; see Figure 9 [3]	-	19	30	-	38	-	45	ns
t_t	transition time	$V_{CC} = 4.5$ V; see Figure 7 [4]	-	5	12	-	15	-	19	ns
t_W	pulse width	CP HIGH or LOW; $V_{CC} = 4.5$ V; see Figure 7	16	7	-	20	-	24	-	ns
		MR HIGH; $V_{CC} = 4.5$ V; see Figure 8	15	6	-	19	-	22	-	ns

Table 8. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 11](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{rec}	recovery time	MR to CP; $V_{\text{CC}} = 4.5$ V; see Figure 8	12	–2	–	15	–	18	–	ns
t_{su}	set-up time	$\overline{\text{En}}$ to CP; $V_{\text{CC}} = 4.5$ V; see Figure 10	22	13	–	28	–	33	–	ns
		Dn to CP; $V_{\text{CC}} = 4.5$ V; see Figure 10	12	7	–	15	–	18	–	ns
t_{h}	hold time	$\overline{\text{En}}$ to CP; $V_{\text{CC}} = 4.5$ V; see Figure 10	0	–6	–	0	–	0	–	ns
		Dn to CP; $V_{\text{CC}} = 4.5$ V; see Figure 10	0	–3	–	0	–	0	–	ns
f_{max}	maximum frequency	CP; see Figure 7								
		$V_{\text{CC}} = 4.5$ V	30	80	–	24	–	20	–	MHz
		$V_{\text{CC}} = 5.0$ V; $C_L = 15$ pF	–	88	–	–	–	–	–	MHz
C_{PD}	power dissipation capacitance	$V_I = \text{GND}$ to $V_{\text{CC}} - 1.5$ V; $V_{\text{CC}} = 5$ V; $f_i = 1$ MHz	5	20	–	–	–	–	–	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH} .

[2] t_{en} is the same as t_{PZH} and t_{PZL} .

[3] t_{dis} is the same as t_{PHZ} and t_{PLZ} .

[4] t_t is the same as t_{THL} and t_{TLH} .

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{\text{PD}} \times V_{\text{CC}}^2 \times f_i \times N + \Sigma(C_L \times V_{\text{CC}}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

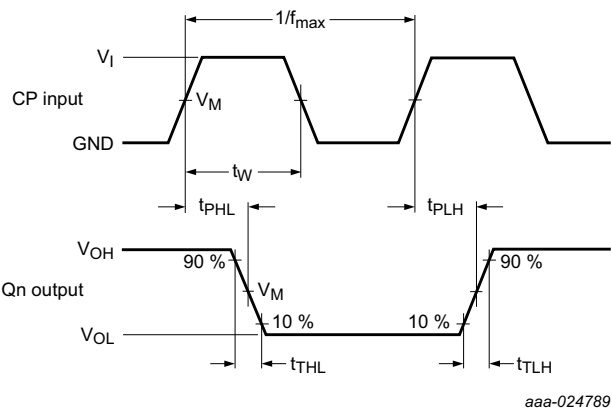
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

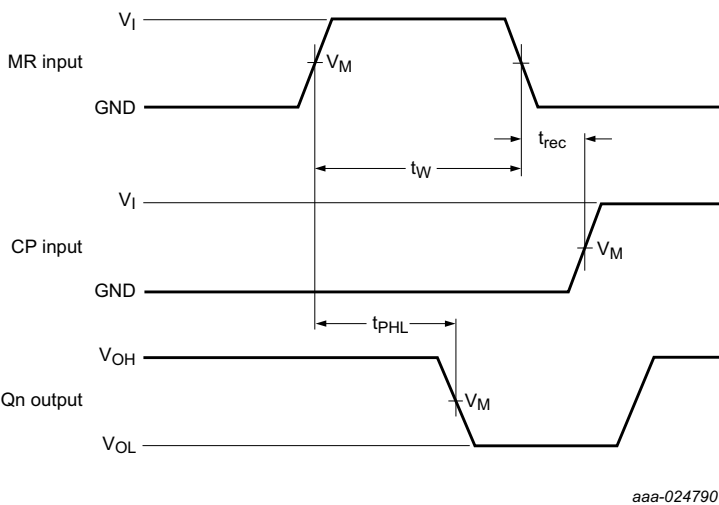
$\Sigma(C_L \times V_{\text{CC}}^2 \times f_o)$ = sum of outputs.

11. Waveforms



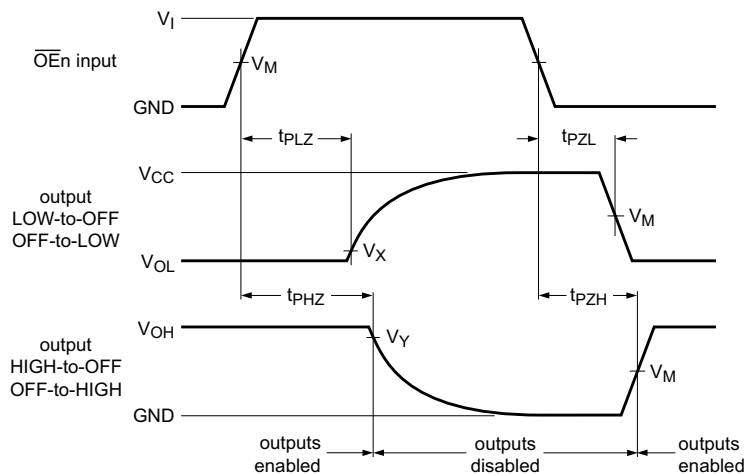
Measurement points are given in [Table 9](#).
Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. The clock (CP) to outputs (Qn) propagation delays, clock pulse width, output transition times and maximum frequency



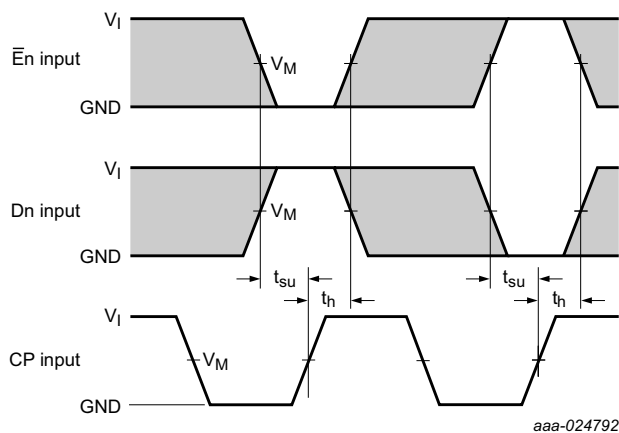
Measurement points are given in [Table 9](#).
Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. The master reset (MR) pulse width, master reset to output (Qn) propagation delays, and the master reset to clock (CP) recovery times



Measurement points are given in [Table 9](#).
Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 9. 3-state enable and disable times



The shaded areas indicate when the input is permitted to change for predictable output performance.
Measurement points are given in [Table 9](#).

Fig 10. The data set-up and hold times from input ($\bar{E}n$, Dn) to clock (CP)

Table 9. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC173	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$
74HCT173	1.3 V	1.3 V	$0.1 \times V_{CC}$	$0.9 \times V_{CC}$

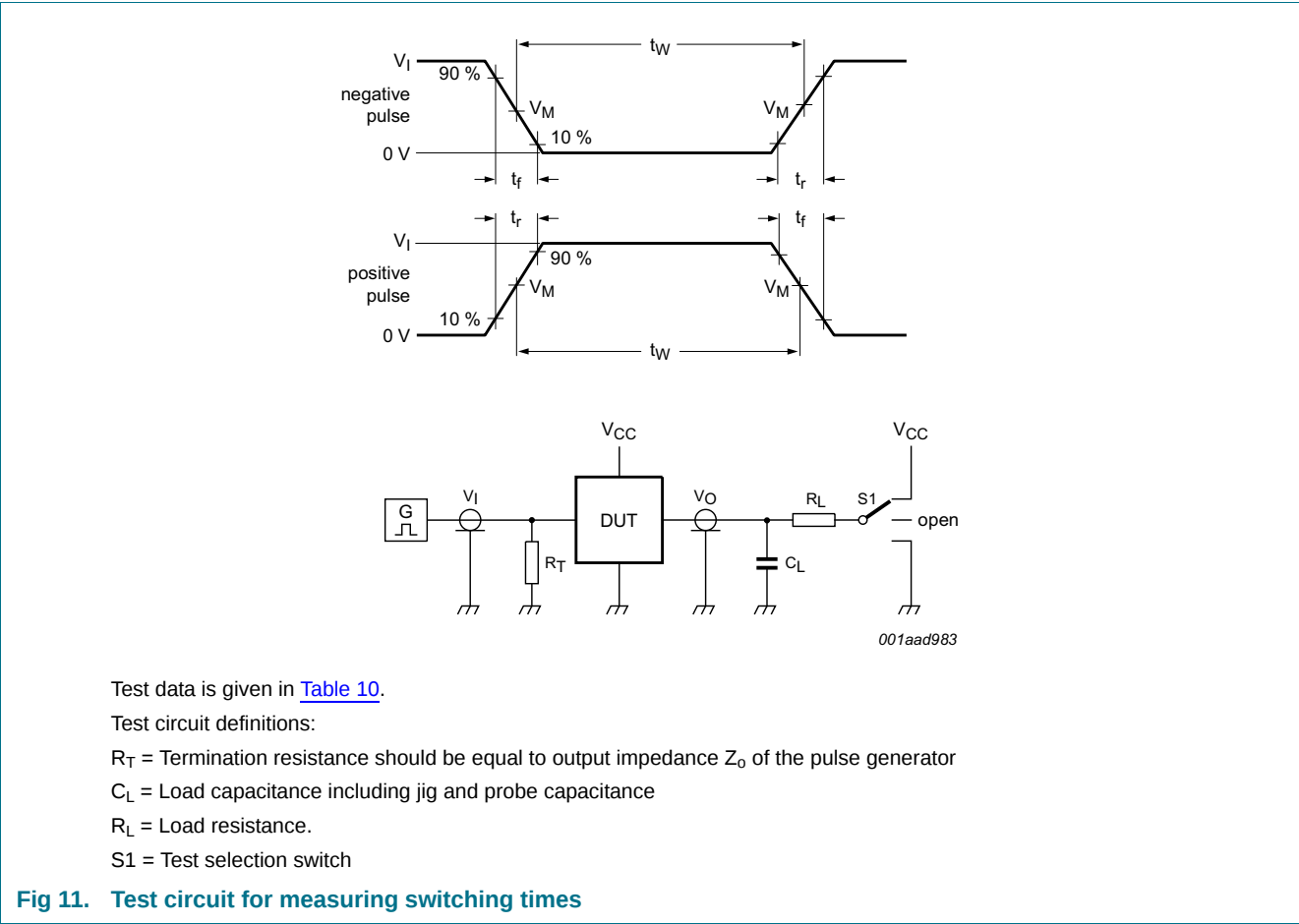


Table 10. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC173	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74HCT173	3 V	6 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

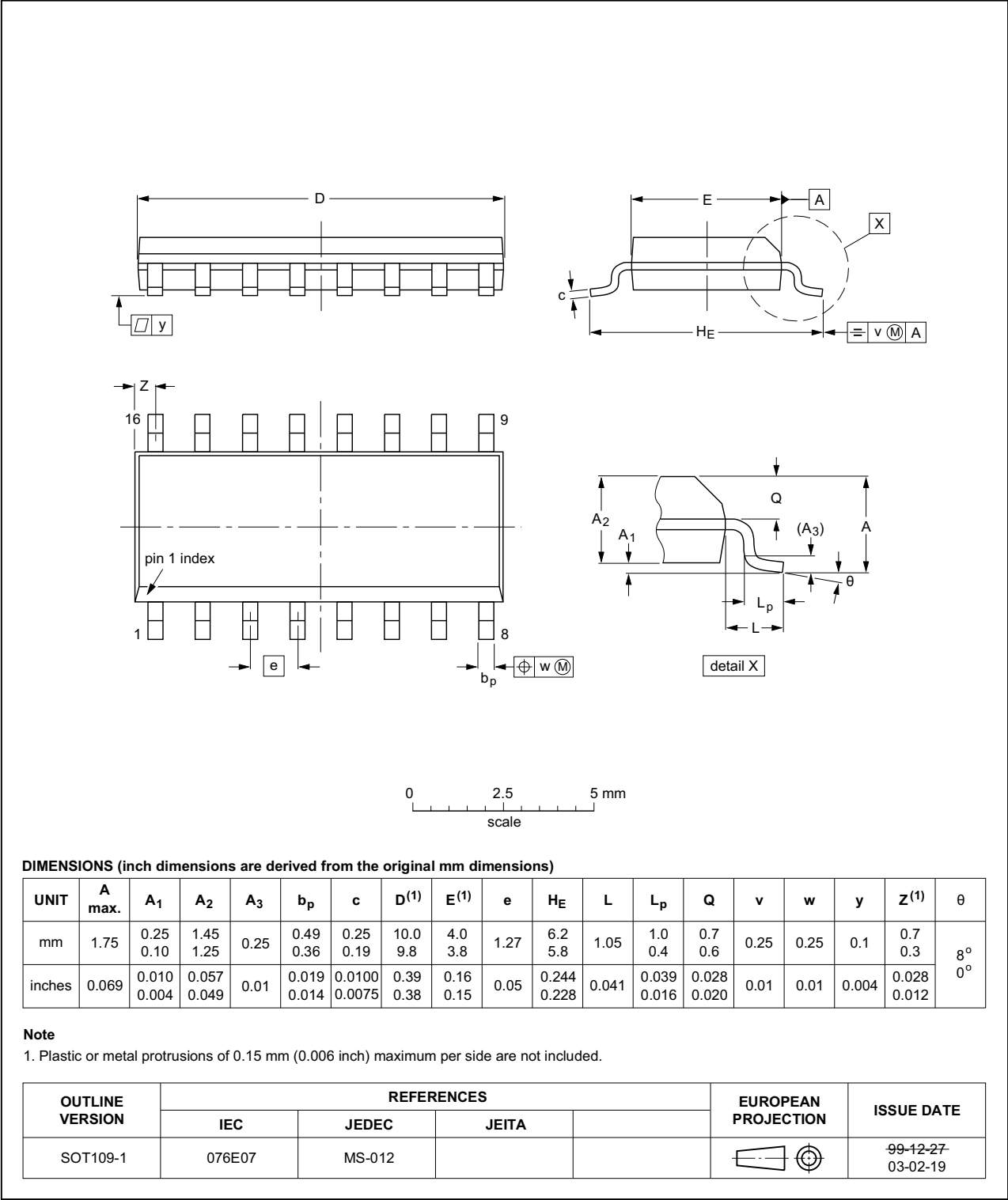


Fig 12. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

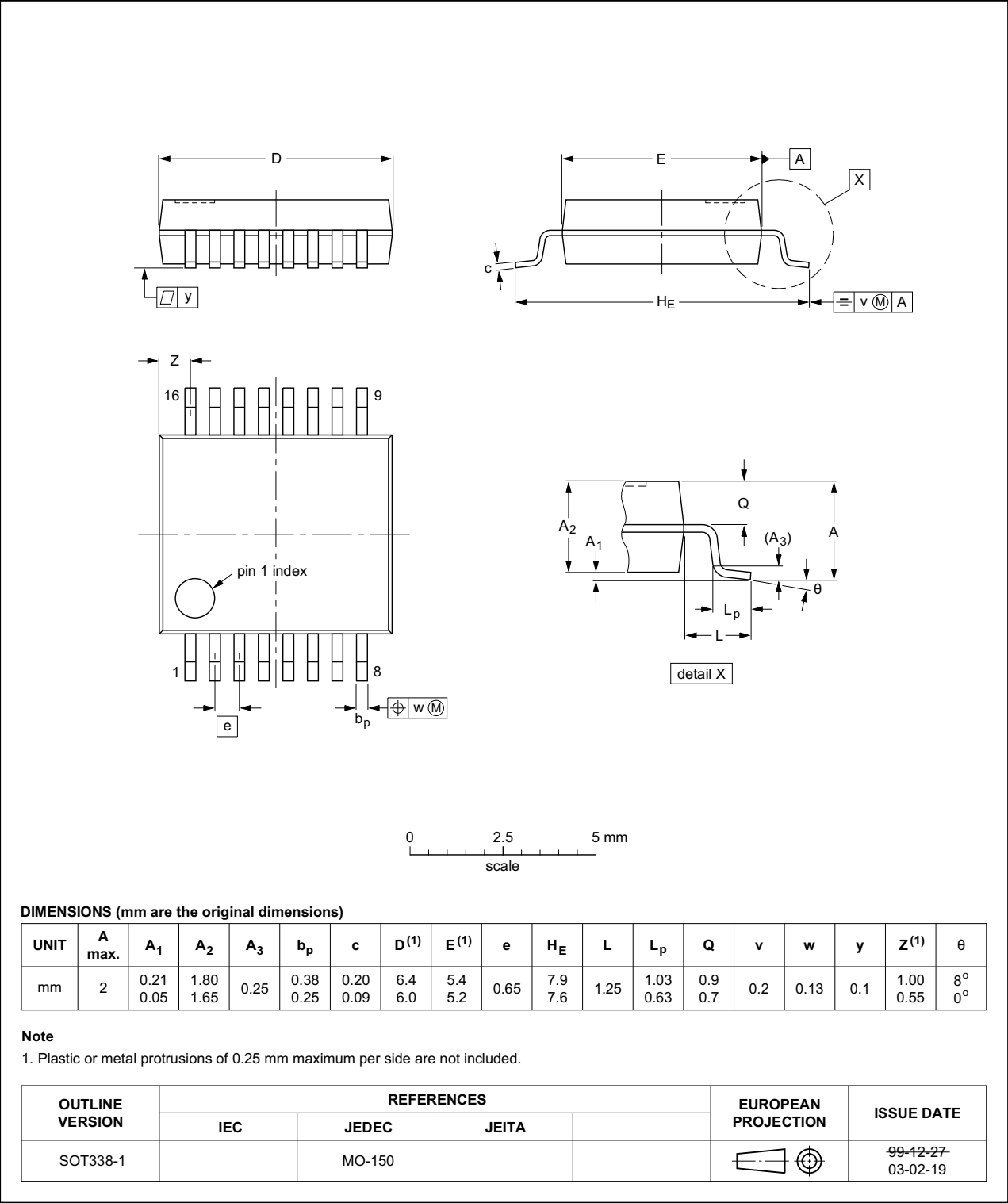
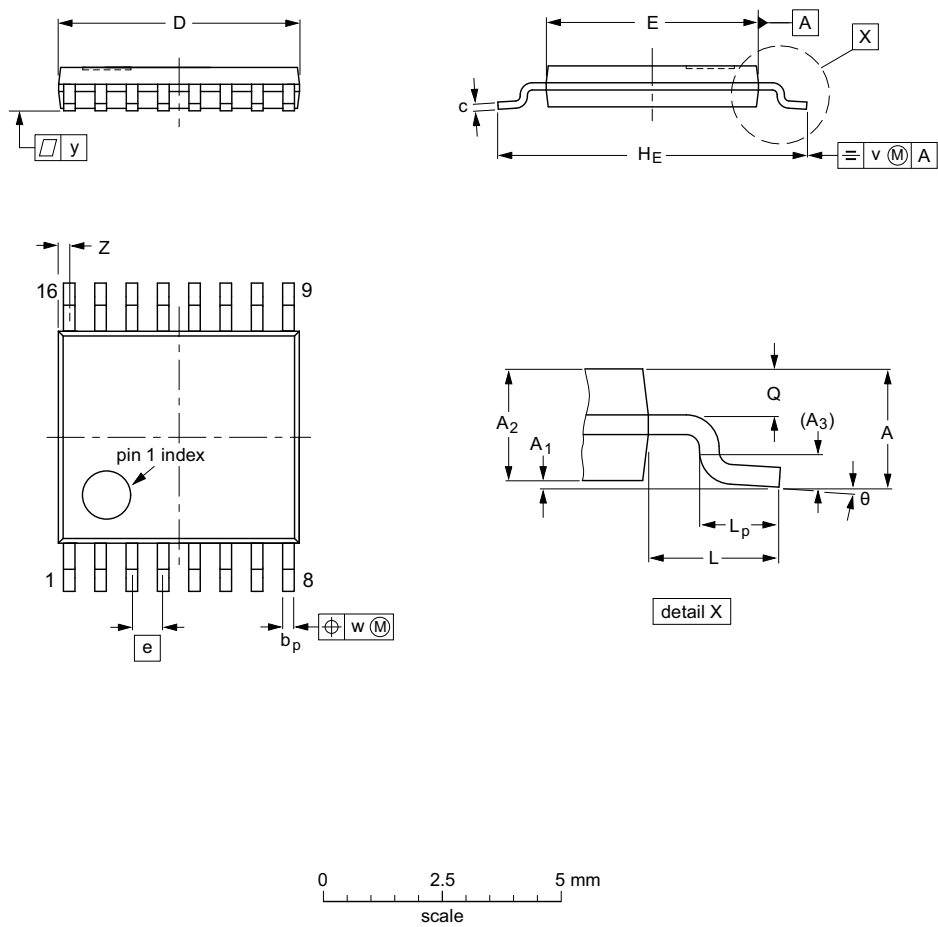


Fig 13. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

- Notes
- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
 - 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

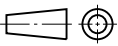
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				-99-12-27 03-02-18

Fig 14. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT173 v.3	20161108	Product data sheet	-	74HC_HCT173 v.2
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. - Type numbers 74HCT173N and 74HC173N removed.			
74HC_HCT173 v.2	19901201	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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