

IRFS9N60APBF-VB Datasheet

N-Channel 650V (D-S) Power MOSFET

**RoHS****PRODUCT SUMMARY**

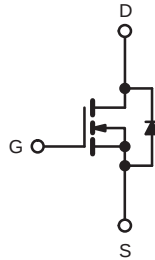
V_{DS} (V) at T_J max.	650	
$R_{DS(on)}$ at 25 °C (Ω)	$V_{GS} = 10$ V	0.65
Q_g max. (nC)	41	
Q_{gs} (nC)	5	
Q_{gd} (nC)	22	
Configuration	Single	

FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	650	V
Gate-Source Voltage			V _{GS}	± 30	
Continuous Drain Current (T _J = 150 °C)	V _{GS} at 10 V	T _C = 25 °C	I _D	12	A
		T _C = 100 °C		9.4	
Pulsed Drain Current ^a			I _{DM}	45	
Linear Derating Factor				3.5	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	9	mJ
Maximum Power Dissipation			P _D	156/34	W
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	°C
Drain-Source Voltage Slope	T _J = 125 °C		dV/dt	15	V/ns
Reverse Diode dV/dt ^d		4.1			
Soldering Recommendations (Peak Temperature) ^c	for 10 s			300	°C

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
 b. $V_{DD} = 50$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 4.5$ A.
 c. 1.6 mm from case.
 d. $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	60	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.8	

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	650	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 1\text{ mA}$	-	0.75	-	V/ $^{\circ}\text{C}$
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	-	5	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
		$V_{GS} = \pm 30\text{ V}$	-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 520\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$	-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 8\text{ A}$	-	0.65	-	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 30\text{ V}$, $I_D = 8\text{ A}$	-	16	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$	-	800	-	pF
Output Capacitance	C_{oss}		-	70	-	
Reverse Transfer Capacitance	C_{rss}		-	8	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 520\text{ V}$, $V_{GS} = 0\text{ V}$	-	63	-	
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$		-	213	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$, $I_D = 8\text{ A}$, $V_{DS} = 520\text{ V}$	-	48	-	nC
Gate-Source Charge	Q_{gs}		-	11	-	
Gate-Drain Charge	Q_{gd}		-	21	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 520\text{ V}$, $I_D = 8\text{ A}$, $V_{GS} = 10\text{ V}$, $R_g = 9.1\text{ }\Omega$	-	13	25	ns
Rise Time	t_r		-	11	35	
Turn-Off Delay Time	$t_{d(off)}$		-	81	90	
Fall Time	t_f		-	25	40	
Gate Input Resistance	R_g	$f = 1\text{ MHz}$, open drain	-	3.5	-	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	15	A
Pulsed Diode Forward Current	I_{SM}		-	-	40	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_S = 8\text{ A}$, $V_{GS} = 0\text{ V}$	-	-	1.5	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = I_S = 8\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $V_R = 400\text{ V}$	-	345	-	ns
Reverse Recovery Charge	Q_{rr}		-	4.5	-	μC
Reverse Recovery Current	I_{RRM}		-	35	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Fig. 1 - Typical Output Characteristics



Fig. 4 - Normalized On-Resistance vs. Temperature



Fig. 2 - Typical Output Characteristics

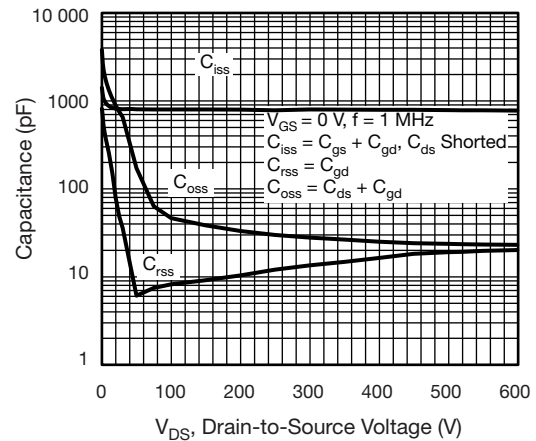


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



Fig. 3 - Typical Transfer Characteristics



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



Fig. 7 - Typical Source-Drain Diode Forward Voltage



Fig. 9 - Maximum Drain Current vs. Case Temperature

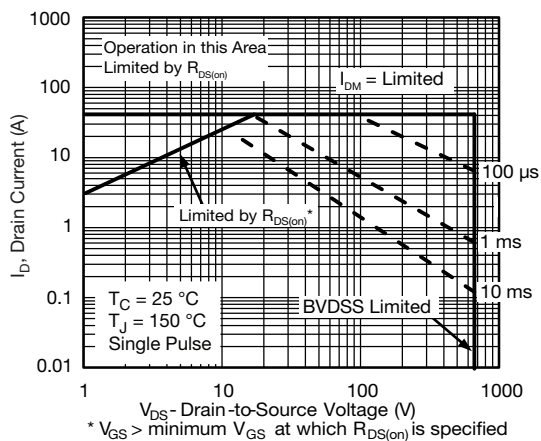


Fig. 8 - Maximum Safe Operating Area



Fig. 10 - Temperature vs. Drain-to-Source Voltage

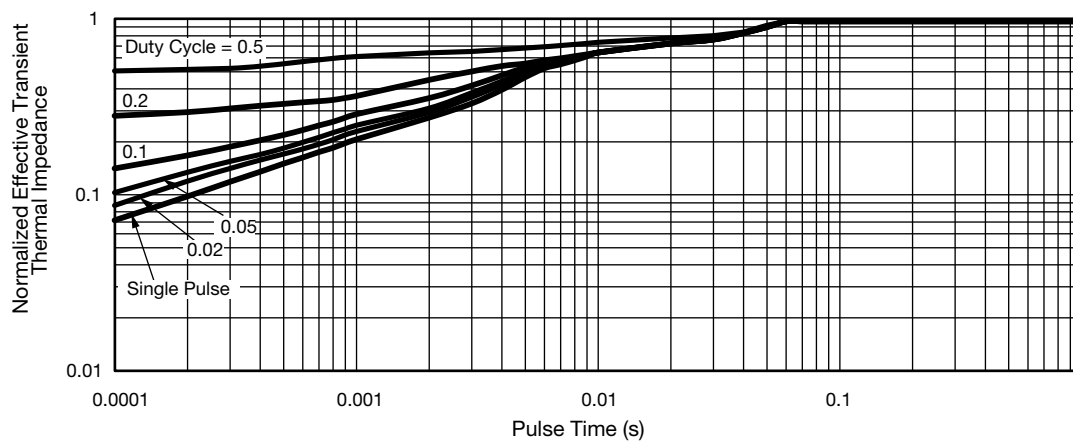


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case



Fig. 12 - Switching Time Test Circuit



Fig. 16 - Basic Gate Charge Waveform

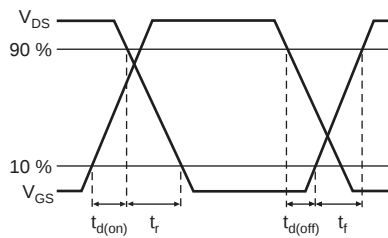


Fig. 13 - Switching Time Waveforms



Fig. 14 - Unclamped Inductive Test Circuit



Fig. 15 - Unclamped Inductive Waveforms

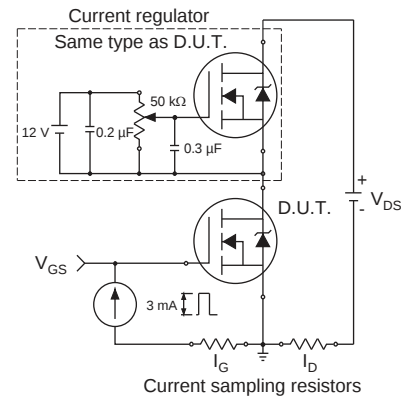


Fig. 17 - Gate Charge Test Circuit

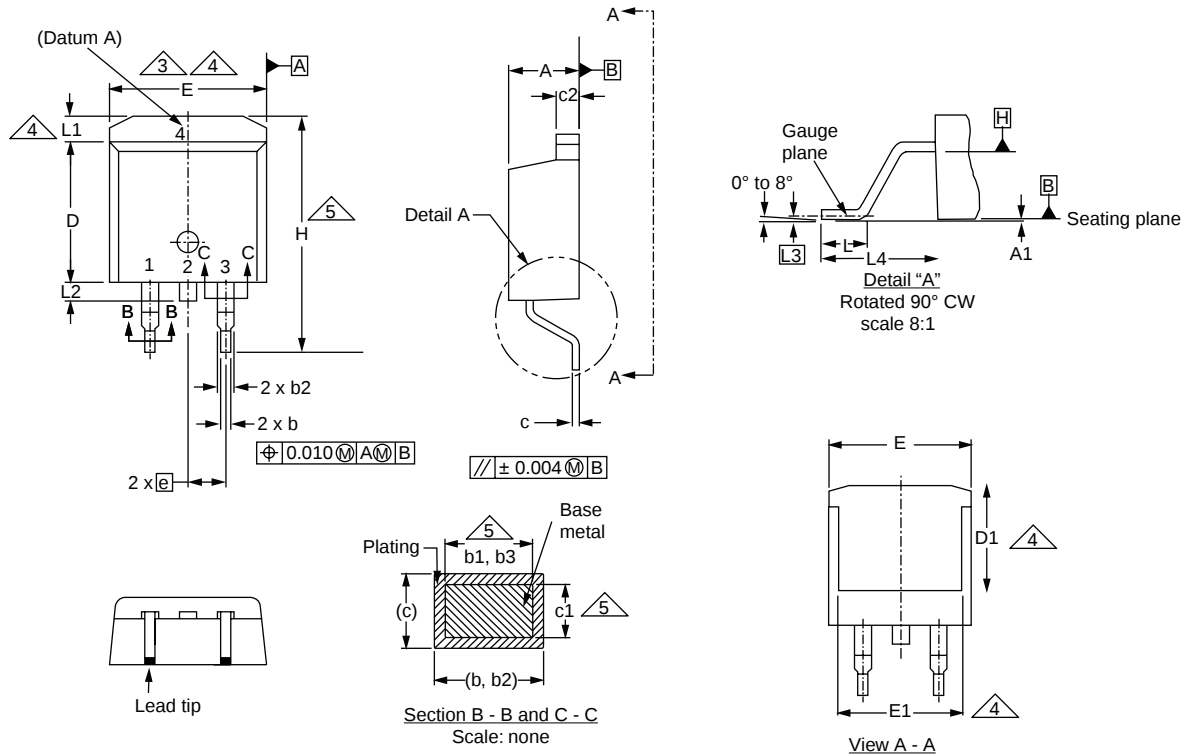


Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 18 - For N-Channel

TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

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