

AUIRF5210STRR-VB Datasheet

P-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY

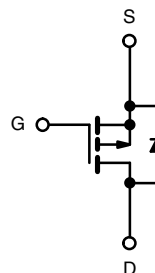
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
- 100	0.040 at V _{GS} = - 10 V	- 37	54 nC
	0.050 at V _{GS} = - 4.5 V	- 32	

FEATURES

- Trench Power MOSFET



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P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 100	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C) ^b	T _C = 25 °C	- 37	A
	T _C = 70 °C	- 29.5	
	T _A = 25 °C	- 10 ^{b, c}	
	T _A = 70 °C	- 8.2 ^{b, c}	
Pulsed Drain Current	I _{DM}	- 150	A
Continuous Source Current (Diode Conduction)	T _C = 25 °C	- 50 ^a	
	T _A = 25 °C	- 6.75 ^{b, c}	
Avalanche Current	I _{AS}	- 35	mJ
Single Pulse Avalanche Energy	E _{AS}	61	
Maximum Power Dissipation	T _C = 25 °C	113.6	W
	T _C = 70 °C	72.7	
	T _A = 25 °C	6.9 ^{b, c}	
	T _A = 70 °C	4.4 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient	R _{thJA}	40	°C/W
Junction-to-Case (Drain)	R _{thJC}	2.1	

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 10 s.

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 100			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 109		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			5.9		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 1		- 3	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 100 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 100 V, V _{GS} = 0 V, T _J = 55 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = - 10 V	- 40			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V, I _D = - 9.2 A		0.040		Ω
		V _{GS} = - 4.5 V, I _D = - 7.7 A		0.050		
Forward Transconductance ^a	g _{fs}	V _{DS} = - 15 V, I _D = - 9.2 A		38		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 50 V, V _{GS} = 0 V, f = 1 MHz		3800		pF
Output Capacitance	C _{oss}			185		
Reverse Transfer Capacitance	C _{rss}			135		
Total Gate Charge	Q _g	V _{DS} = - 50 V, V _{GS} = - 10 V, I _D = - 9.2 A		106	160	nC
		V _{DS} = - 50 V, V _{GS} = - 4.5 V, I _D = - 9.2 A		54	81	
Gate-Source Charge	Q _{gs}			14		
Gate-Drain Charge	Q _{gd}			26		
Gate Resistance	R _g	f = 1 MHz		4		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 50 V, R _L = 6.5 Ω I _D ≅ - 7.7 A, V _{GEN} = - 10 V, R _g = 1 Ω		15	25	ns
Rise Time	t _r			20	30	
Turn-Off Delay Time	t _{d(off)}			110	165	
Fall Time	t _f			100	150	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 50 V, R _L = 6.5 Ω I _D ≅ - 7.7 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		42	65	ns
Rise Time	t _r			160	240	
Turn-Off Delay Time	t _{d(off)}			100	150	
Fall Time	t _f			100	150	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 50	A
Pulse Diode Forward Current ^a	I _{SM}				- 40	
Body Diode Voltage	V _{SD}	I _S = - 7.7 A		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 7.7 A, dI/dt = 100 A/μs, T _J = 25 °C		60	90	ns
Body Diode Reverse Recovery Charge	Q _{rr}			150	225	nC
Reverse Recovery Fall Time	t _a			46		ns
Reverse Recovery Rise Time	t _b			14		

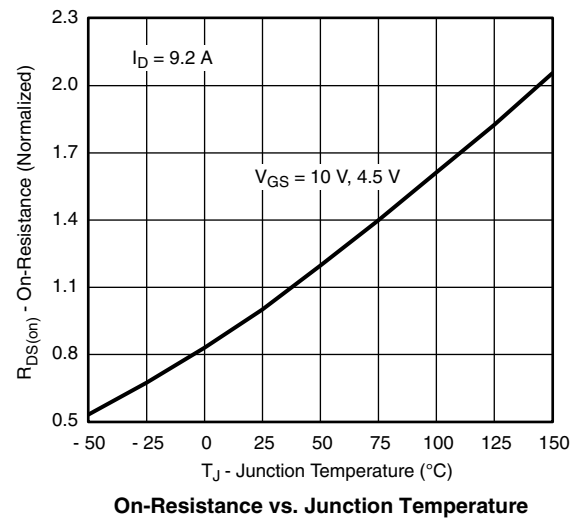
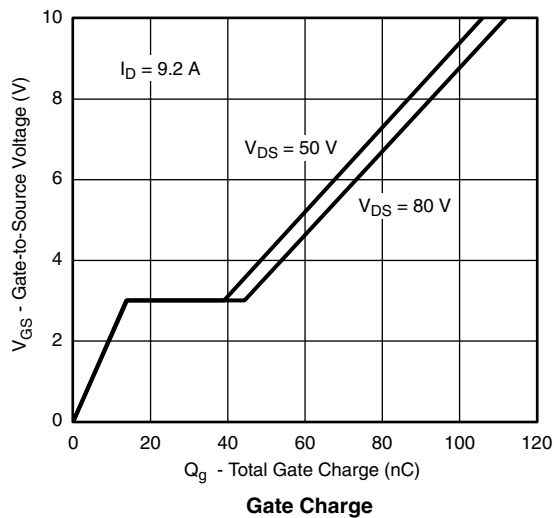
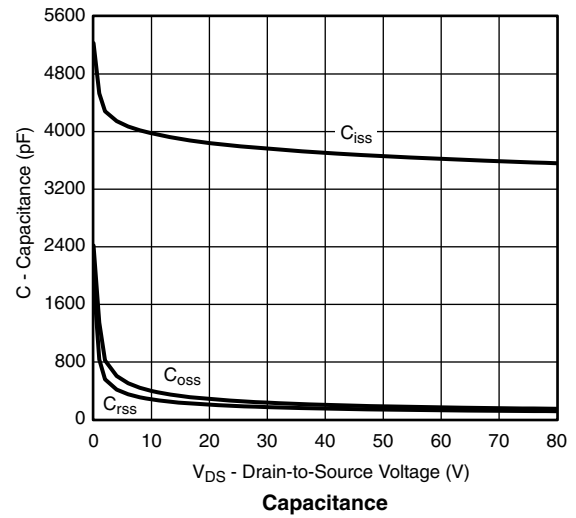
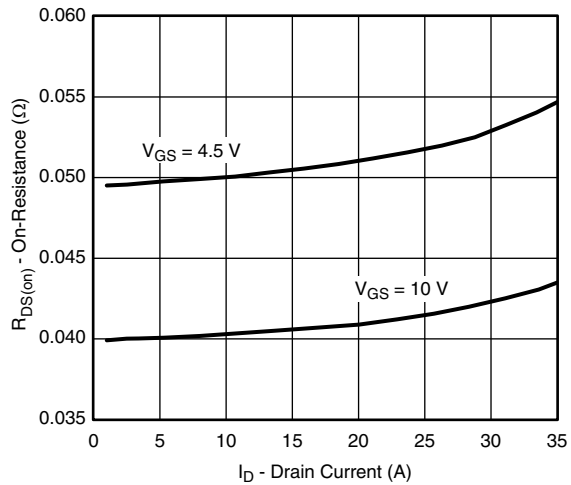
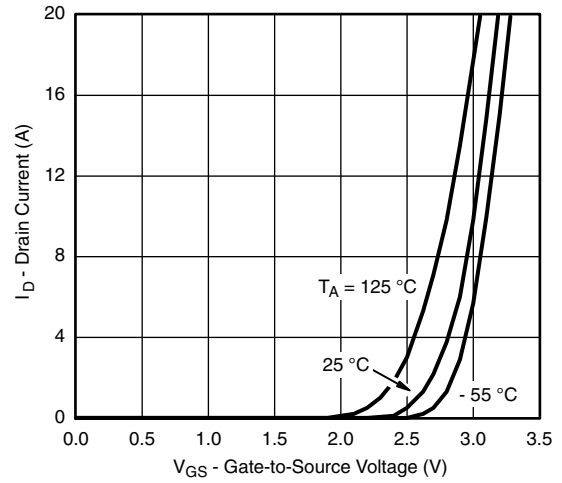
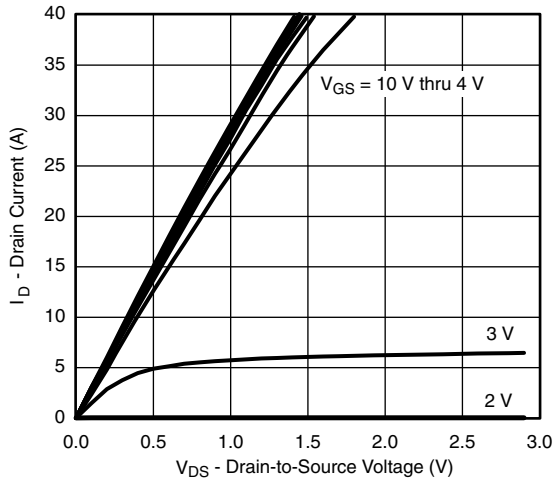
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

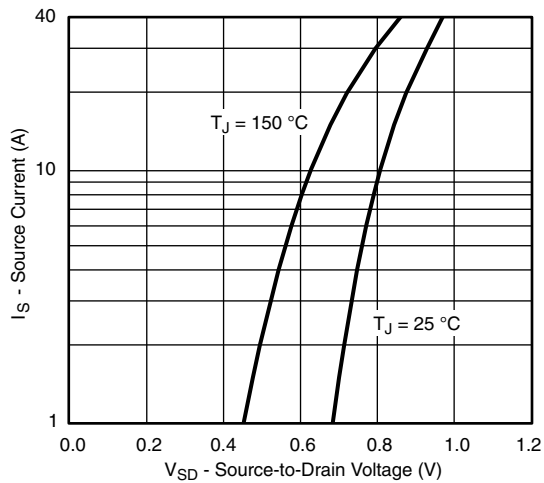
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

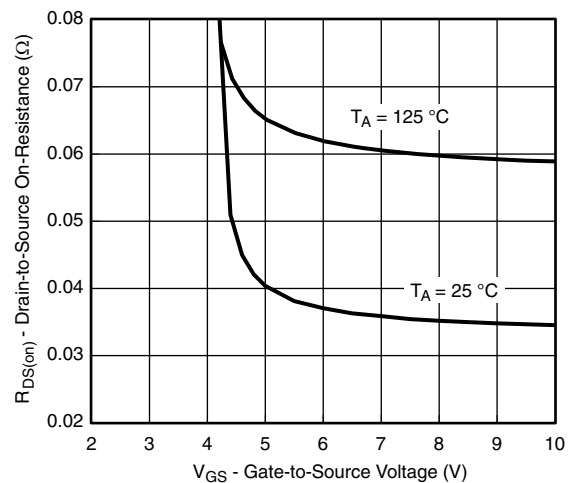
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



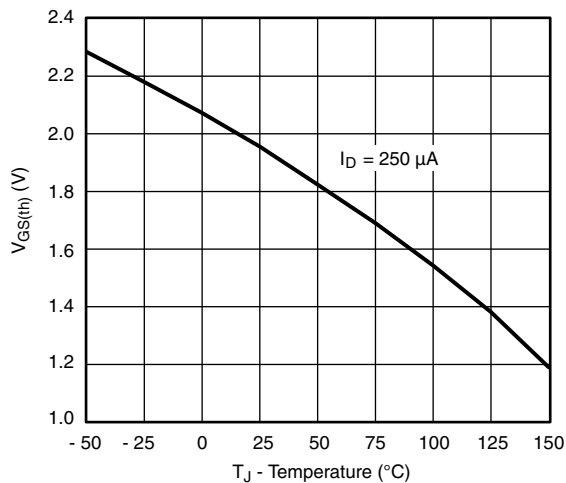
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



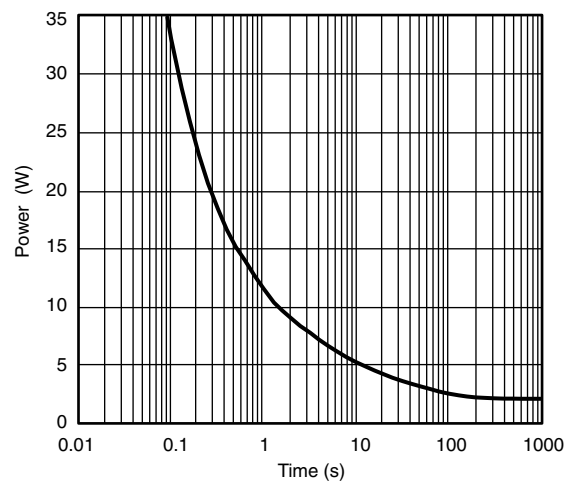
Source-Drain Diode Forward Voltage



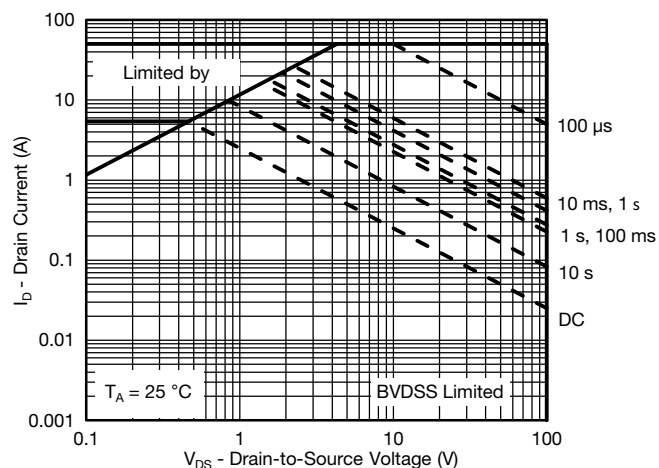
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



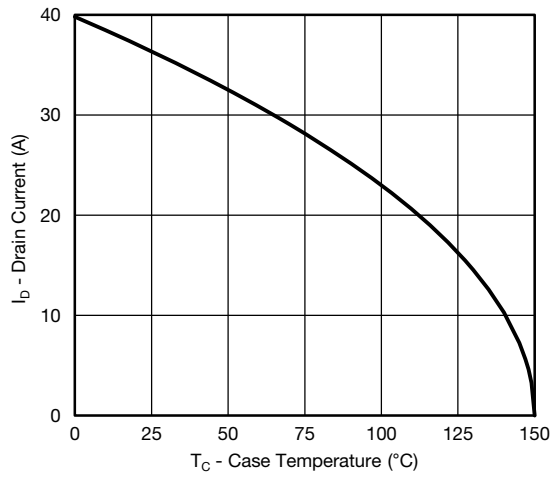
Single Pulse Power, Junction-to-Ambient



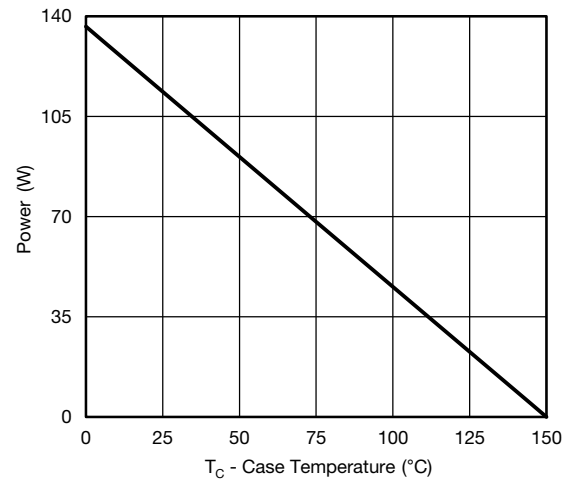
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

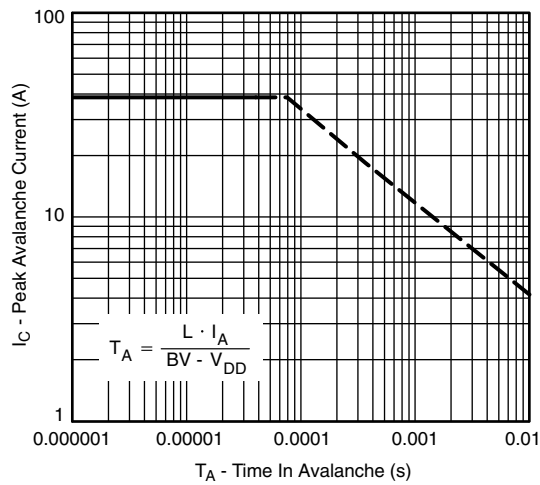
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



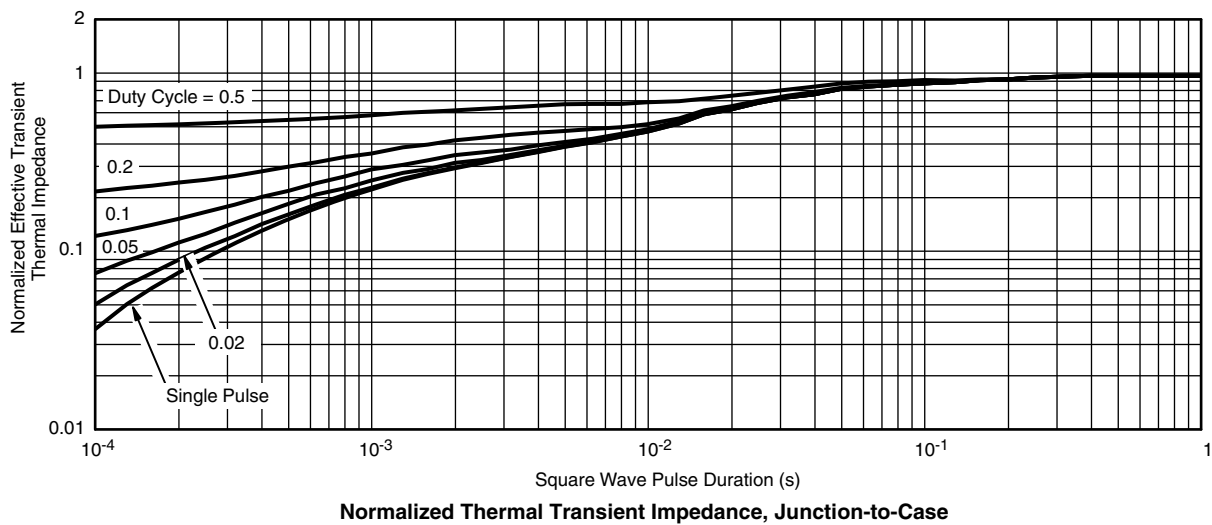
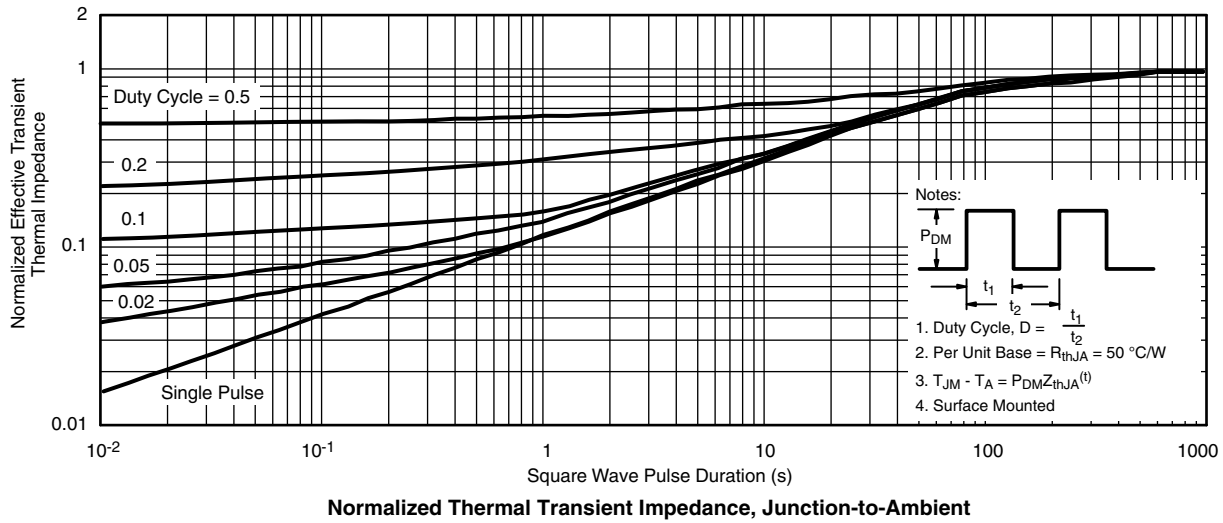
Single Pulse Power, Junction-to-Ambient



Single Pulse Avalanche Capability

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Technical drawing of a lead tip assembly, showing front, side, and detail views with dimensions and tolerances.

Front View: Shows the lead tip assembly with dimensions E , D , H , $L1$, $L2$, $L3$, $L4$, $L5$, $L6$, $L7$, $L8$, $L9$, $L10$, $L11$, $L12$, $L13$, $L14$, $L15$, $L16$, $L17$, $L18$, $L19$, $L20$, $L21$, $L22$, $L23$, $L24$, $L25$, $L26$, $L27$, $L28$, $L29$, $L30$, $L31$, $L32$, $L33$, $L34$, $L35$, $L36$, $L37$, $L38$, $L39$, $L40$, $L41$, $L42$, $L43$, $L44$, $L45$, $L46$, $L47$, $L48$, $L49$, $L50$, $L51$, $L52$, $L53$, $L54$, $L55$, $L56$, $L57$, $L58$, $L59$, $L60$, $L61$, $L62$, $L63$, $L64$, $L65$, $L66$, $L67$, $L68$, $L69$, $L70$, $L71$, $L72$, $L73$, $L74$, $L75$, $L76$, $L77$, $L78$, $L79$, $L80$, $L81$, $L82$, $L83$, $L84$, $L85$, $L86$, $L87$, $L88$, $L89$, $L90$, $L91$, $L92$, $L93$, $L94$, $L95$, $L96$, $L97$, $L98$, $L99$, $L100$. Tolerances: ± 0.010 (M), ± 0.004 (B). Datum A is indicated.

Side View: Shows the lead tip assembly with dimensions A , B , C , D , E , F , G , H , I , J , K , L , M , N , O , P , Q , R , S , T , U , V , W , X , Y , Z . Tolerances: ± 0.010 (M), ± 0.004 (B). Datum A is indicated.

Detail A: Shows the lead tip assembly with dimensions A , B , C , D , E , F , G , H , I , J , K , L , M , N , O , P , Q , R , S , T , U , V , W , X , Y , Z . Tolerances: ± 0.010 (M), ± 0.004 (B). Datum A is indicated.

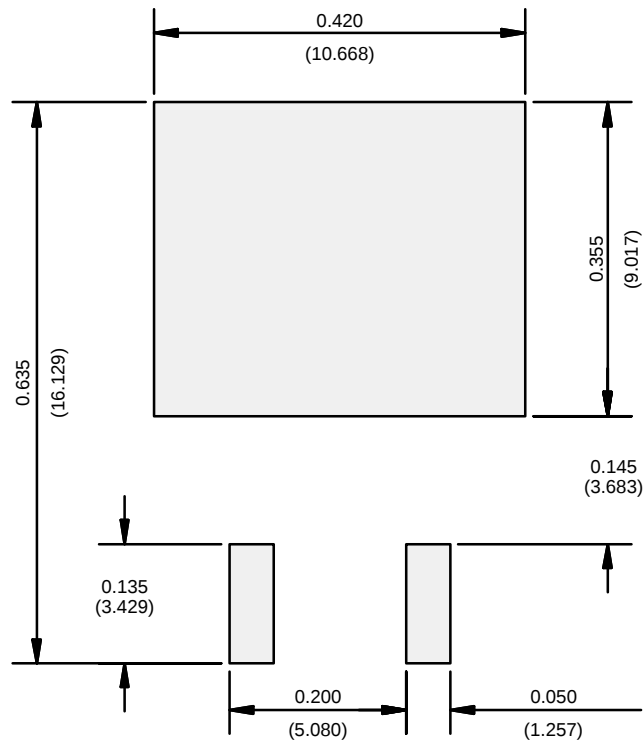
Section B - B and C - C: Shows the lead tip assembly with dimensions $b1$, $b2$, $b3$, $c1$, $c2$, $c3$, $c4$, $c5$, $c6$, $c7$, $c8$, $c9$, $c10$, $c11$, $c12$, $c13$, $c14$, $c15$, $c16$, $c17$, $c18$, $c19$, $c20$, $c21$, $c22$, $c23$, $c24$, $c25$, $c26$, $c27$, $c28$, $c29$, $c30$, $c31$, $c32$, $c33$, $c34$, $c35$, $c36$, $c37$, $c38$, $c39$, $c40$, $c41$, $c42$, $c43$, $c44$, $c45$, $c46$, $c47$, $c48$, $c49$, $c50$. Tolerances: ± 0.010 (M), ± 0.004 (B). Datum A is indicated.

View A - A: Shows the lead tip assembly with dimensions A , B , C , D , E , F , G , H , I , J , K , L , M , N , O , P , Q , R , S , T , U , V , W , X , Y , Z . Tolerances: ± 0.010 (M), ± 0.004 (B). Datum A is indicated.

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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