

Ultra-Low Phase Jitter LVPECL SMD Clock Oscillator

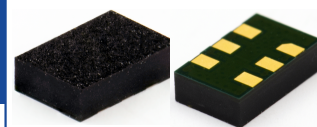
ASFLMX-25.000MHz-5ABA



ESD Sensitive



RoHS/RoHS II compliant



5.0 x 3.2 x 1.4mm

Moisture Sensitivity Level – MSL 3

FEATURES:

- 25MHz LVPECL
- Typical phase noise: 100fs (Integration range: 1.875MHz-20MHz)
- ± 50 ppm total frequency stability over -40°C to +85°C temperature range
- Industry standard 6-Pin 5 x 3.2mm LGA package

APPLICATIONS:

- Communications
- Backplane reference clock
- SERDES reference clock
- FPGA

KEY ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Minimum	Maximum	Unit	Condition
Supply Voltage	-0.3	+3.6	V	
Storage Temp.	-55	+125	°C	
Lead Temp.(soldering, 10s)		+260	°C	
ESD (HBM)		2	kV	

VDD = 2.375 - 3.63V, TA = -40°C to +85°C, outputs terminated with 50 Ohms to VDD - 2.⁽¹⁾

Parameters		Minimum	Typical	Maximum	Units	Notes
Frequency		25.000			MHz	
Operating Temperature (TA)		-40		+85	°C	
Overall Frequency Stability ⁽²⁾		-50		+50	ppm	
Supply Voltage (VDD)		+2.375		+3.63	V	
Supply Current (IDD)				120	mA	
Output Logic Level	VOH	VDD-1.35	VDD-1.01	VDD-0.8	V	
	VOL	VDD-2.0	VDD-1.78	VDD-1.6	V	
Peak to Peak Output Swing (Vswing)		0.65	0.77	0.95	V	Single ended
Start-up Time				20	ms	
Rise Time (Tr)		85		350	ps	RL=50Ω, CL=0pF 20% to 80%
Fall Time (Tf)		85		350		
Duty Cycle		45		55	%	
Phase Noise	Integration Range: 12kHz to 20MHz		220		fsRMS	
	Integration Range: 1.875MHz to 20MHz		100			

Notes:

1. Guaranteed after thermal equilibrium
2. Inclusive of initial accuracy, temperature drift, aging, shock, vibration from -40°C to +85°C.

PART IDENTIFICATION

ASFLMX-25.000MHz -5ABA -

Packing

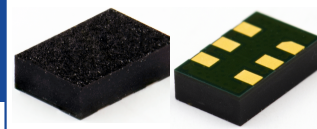
Blank: Bulk or Tube
T: Tape & Reel (1k/reel)

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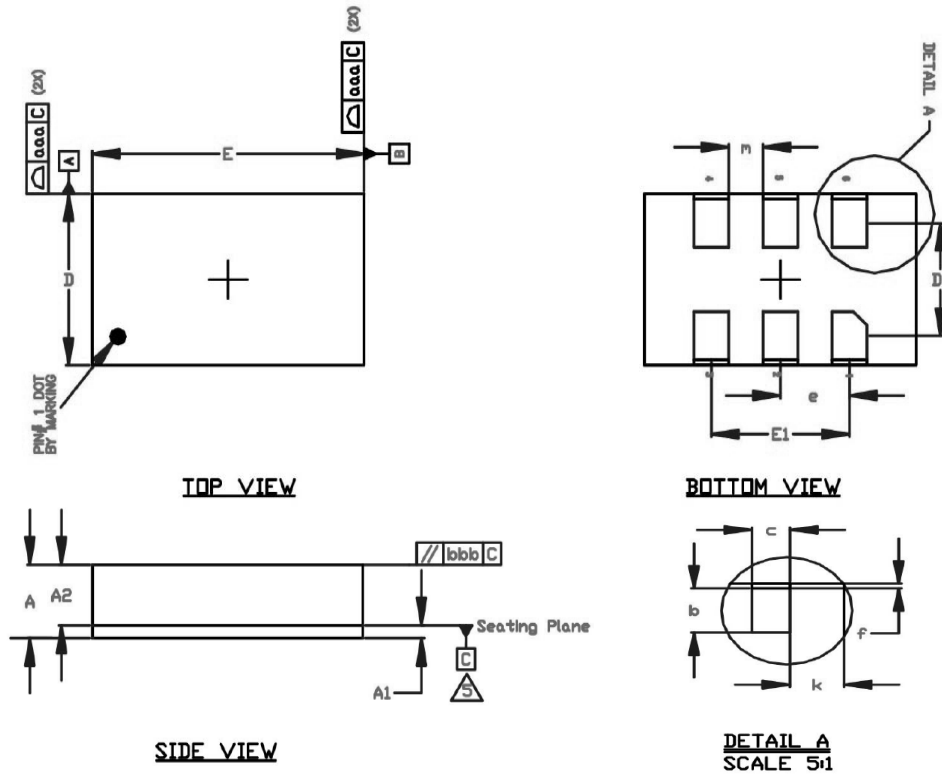


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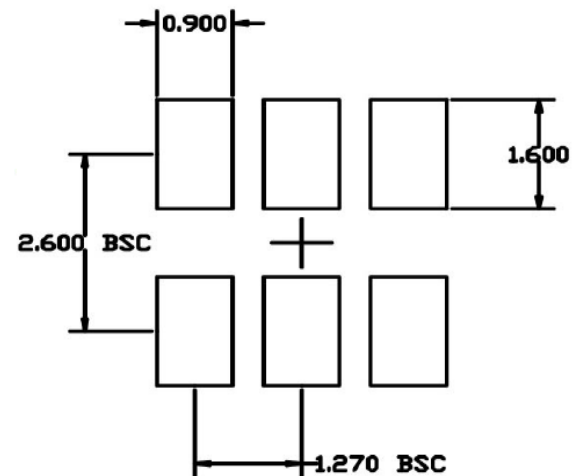
OUTLINE DIMENSION



Ref.	Min.	Nom.	Max.
A	1.260	1.330	1.400
A1	0.190	0.230	0.270
A2	1.070	1.100	1.130
D	3.100	3.200	3.300
D1	2.100 BSC		
E	4.900	5.000	5.100
E1	2.540 BSC		
b	0.850	0.900	0.950
c	0.850	0.900	0.950
e	1.270 BSC		
f	0.050	0.100	0.150
k	0.860	0.910	0.960
m	0.580	0.630	0.680
n		6	

Dimensional Tolerance	
aaa	0.100
bbb	0.070

Recommended Land Pattern



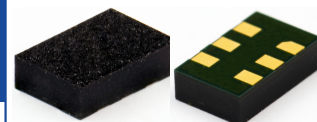
Dimensions: mm

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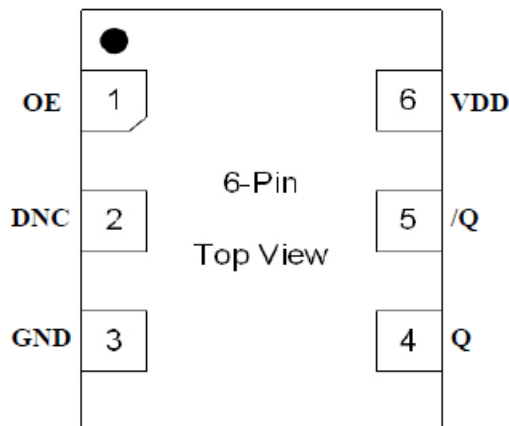


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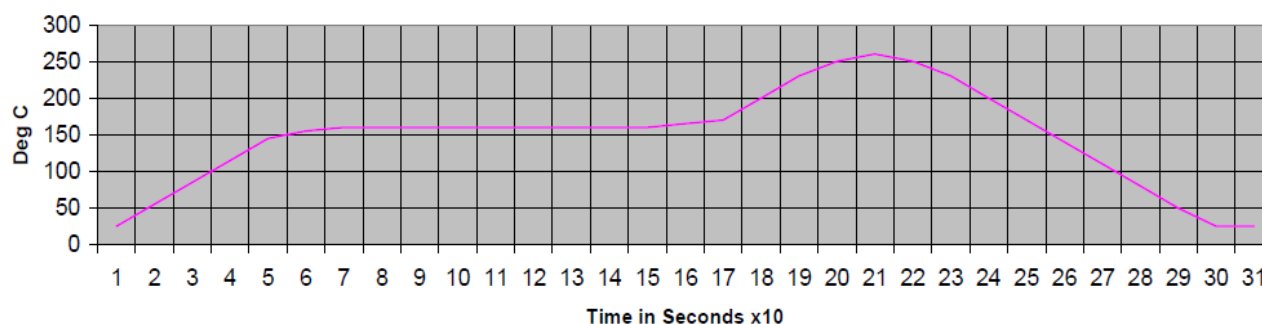
PIN CONFIGURATION



Pin #	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I, SE	LVC MOS	Output Enable, disables output to tri-state. 0 = Disabled, 1= Enabled, 50k Ω Pull-up
2	DNC			Make no connection, leave floating
3	GND	PWR		Power Supply Ground
4	Q	O	LVPECL	Clock Output
5	/Q	O	LVPECL	Complimentary Clock Output
6	VDD	PWR		Power Supply

REFLOW PROFILE

Lead-free Reflow Profile



Parameters	Specifications
Average Ramp-up Rate	3°C /second max.
Pre-Heat Temp 150 – 200°C	60 – 180 second
Temp > 217°C	60 – 150 second
Time @ Peak Temperature	20 – 40 second
Peak Temperature	260°C + 0°C / -5°C
Ramp-down Rate	-6°C / second max.
Time 25°C to Peak Temp.	8 minutes max.



5.0 x 3.2 x 1.4mm

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