

#### **Features**

- Integrated <u>Transient Voltage Suppressor</u>
   (TVS) in the Transceiver IC
- TVS Protection for Bus Terminals:
   ±15 kV IEC 61000-4-2, Contact Discharge
   ±18 kV IEC 61000-4-2, Air-Gap Discharge
   ±15 kV EIA/JEDEC Human Body Model
- HBM ±4kV ESD Protection for all pins
- MM ±400V ESD Protection for all pins
- Latchup immunity up to ±400mA for all pins.
- High CDM protection up to ±1kV for all pins.
- Meet the Requirements of the EIA/TIA-485
   Standards with 5V Power Supply
- True Fail-Safe Receiver While Maintaining EIA/TIA-485 Compatibility
- Data Rate up to 10Mbps
- Hot-Swap Glitch free Protection on Control Inputs
- High driving ability of VOD2
- Up to 256 Transceivers on the Bus

### **Applications**

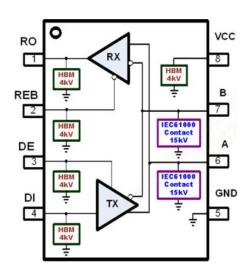
- Utility Meters
- Lighting Systems
- Industrial Control
- Security Systems
- Instrumentation
- Profibus Application

# **Description**

The AZRS5054PA is a ±15kV IEC 61000-4-2 contact discharge protected half-duplex RS485 transceiver IC, which contains one transmitter and one receiver inside. This device is fully compliant with the EIA/TIA-485 standard with 5V power supply.

The AZRS5054PA features a fail-safe receiver, which guarantees the output of the receiver to be logic high when the differential inputs (bus pins, A and B) of the receiver are open, short or idle under abnormal operating conditions.

The AZRS5054PA features a hot-swap glitch-free design which guarantees outputs of the transmitter and the receiver in a high impedance state and even no short current event during the power up period. The AZRS5054PA has the thermal shutdown and the current limited function in the transmitter to protect the device from damage by system fault conditions during normal AZRS5054PA operating condition. The designed 1/8 unit load with minimum 96kohm of input impedance, which can connect 256 devices on a bus at most. The AZRS5054PA is also a high reliable device with built-in system level ESD protected devices against high-energy noise transients without requiring any external components.



**Functional Block of AZRS5054PA** 

Part Number	Duplex	Tx/Rx	Supply	Max Data Rate	Fail- safe	Rx Input	HBM on	IEC 61000-4-2	Package
			(V)	(Mbps)		Filtering	A,B	Contact on A,B	Туре
AZRS5054PA	Half	1/1	5	10	Yes	Yes	±15kV	± 15kV	SO-8

### **ABSOLUTE MAXIMUM RATINGS**

PARAMETER	PARAMETER	RATING	UNITS
Power Supply Vcc	Vcc	-0.3 to 8.0	V
Control Input Voltage	REB, DE	-0.3 to (Vcc+ 0.3)	V
Receiver Input Voltage	A, B	±13	V
Receiver Output Voltage	RO	-0.3 to (Vcc+ 0.3)	V
Transmitter Output Voltage	A, B	±13	V
Transmitter Input	DI	-0.3 to (Vcc+ 0.3)	V
Operating Temperature	T <sub>OP</sub>	-40 to +85	°C
Storage Temperature	T <sub>STO</sub>	-65 to +150	°C

### DC ELECTRICAL CHARACTERISTICS

(Vcc=5V  $\pm$ 5% with T<sub>AMB</sub>= T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at Vcc=5V and T<sub>AMB</sub>= 25 °C.)

PARAMETER	SYMBOL	SYMBOL CONDITIONS		MIN	TYP	MAX	UNITS
Transmitter							
Differential Transmitter Output	V <sub>OD1</sub>	/ <sub>OD1</sub> No load				Vcc	V
Differential Transmitter Output	V <sub>OD2</sub>	Fig.1, $R_L = 27 \Omega$		2.3	3.0		V
Change in Magnitude of Differential Output Voltage	$\Delta V_{OD}$	Fig.1, $R_L = 27 \Omega$				0.2	V
Transmitter Common- Mode Output Voltage	V <sub>oc</sub>	Fig.1, $R_L = 27 \Omega$				3	V
Change in Magnitude of Common- Mode Voltage	$\Delta V_{ m OC}$	Fig.1, $R_L = 27 \Omega$				0.2	V
Input High Voltage	V <sub>IH</sub>	DE, DI, REB		2.0			V
Input Low Voltage	V <sub>IL</sub>	DE, DI, REB				0.8	V
Input Current	I <sub>IN1</sub>	DE, DI, REB				±2	μΑ
land Compatition A and D	I <sub>IN2</sub>	DE=0, Vcc=0V	V <sub>IN</sub> =12V			125	^
Input Current for A and B		or 5.25V	V <sub>IN</sub> =-7V	-100			uA
Transmitter Short-Circuit Output Current	I <sub>OSD</sub>	$-7V \le V_{OUT} \le 12V$ , $Vcc=5.0V$		-250		250	mA
RECEIVER							
Receiver Differential Threshold Voltage			-200		-50	mV	
Receiver Input Hysteresis	$\Delta$ V <sub>TH</sub>				20		mV
		Io= -4mA, VID= 200mV		Vcc-0.6			V
Receiver Output Low Voltage	V <sub>OL</sub>	Io= 4mA, VID= -	200mV			0.4	V
Three- State Output Current at	I <sub>OZR</sub>	REB=Vcc				±1	μΑ

**SYMBOL CONDITIONS** MIN **TYP** MAX **UNITS PARAMETER** Receiver  $-7V \le V_{CM} \le +12V$ Receiver Input Resistance  $R_{IN}$ 96  $k\Omega$ Receiver Output Short-Circuit Fig. 6,  $0V \le V_{RO} \le V_{CC}$  $I_{\text{OSR}}$ ±95 m A Current **SUPPLY CURRENT** No load, DE= Vcc 600 900 μΑ REB=GND, Supply Current Icc DI=Vcc or DE= GND 600 900 μΑ GND. Supply Current in Shutdown REB= Vcc DE= GND  $I_{\text{SHDN}}$ 10 μΑ

### **SWITCHING CHARACTERISTICS**

Mode

(Vcc=5V  $\pm$ 5% with T<sub>AMB</sub>= T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at Vcc=5V and T<sub>AMB</sub>= 25 °C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Transmitter Input to Output		Fig.2 and 7, $R_{DIFF}$ =54 $\Omega$ ,			50	20
Transmitter input to Output	t <sub>DPLH</sub> , t <sub>DPHL</sub>	C <sub>L1</sub> =C <sub>L2</sub> = 100pF			30	ns
Transmitter Output Skew	+	Fig.2, Fig.7, $R_{DIFF}$ =54 $\Omega$ ,		10		nc
$t_{DPLH}t_{DPH}$	t <sub>DSKEW</sub>	C <sub>L1</sub> =C <sub>L2</sub> = 100pF		10		ns
Transmitter Rise or Fall Time	t <sub>DF</sub> , t <sub>DR</sub>	Fig.2, Fig.7, $R_{DIFF}$ =54 $\Omega$ ,			20	ns
		C <sub>L1</sub> =C <sub>L2</sub> = 100pF				_
Data Rate	f <sub>Data</sub>				10	Mbps
Transmitter Enable to Output	t <sub>DZL</sub>	Fig.4, Fig.8, C <sub>DL</sub> = 100pF, S1			70	ns
Low	-DZL	closed				
Transmitter Enable to Output	t <sub>DZH</sub>	Fig.4, Fig.8, C <sub>DL</sub> = 100pF, S2			70	ns
High	-5211	closed				_
Transmitter Disable Time	$t_{DLZ}$	Fig.4, Fig.8, C <sub>DL</sub> = 15pF, S1			70	ns
from Low	-502	closed				_
Transmitter Disable Time	t <sub>DHZ</sub>	Fig.4, Fig.8, C <sub>DL</sub> = 15pF, S2			70	ns
from High	-DHZ	closed				
Transmitter Enable from		Fig.4, Fig.8, C <sub>DL</sub> = 50pF, S1			4000	
Shutdown to Output Low	t <sub>DZL(SHDN)</sub>	closed			1800	ns
Transmitter Enable from		Fig.4, Fig.8, C <sub>DI</sub> = 50pF, S2				
	t <sub>DZH(SHDN)</sub>				1800	ns
Shutdown to Output High	` ,	closed				
Time to shutdown	t <sub>SHDN</sub>		50	800	1200	ns
		Fig.5, Fig.9, $ V_{ID}  \ge 2.0V$ ;				
Receiver Input to Output	t <sub>RPLH</sub> , t <sub>RPHL</sub>	rise and fall time of $V_{ID} \le$		120	200	ns
		15ns				
$t_{RPL\overline{H}}t_{RPH}$ Different	t	Fig.5, Fig.9, $ V_{ID}  \ge 2.0V$ ;		10		ns
Receiver Skew	t <sub>RSKD</sub>	rise and fall time of $V_{ID} \le$		10		113



PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		15ns				
Receiver Enable to Output Low	t <sub>RZL</sub>	Fig.3, Fig.10, C <sub>RL</sub> = 15pF, S1 closed			50	ns
Receiver Enable to Output High	t <sub>RZH</sub>	Fig.3, Fig.10, C <sub>RL</sub> = 15pF, S2 closed			50	ns
Receiver Disable Time from Low	t <sub>RLZ</sub>	Fig.3, Fig.10, C <sub>RL</sub> = 15pF, S1 closed			50	ns
Receiver Disable Time from High	t <sub>RHZ</sub>	Fig.3, Fig.10, C <sub>RL</sub> = 15pF, S2 closed			50	ns
Receiver Enable from Shutdown to Output Low	t <sub>RZL(SHDN)</sub>	Fig.3, Fig.10, C <sub>RL</sub> = 15pF, S1 closed			1800	ns
Receiver Enable from Shutdown to Output High	t <sub>RZH(SHDN)</sub>	Fig.3, Fig.10, C <sub>RL</sub> = 15pF, S2 closed			1800	ns
Time to shutdown	t <sub>SHDN</sub>		50	400	700	ns

## PIN FUNCTION DESCRIPTION

Pin Number	Mnemonic	Function
1	RO	Receiver Output: When REB is low and if (A - B) ≥ -50mV,
		RO is high; if (A - B) ≤ -200mV, RO is low.
2	REB	Receiver Output Enable: REB is low to enable the Receiver; REB
		is high to disable the Receiver.
3	DE	Transmitter Output Enable: DE is high to enable the transmitter;
		DE is low to disable the transceiver.
4	DI	Transmitter Input: When DE is high, a low on DI forces A output
		low and B output high. Similarly, a high on DI forces A output high
		and B output low.
5	GND	Ground pin. Must be connected to 0V.
6	А	Non-inverting Receiver Input and Non-inverting Transmitter
		Output
7	В	Inverting Receiver Input and Inverting Transmitter Output
8	VCC	Power Supply Input 5V. Must adding a 100nF decoupling
		capacitor as close to the VCC pin as possible.



## **FUNCTION TABLE**

TRANSMITTING					
INPUTS			OUTPUTS		
REB	DE	DI	Α	В	
X	1	0	0	1	
X	1	1	1	0	
0	0	X	HIGH- Z	HIGH- Z	
1	0	X	Shut	down	

X= Don't care HIGH- Z= High impedance

RECEIVING					
	INPUTS				
REB	DE	A - B	RO		
0	0	≥-0.05∨	1		
0	0	≤-0.2 V	0		
0	0	Open/Shorted	1		
1	1	X	HIGH- Z		
1	0	X	Shutdown		

X= Don't care HIGH- Z= High impedance



### **Detail Description**

The AZRS5054PA is a half-duplex RS-485 transceiver IC with IEC61000-4-2 contact ±15kV ESD protection for bus pins (A and B), which contains one transmitter and one receiver inside with 5V power supply. This device is fully compliant with the EIA/TIA-485 standard.

The AZRS5054PA features the hot-swap glitch free design which guarantees the outputs of the transceiver in a high impedance state during the power-up period until the supply voltage has stabilized. The AZRS5054PA with whole chip ESD protected design for all of the I/O pins has robust ESD protection up to both HBM  $\pm$ 4kV and MM  $\pm$ 400V. Moreover, the latchup immunity of the AZRS5054PA is up to  $\pm$ 400mA for all of the pins. For IC self discharge issue, the CDM protection level of the AZRS5054PA is up to  $\pm$ 1kV.

### **Transmitter**

The design of the transmitter is a non-inverted translator that converts the single-ended TTL input signal to differential EIA/TIA-485 signal level. The transmitter of the AZRS5054PA guarantees 10Mbps data rate communication. When the transmitter is active (DE= HIGH), the single-end TTL input signals of transmitter will be transported to differential output RS485 signals of the transmitter. Under the disable state (DE= LOW), the outputs of transmitter keep at high impedance state. The differential output voltage VA-VB(VOD2) of the AZRS5054PA is 3.0V with 54 ohm load under Vcc = 5.0V, T= 25°C.

#### Receiver

The receiver of the AZRS5054PA converts the differential EIA/TIA-485 signals to single-end output TTL signal when receiver is in active state (REB=LOW), which incorporates input filtering in addition to input hysteresis. The input filtering

enhances the noise immunity under normal operating condition. When the receiver is disable (REB=HIGH), the output of the receiver keeps in high impedance state no matter what the input of the receiver is.

#### True Fail-Safe

In traditional design, the fail-safe function is implemented by two resistors on the PCB. One resistor is terminated pin A to VCC; the other is terminated pin B to GND to keep RO at high state when bus is idle, which is only the open fail-safe. The AZRS5054PA guarantees a receiver output high when the receiver inputs are short, open or idle, that is true fail-safe. The threshold voltage of receiver input is between -50mV and -200mV. If the differential input voltage (A - B) of receiver is greater than or equal to -50mV, receiver output (RO) is logic-high. If (A - B) is less than or equal to -200mV, RO is logic-low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage (A - B) is 0V, so the RO is logic-high at that time.

### 1/8 Unit Load

The AZRS5054PA transceiver has a  $96k\Omega$  input impedance (1/8 unit load) of the receiver, allowing up to 256 or fewer devices to be connected in parallel on the RS485 bus.

# **Transmitter Output Protection**

The AZRS5054PA has the current limitation function and the thermal shutdown protection in the transmitter. Firstly, the function of current limitation provides immediate protection against short circuits over the whole common-mode voltage range (-7V to +12V). Secondly, the function of thermal shutdown protection forces the transmitter outputs into a high impedance state if the die temperature becomes excessive.



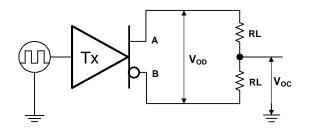


Fig.1 Transmitter DC test circuit

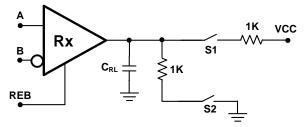


Fig.3 Receiver enable/disable timing test load

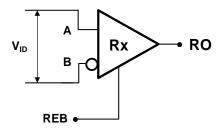


Fig.5 Receiver timing test circuit

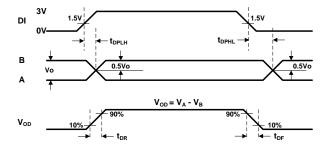


Fig.7 Transmitter Propagation Delays

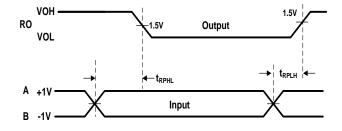


Fig.9 Receiver Propagation Delays

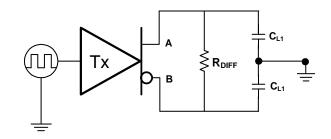


Fig.2 Transmitter timing test circuit

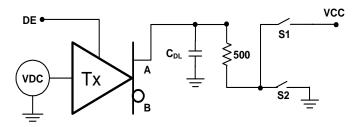


Fig.4 Transmitter enable/disable timing test load

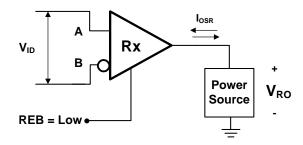


Fig.6 Receiver output short circuit

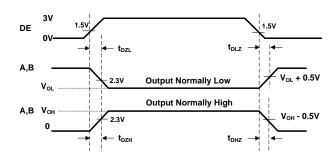


Fig.8 Transmitter Enable and Disable Times

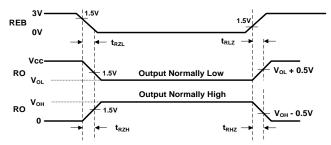
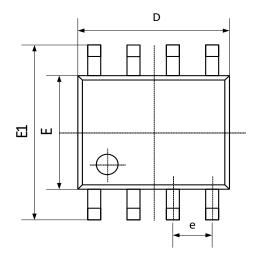


Fig.10 Receiver Enable and Disable Times

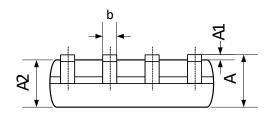


## **Mechanical Details**

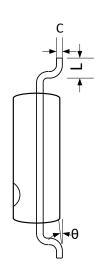
SO-8
PACKAGE DIAGRAMS
TOP VIEW



**SIDE VIEW** 



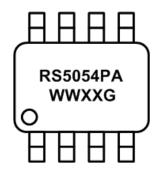
**END VIEW** 



### **PACKAGE DIMENSIONS**

	Millim	neters	Incl	hes
Symbol	min	max	min	max
А	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.55	0.049	0.061
b	0.33	0.51	0.013	0.020
С	0.17	0.26	0.007	0.010
D	4.70	5.10	0.185	0.201
Е	3.70	4.10	0.146	0.161
E1	5.80	6.20	0.228	0.244
е	1.27 BSC		0.05	BSC
L	0.40	1.27	0.016	0.050
θ	0	8	0	8

### **MARKING CODE**



RS5054PA= Device Code

WW = Date Code

XX = Control Code

G = Green Part Indication

Part Number	Marking Code
AZRS5054PA.RDG	RS5054PA
	WWXXG



ESD-Protected, High Speed, True Fail-Safe Large VOD2, RS485 Transceiver IC

# **Ordering Information**

PN#	Material	Type	Reel size	MOQ	MOQ/interal box	MOQ/carton
AZRS5054PA.RDG	Green	T/R	13 inch	2,500/reel	1 reel=2,500/box	5 boxes=12,500/carton

# **Revision History**

Revision	Modification Description				
Revision 2023/07/15	Customized Release.				