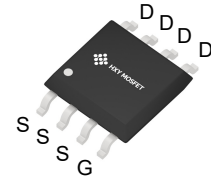




Description

The AO4459 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.



SOP-8

General Features

$V_{DS} = -30V$ $I_D = -5.8A$

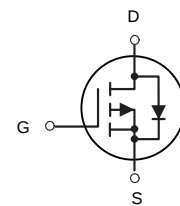
$R_{DS(ON)} < 55m\Omega$ @ $V_{GS}=10V$

Application

Battery protection

Load switch

Uninterruptible power supply



P-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AO4459	SOP-8	9435 XXX YYYY	3000

Absolute Maximum Ratings (Tc=25°C unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	- 30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_A=25^\circ C$	Drain Current ³ , V_{GS} @ 10V	-5.8	A
IDM	Pulsed Drain Current ¹	-20	A
$P_D@T_A=25^\circ C$	Total Power Dissipation	2.5	W
	Linear Derating Factor	0.02	W/°C
TSTG	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³	50	°C/W



Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	-30	-33	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-24V,V _{GS} =0V	-	-	-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =-250μA	-1	-1.6	-3	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-5.1A	-	43	55	mΩ
		V _{GS} =-4.5V, I _D =-4.2A	-	62	90	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-15V,I _D =-4.5A	4	7	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =-15V,V _{GS} =0V, F=1.0MHz	-	520	-	PF
Output Capacitance	C _{oss}		-	130	-	PF
Reverse Transfer Capacitance	C _{rss}		-	70	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-15V, I _D =-1A, V _{GS} =-10V,R _{GEN} =6Ω	-	7	-	nS
Turn-on Rise Time	t _r		-	13	-	nS
Turn-Off Delay Time	t _{d(off)}		-	14	-	nS
Turn-Off Fall Time	t _f		-	9	-	nS
Total Gate Charge	Q _g	V _{DS} =-15V,I _D =-5.1A,V _{GS} =-10V	-	11	-	nC
Gate-Source Charge	Q _{gs}		-	2.2	-	nC
Gate-Drain Charge	Q _{gd}		-	3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =-5.1A	-	-	-1.2	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production



Typical Electrical and Thermal Characteristics

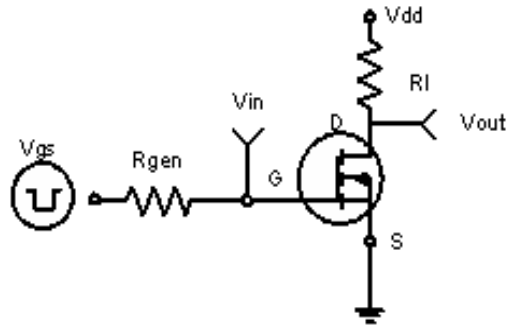


Figure 1: Switching Test Circuit

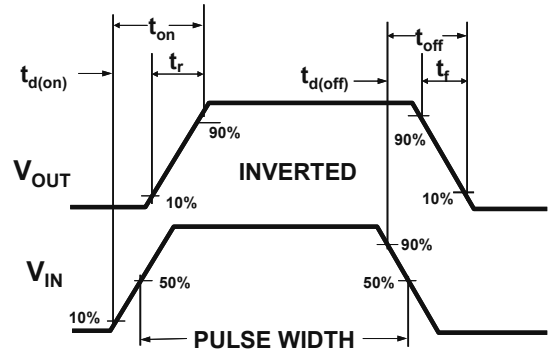


Figure 2: Switching Waveforms

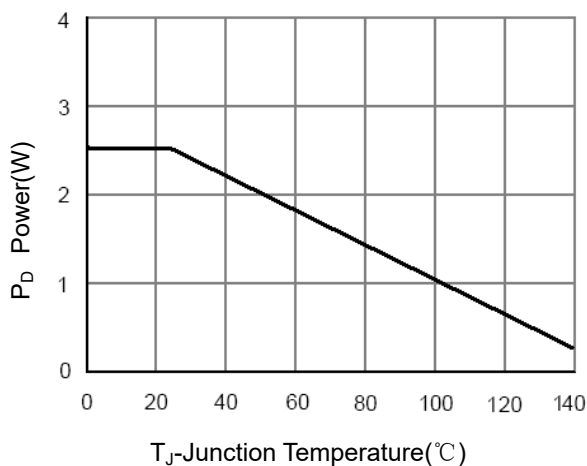


Figure 3 Power Dissipation

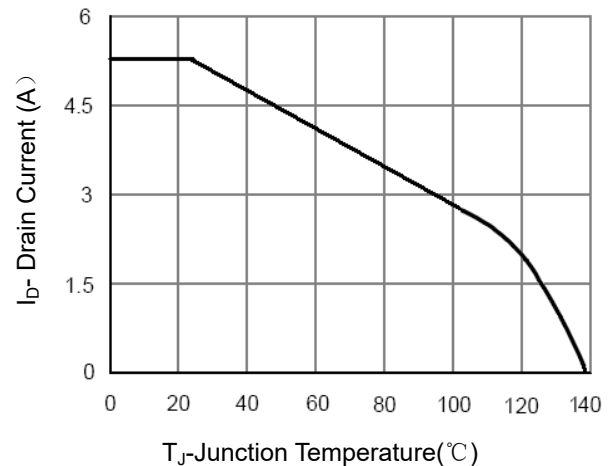


Figure 4 Drain Current

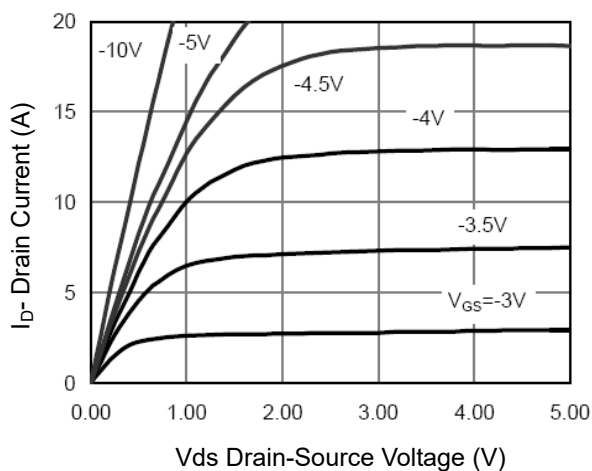


Figure 5 Output Characteristics

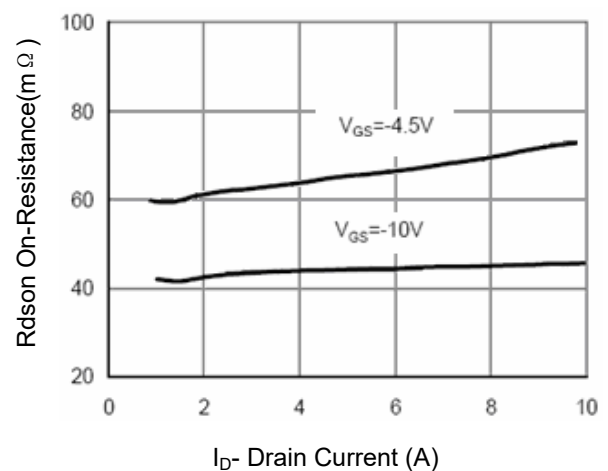


Figure 6 Drain-Source On-Resistance

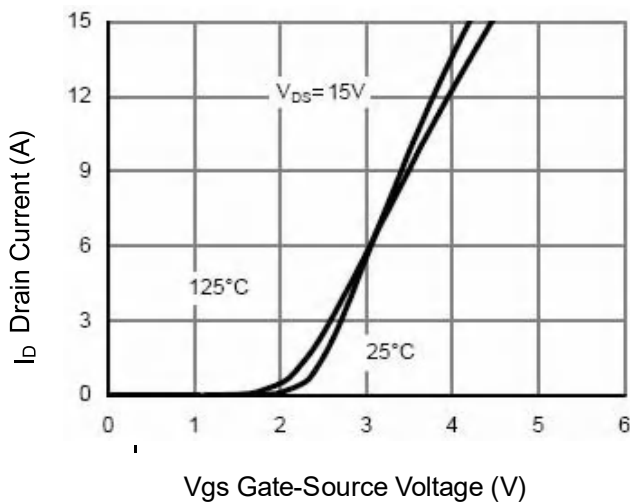


Figure 7 Transfer Characteristics

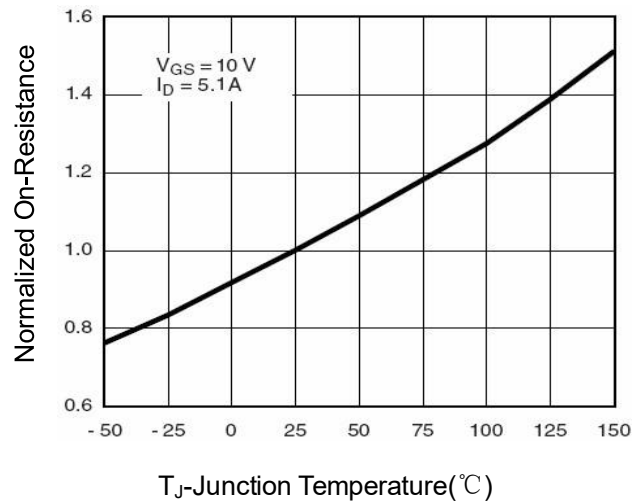


Figure 8 Drain-Source On-Resistance

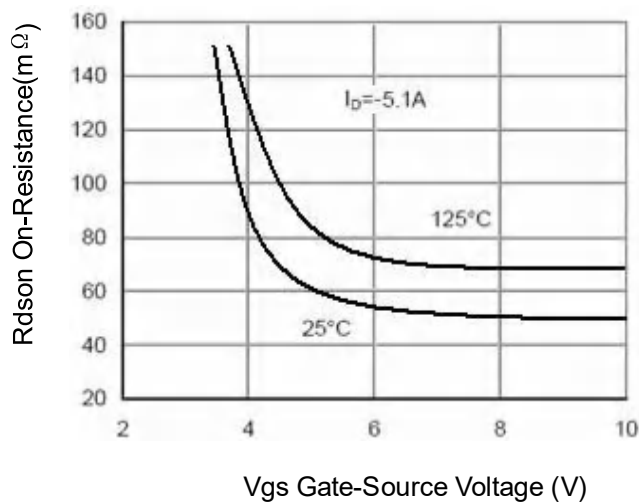


Figure 9 $R_{DS(on)}$ vs V_{GS}

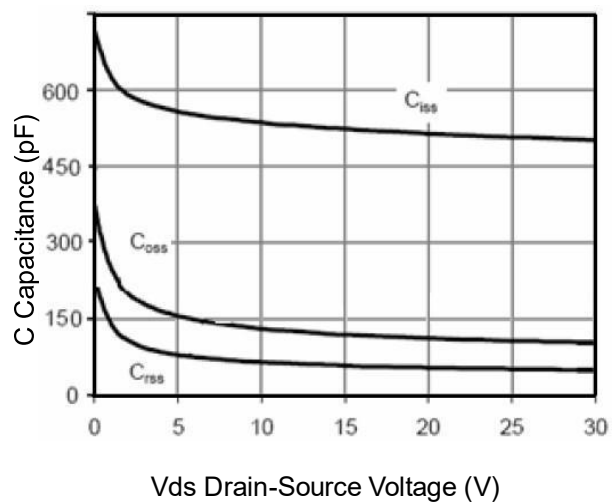


Figure 10 Capacitance vs V_{DS}

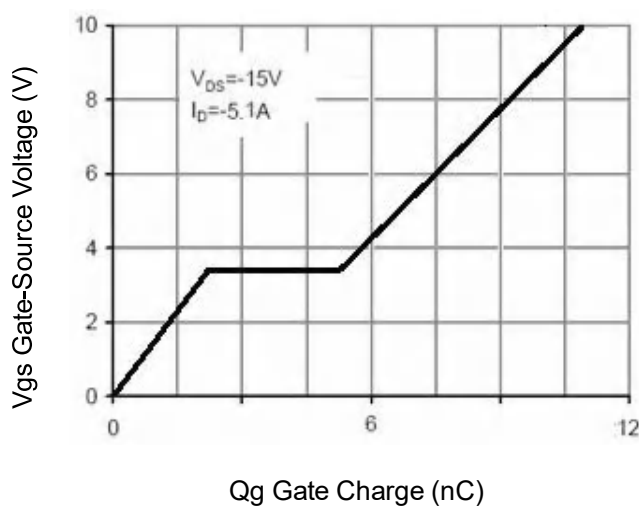


Figure 11 Gate Charge

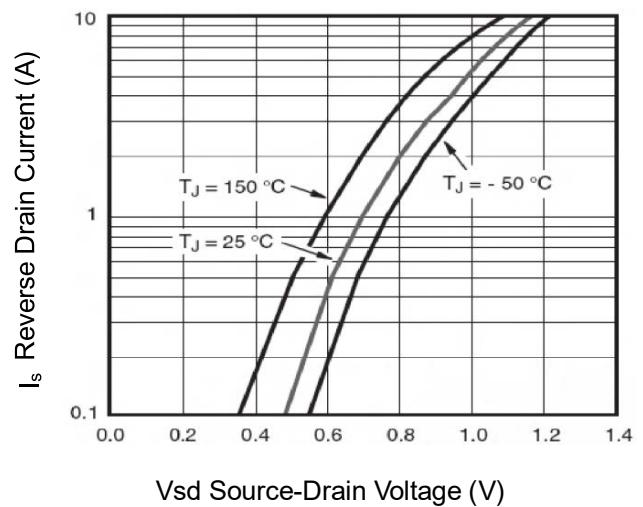
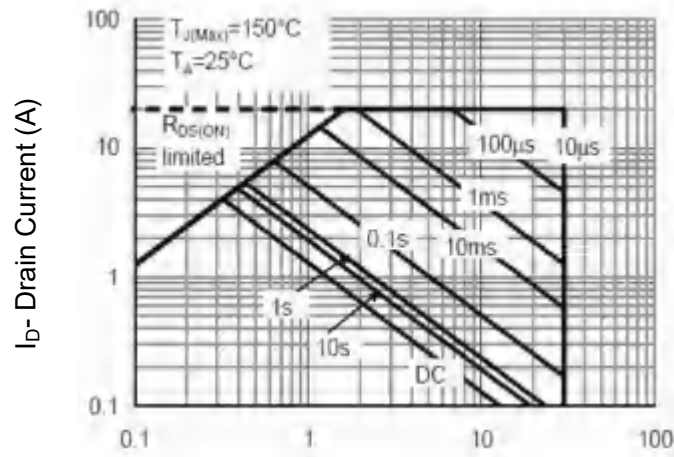
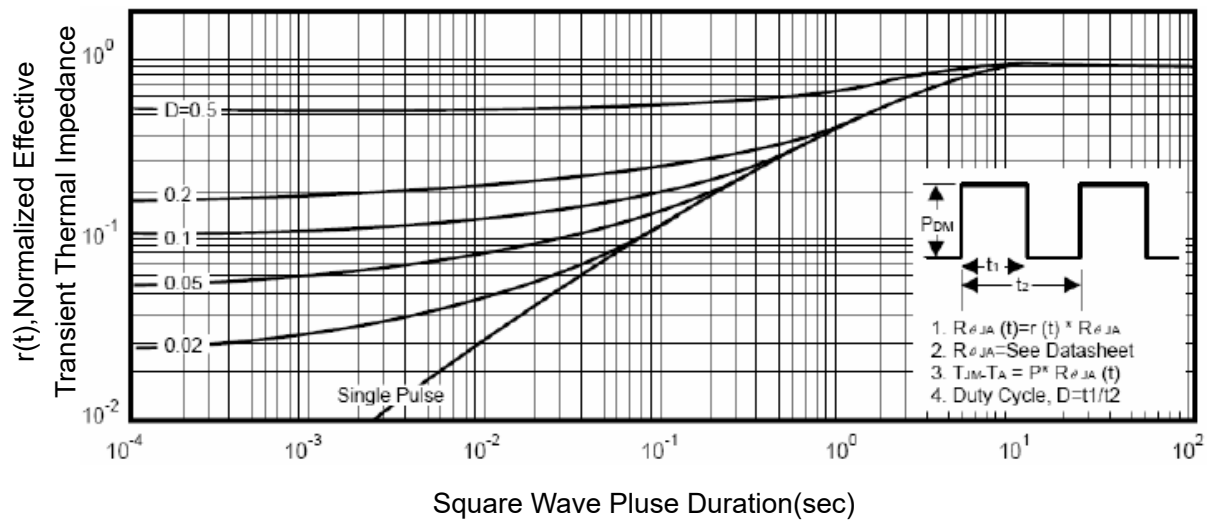


Figure 12 Source- Drain Diode Forward



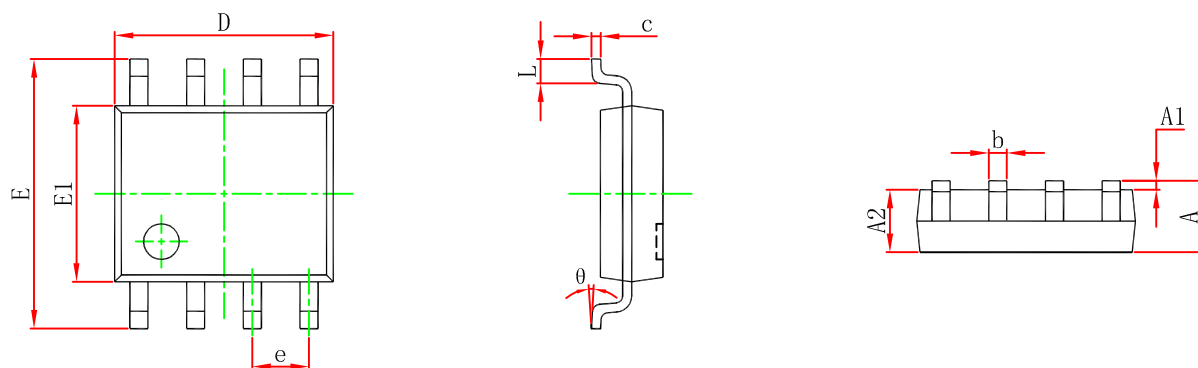
Vds Drain-Source Voltage (V)
Figure 13 Safe Operation Area



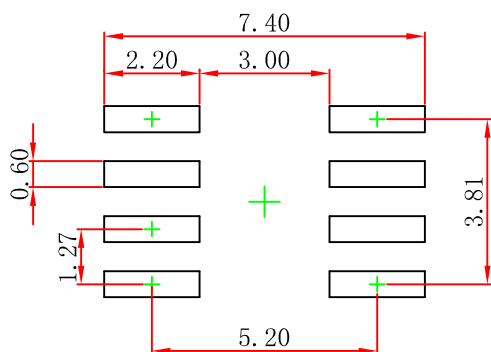
Square Wave Pluse Duration(sec)
Figure 14 Normalized Maximum Transient Thermal Impedance



SOP-8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Note:
1. Controlling dimension; in millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.



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