



JLHF600B120E62E7DN

L62 PACK module with Gen7 IGBT and Emitter Controlled 7 diode

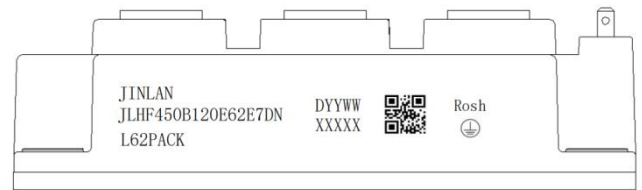


Features

- 1200V Trench Stop IGBTs
- $T_{vj\ op}=150^{\circ}\text{C}$
- V_{CEsat} with positive temperature coefficient
- 10 μs short circuit capability
- For higher switching frequencies up to 12kHz
- Standard housing
- 4 kV AC 1 min insulation
- Low inductance case
- Insulated copper baseplate using DBC technology
- High creepage and clearance distances



L62 Pack

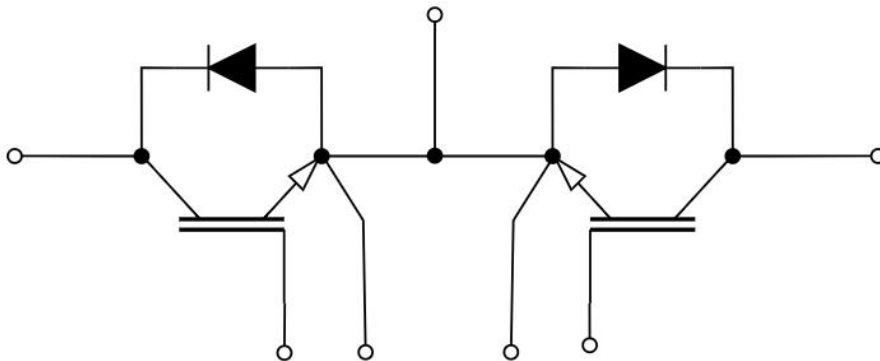


Typical Applications

- Matrix Inverter
- Bidirectional switch

JINLAN	= Company Name
JLHF600B120E62E7DN	= Specific Device Code
YYWW	= Year and Work Week Code
XXXXX	= Serial Number
QR code	= Custom Assembly Information

Description





Package Insulation coordination

Parameter	Symbol	Note or test condition	Values	Unit
Isolation test voltage	V_{ISOL}	RMS, f=50Hz, t=60s	4.0	kV
Internal isolation		basic insulation(class 1, IEC 61140)	Al_2O_3	
Creepage distance	d_{creep}	terminal to heatsink	29.0	mm
Creepage distance	d_{creep}	terminal to terminal	23.0	mm
Clearance	d_{clear}	terminal to heatsink	23.0	mm
Clearance	d_{clear}	terminal to terminal	11.0	mm
Comparative tracking index (electrical)	CTI		>500	
RTI Elec.	RTI	housing	140	°C

Package Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Stray Inductance	L_{CE}			--	20	--	nH
Module Lead Resistance, Terminal to Chip	$R_{CC'+EE'}$	$T_C=25^{\circ}C$, per switch		--	0.5	--	mΩ
Storage Temperature Range	T_{STG}			-40		125	°C
M	Mounting torque for module mounting	-Mounting according to valid application note	M5, Screw	3.0	--	6.0	Nm
M	Terminal connection torque	-Mounting according to valid application note	M6, Screw	2.5	--	5.0	Nm
Weight	G			--	340	--	g



IGBT

Absolute Maximum Ratings (T_C = 25°C unless otherwise noted)

Symbol	Description	Note or test condition		Value	Unit
V _{CES}	Collector-Emitter Voltage	T _{vj} = 25 °C		1200	V
I _{CDC}	Continuous DC collector current	T _{vj max} = 175 °C	T _C = 90 °C	600	A
I _{CRM}	Repetitive peak collector current	t _p limited by T _{vj op}		1200	A
V _{GES}	Gate-emitter peak voltage			±20	V

Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V _{CE(sat)}	Collector-Emitter Saturation Voltage	I _C = 600 A, V _{GE} = 15 V	T _{vj} = 25 °C	--	1.45	1.95	V
			T _{vj} = 150 °C	--	1.70	--	
			T _{vj} = 175 °C	--	1.75	--	
V _{GE(TH)}	Gate-Emitter Threshold Voltage	V _{GE} = V _{CE} , I _C = 5 mA, T _{vj} = 25°C		5.0	5.8	6.5	V
I _{CES}	Collector-Emitter Cutoff Current	V _{GE} = 0 V, V _{CE} = 1200V, T _{vj} = 25°C		--	--	100	uA
I _{GES}	Gate-Emitter Leakage Current	V _{GE} = ±30 V, V _{CE} = 0 V, T _{vj} = 25°C		--	--	±100	nA
R _{Gint}	Internal Gate Resistance	T _{vj} = 25 °C		--	1.34	--	Ω
C _{ies}	Input Capacitance	f = 100 kHz, T _{vj} = 25 °C, V _{CE} = 25 V, V _{GE} = 0 V		--	73.9	--	nF
C _{oes}	Out Capacitance			--	1.7	--	nF
C _{res}	Reverse Transfer			--	0.2	--	nF
Q _G	Gate Charge	V _{GE} = ±15 V, V _{CC} = 600 V		--	2.40	--	μC
t _{d(on)}	Turn-On Delay Time	I _C = 600 A, V _{CC} = 600 V, V _{GE} = 15 /-5V, R _G = 1.0 Ω	T _{vj} = 25 °C	--	0.441	--	μS
			T _{vj} = 150 °C	--	0.500	--	
			T _{vj} = 175 °C	--	0.507	--	
t _r	Rise Time	I _C = 600 A, V _{CC} = 600 V, V _{GE} = 15 /-5V, R _G = 1.0 Ω	T _{vj} = 25 °C	--	0.080	--	μS
			T _{vj} = 150 °C	--	0.096	--	
			T _{vj} = 175 °C	--	0.097	--	
t _{d(off)}	Turn-off Delay Time	I _C = 600 A, V _{CC} = 600 V, V _{GE} = 15 /-5V, R _{Goff} = 1.0 Ω	T _{vj} = 25 °C	--	0.896	--	μS
			T _{vj} = 150 °C	--	1.021	--	
			T _{vj} = 175 °C	--	1.043	--	
t _f	Fall Time	I _C = 600 A, V _{CC} = 600 V, V _{GE} = 15 /-5V, R _G = 1.0 Ω	T _{vj} = 25 °C	--	0.109	--	μS
			T _{vj} = 150 °C	--	0.244	--	
			T _{vj} = 175 °C	--	0.248	--	
E _{on}	Turn-On Switching Loss per Pulse	I _C = 600 A, V _{CC} = 600 V, V _{GE} = 15 /-5V, R _G = 1.0 Ω (T _{vj max} = 175 °C)	T _{vj} = 25 °C	--	13.52	--	mJ
			T _{vj} = 150 °C	--	26.94	--	
			T _{vj} = 175 °C	--	29.98	--	
E _{off}	Turn Off Switching Loss per Pulse	I _C = 600 A, V _{CC} = 600 V, V _{GE} = 15 /-5V, R _G = 1.0 Ω (T _{vj max} = 175 °C)	T _{vj} = 25 °C	--	58.73	--	mJ
			T _{vj} = 150 °C	--	78.24	--	
			T _{vj} = 175 °C	--	80.84	--	



I _{sc}	SC Data	V _{GE} ≤ 15 V, V _{CC} = 800 V, V _{CEmax} =V _{CES} -L _{sCE} .di/dt	t _p ≤ 10 μs, T _{vj} =150 °C	--	2173	--	A
			t _p ≤ 10 μs, T _{vj} =175 °C	--	2044	--	
R _{thJC}	Thermal resistance	Junction-to-Case (per IGBT)		--	0.053	0.064	K/W
T _{vj op}	Temperature under switching conditions			-40	--	175 ¹⁾	°C

¹⁾ T_{vj op} > 175 °C is only allowed for operation at overload conditions. For detailed specifications please refer to AN 2018-14.

Diode

Absolute Maximum Ratings (T_c = 25 °C unless otherwise noted)

Symbol	Description	Note or test condition	Value	Unit
V _{RRM}	Repetitive peak reverse voltage	T _{vj} = 25 °C	1200	V
I _F	Continuous DC forward current		600	A
I _{FRM}	Repetitive peak forward current	t _p = 1 ms	1200	A

Characteristics (T_c=25 °C unless otherwise noted)

Symbol	Parameter	Test Condition		Value			Unit
				Min	Typ	Max	
V _F	Diode Forward Voltage	I _F = 600 A, V _{GE} = 0 V	T _{vj} = 25 °C	--	2.00	2.80	V
			T _{vj} = 150 °C	--	1.95	--	
			T _{vj} = 175 °C	--	1.85	--	
Q _r	Recovered Charge	I _C = 600 A, V _{CC} = 600 V, V _{GE} = 15 /-5V, R _G = 1.0 Ω (T _{vj max} = 175 °C)	T _{vj} = 25 °C	--	10.1	--	μC
			T _{vj} = 150 °C	--	33.3	--	
			T _{vj} = 175 °C	--	40.7	--	
I _{RM}	Peak Reverse Recovery Current	I _C = 600 A, V _{CC} = 600 V, V _{GE} = 15 /-5V, R _G = 1.0 Ω (T _{vj max} = 175 °C)	T _{vj} = 25 °C	--	345	--	A
			T _{vj} = 150 °C	--	433	--	
			T _{vj} = 175 °C	--	456	--	
E _{rec}	Reverse Recovery Energy	I _C = 600 A, V _{CC} = 600 V, V _{GE} = 15 /-5V, R _G = 1.0 Ω (T _{vj max} = 175 °C)	T _{vj} = 25 °C	--	10.8	--	mJ
			T _{vj} = 150 °C	--	29.6	--	
			T _{vj} = 175 °C	--	34.5	--	
R _{thJC}	Thermal resistance, junction to case	per diode		--	0.076	0.086	K/W
T _{vj op}	Temperature under switching conditions			-40	--	175 ²⁾	°C

²⁾ T_{vj op} > 175 °C is only allowed for operation at overload conditions. For detailed specifications please refer to AN 2018-14.

The diagram illustrates a two-stage CMOS differential amplifier. The first stage (left) has inputs 1 and 2, and outputs 6 and 7. It consists of a differential pair of NMOS transistors with a PMOS load and a current source. The second stage (right) has inputs 5 and 4, and outputs 3 and 3. It also consists of a differential pair of NMOS transistors with a PMOS load and a current source. The two stages are connected in a cascaded manner.

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REVISION HISTORY

Document version	Date of release	Description of changes
Rev.00	2024-05-31	Preliminary Data



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