

Description

The SX40P02DF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = -20V$ $I_D = -40A$

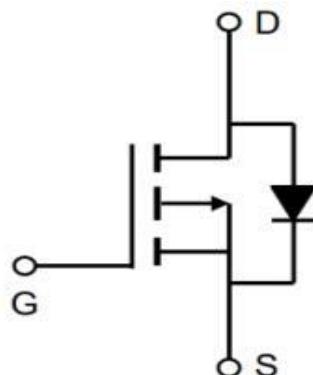
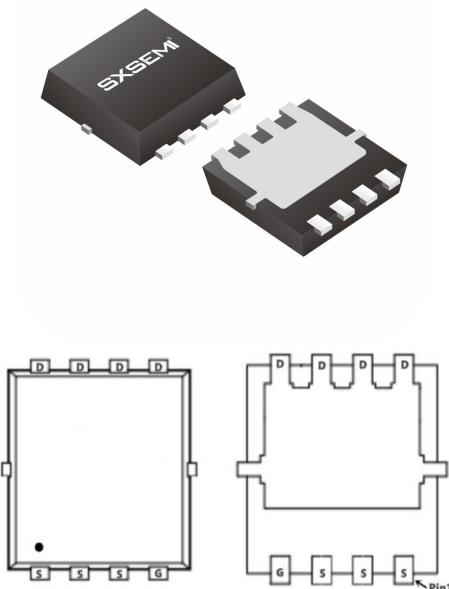
$R_{DS(ON)} < 12m\Omega$ @ $V_{GS} = -4.5V$

Application

Battery protection

Load switch

Uninterruptible power supply

PDFN3*3-8L**Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)**

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-Source Voltage	± 12	V
$I_D @ T_c=25^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V^1$	-40	A
$I_D @ T_c=70^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V^1$	-20	A
I_{DM}	Pulsed Drain Current ²	-160	A
$P_D @ T_c=25^\circ C$	Total Power Dissipation ³	60	W
$P_D @ T_c=70^\circ C$	Total Power Dissipation ³	30	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C
R_{eJA}	Thermal Resistance Junction-Ambient ¹	83	°C/W
R_{eJA}	Thermal Resistance Junction-Ambient ¹ ($t \leq 10s$)	52	°C/W
R_{eJC}	Thermal Resistance Junction-Case ¹	4.5	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=-250\mu\text{A}$	-20	-22	---	V
$\Delta BVDSS/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	-0.012	---	$\text{V}/^\circ\text{C}$
RDS(ON)	Static Drain-Source On-Resistance ²	$V_{GS}=-4.5\text{V}$, $I_D=-10\text{A}$	---	8	12	$\text{m}\Omega$
RDS(ON)	Static Drain-Source On-Resistance ²	$V_{GS}=-2.5\text{V}$, $I_D=-5.0\text{A}$	---	11	16	
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=-250\mu\text{A}$	-0.4	-0.65	-1.0	V
$\Delta V_{GS(\text{th})}$	$V_{GS(\text{th})}$ Temperature Coefficient		---	2.94	---	$\text{mV}/^\circ\text{C}$
IDSS	Drain-Source Leakage Current	$V_{DS}=-20\text{V}$, $V_{GS}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	uA
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 12\text{V}$, $V_{DS}=0\text{V}$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=-10\text{V}$, $I_D=-10\text{A}$	12	---	---	S
Qg	Total Gate Charge (-4.5V)	$V_{DS}=-10\text{V}$, $V_{GS}=-4.5\text{V}$, $I_D=-10\text{A}$	---	63	---	nC
Qgs	Gate-Source Charge		---	9.1	---	
Qgd	Gate-Drain Charge		---	13	---	
Td(on)	Turn-On Delay Time	$V_{DD}=-10\text{V}$, $V_{GS}=-4.5\text{V}$, $R_G=6.0\Omega$, $I_D=1\text{A}$	---	10	---	ns
Tr	Rise Time		---	15	---	
Td(off)	Turn-Off Delay Time		---	110	---	
Tr	Fall Time		---	70	---	
Ciss	Input Capacitance	$V_{DS}=-15\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	---	1600	---	pF
Coss	Output Capacitance		---	350	---	
Crss	Reverse Transfer Capacitance		---	300	---	
IS	Continuous Source Current ^{1,4}	$V_G=V_D=0\text{V}$, Force Current	---	---	-50	A
VSD	Diode Forward Voltage ²	$V_{GS}=0\text{V}$, $I_S=-15\text{A}$, $T_J=25^\circ\text{C}$	---	---	-1.2	V

Note :

- 1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3、The EAS data shows Max. rating . The test condition is $VDD=-16\text{V}$, $VGS=-10\text{V}$, $L=0.1\text{mH}$, $IAS=12\text{A}$
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

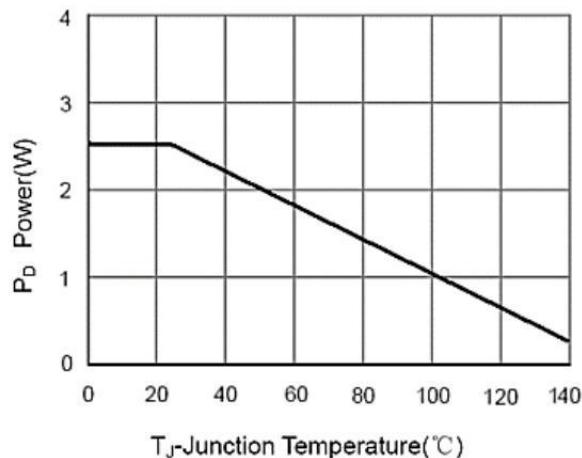


Figure 1 : Power Dissipation

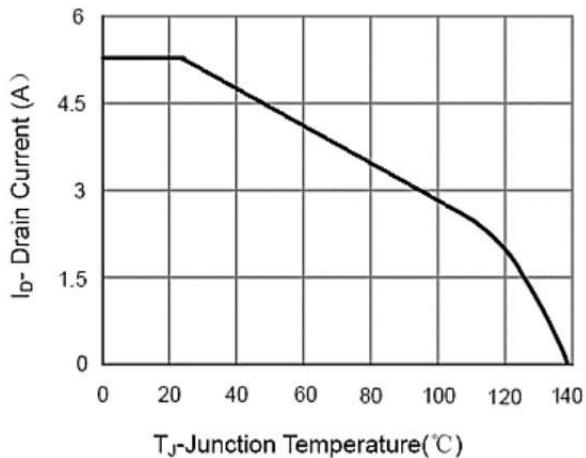


Figure 2 : Drain Current

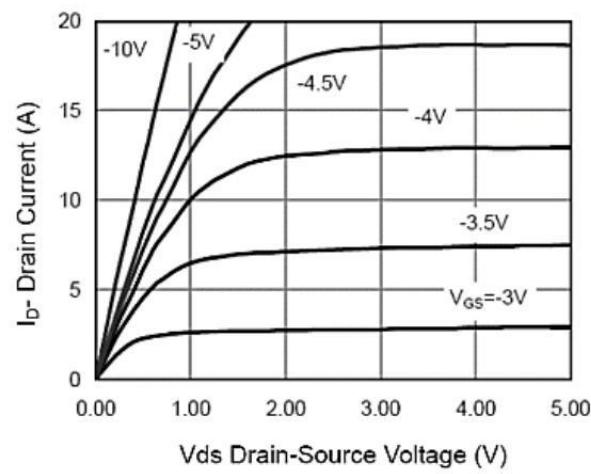


Figure 3: Output Characteristics

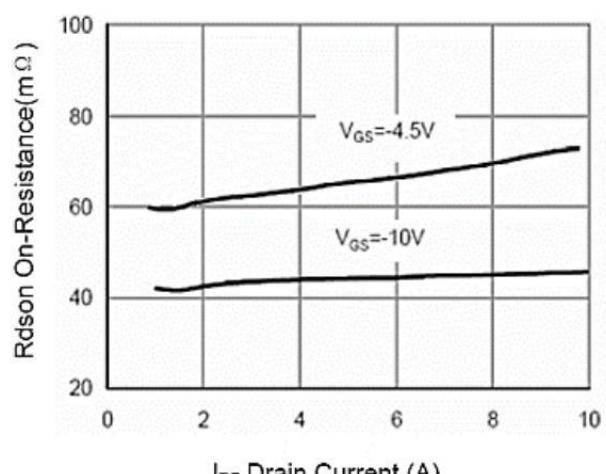


Figure 4 : Drain-Source On-Resistance

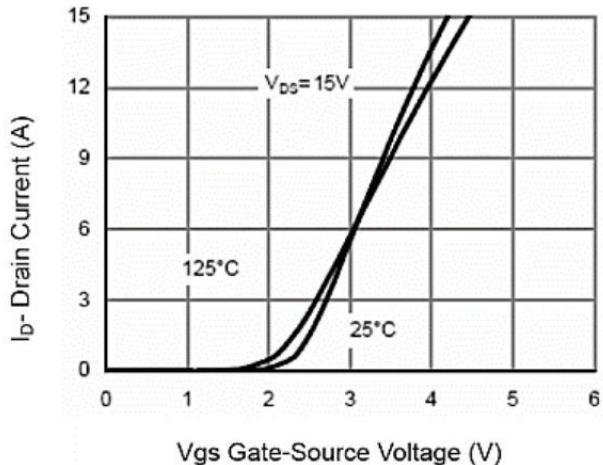


Figure 5 : Transfer Characteristics

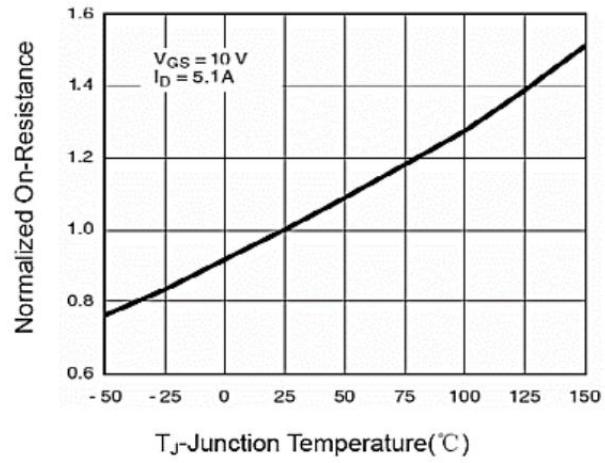


Figure 6 : Drain-Source On-Resistance

Typical Characteristics

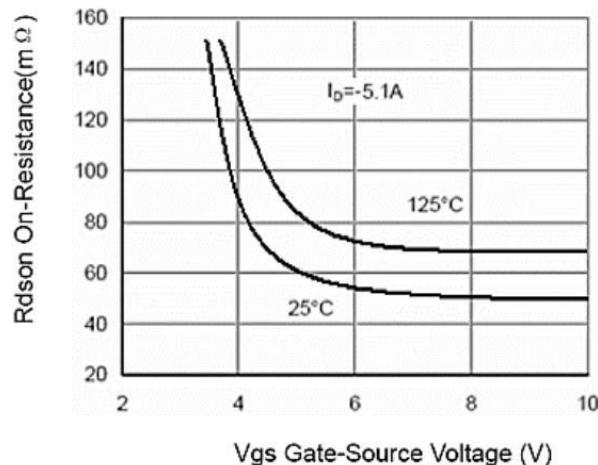


Figure 7 : $R_{DS(on)}$ vs V_{GS}

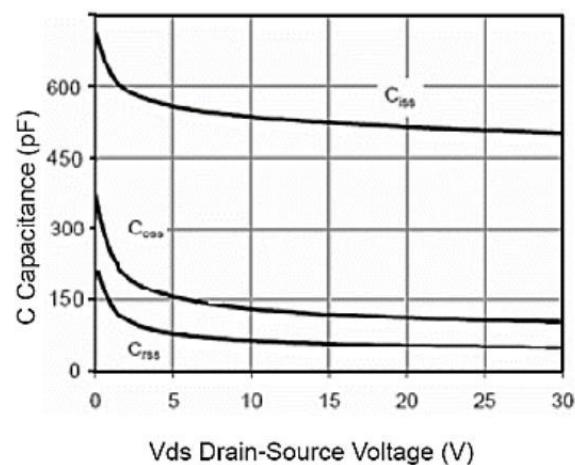


Figure 8 : Capacitance vs V_{DS}

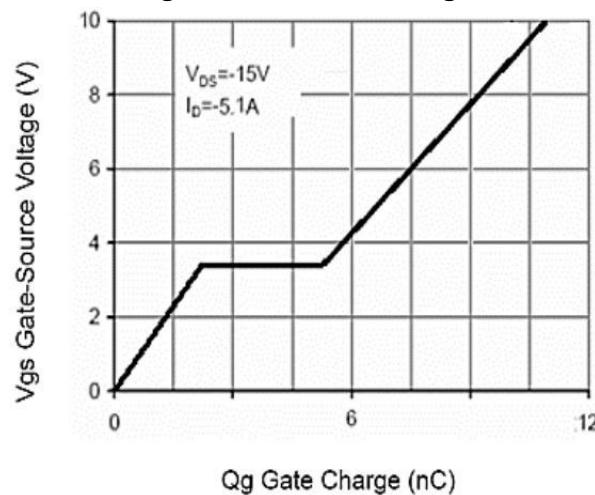


Figure 9 : Gate Charge

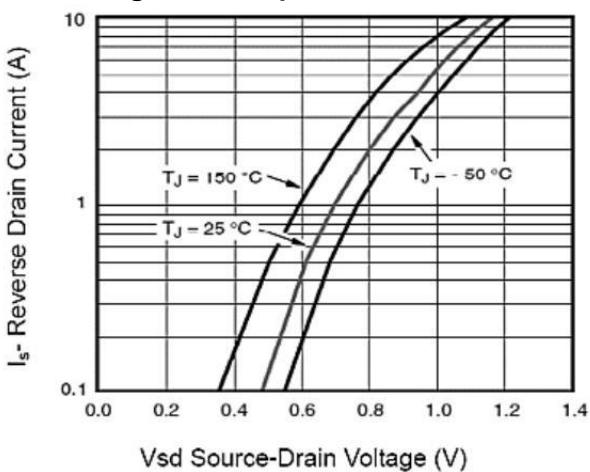


Figure 10: Source-Drain Diode Forward

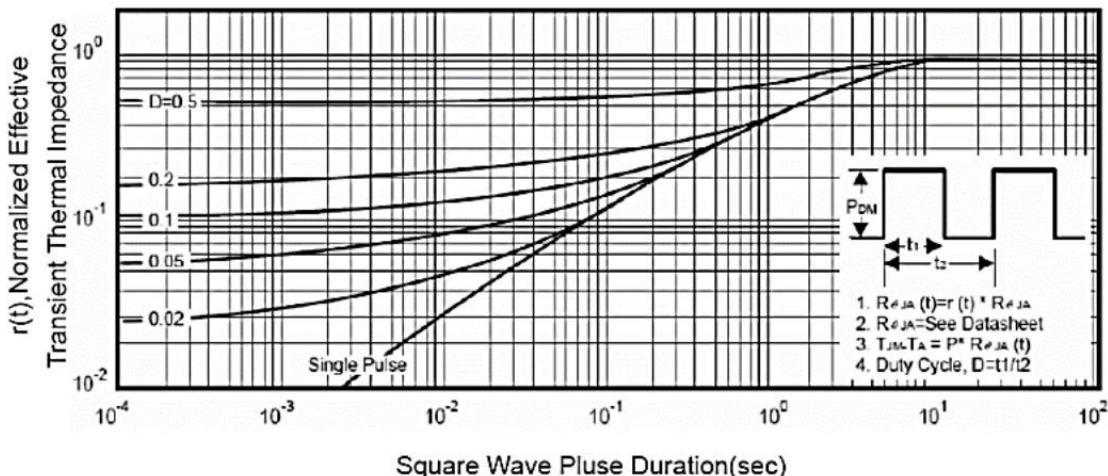
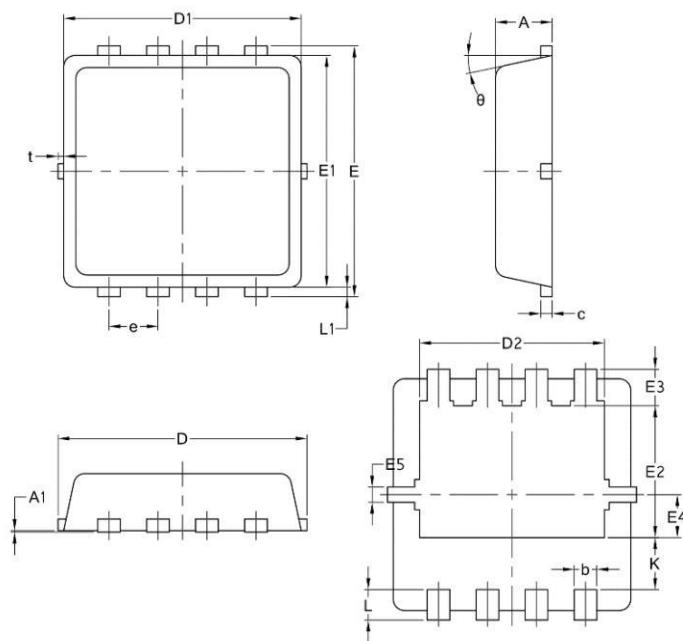


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

Package Mechanical Data-DFN3*3-8L-JQ Single



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
Φ	10	12	14

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
TAPING	PDFN3*3-8L		5000