MAX7219 Serially Interfaced, 8-Digit LED Display Drivers

1. General Description

1.1 Description

The MAX7219 are compact, serial input/output common-cathode display drivers that interface microprocessors (uPs) to 7-segment numeric LED displays of up to 8 digits, bar-graph displays, or 64 individual LEDs. Included on-chip are a BCD code-B decoder, multiplex scan circuitry, segment and digit drivers, and an 8x8 static RAM that stores each digit.Only one external resistor is required to set the segment current for all LEDs.

A convenient 3-wire serial interface connects to all common μPs. Individual digits may be addressed and updated without rewriting the entire display. The MAX7219 also allow the user to select code-B decoding or no-decode for each digit.

The devices include a 150μA low-power shutdown mode, analog and digital brightness control, a scan-limit register that allows the user to display from 1 to 8 digits, and a test mode that forces all LEDs on.

1.2 Features

- Individual LED Segment Control
- Decode/No-Decode Digit Selection
- 150μA Low-Power Shutdown (Data Retained)
- Digital and Analog Brightness Control
- Display Blanked on Power-Up
- Drive Common-Cathode LED Display

1.3 Ordering Information

PART NUMBER	PACKAGE
MAX7219	DIP
	SOP-W
	SSOP

2. Connection Diagrams and Pin Description

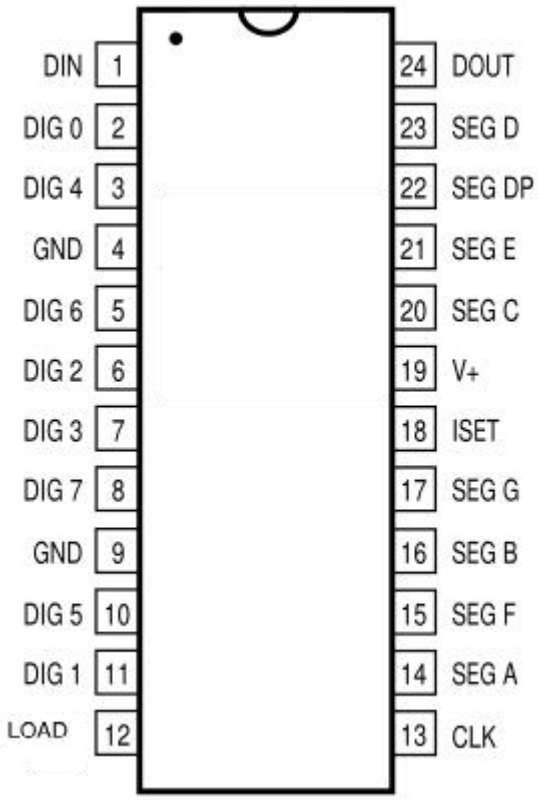


Figure 2.1 Top View

PIN No.	NAME	I/O	FUNCTION
1	DIN	I	Serial-Data Input. Data is loaded into the internal 16-bit shift register on CLK's rising edge.
2,3,5-8,10,11	DIG 0–DIG 7	O	Eight-Digit Drive Lines that sink current from the display common cathode. The MAX7219 pulls the digit outputs to V+ when turned off.
4, 9	GND	-	Ground (both GND pins must be connected)
12	LOAD	I	Load-Data Input. The last 16 bits of serial data are latched on LOAD's rising edge.
13	CLK	I	Serial-Clock Input. On CLK's rising edge, data is shifted into the internal shift register. On CLK's falling edge, data is clocked out of DOUT.
14-17,20-23	SEG A - SEG G , SEG DP	O	Seven Segment Drives and Decimal Point Drive that source current to the display. On the MAX7219, when a segment driver is turned off it is pulled to GND.
18	ISET	I	Connect to VDD through a resistor (RSET) to set the peak segment current (Refer to Selecting RSET Resistor section).
19	V+	-	Positive Supply Voltage. Connect to +5V.
24	DOUT	O	Serial-Data Output. The data into DIN is valid at DOUT 16.5 clock cycles later. This pin is used to daisy-chain several MAX7219 and is never high-impedance.

3. System Diagram

3.1 Function Diagram

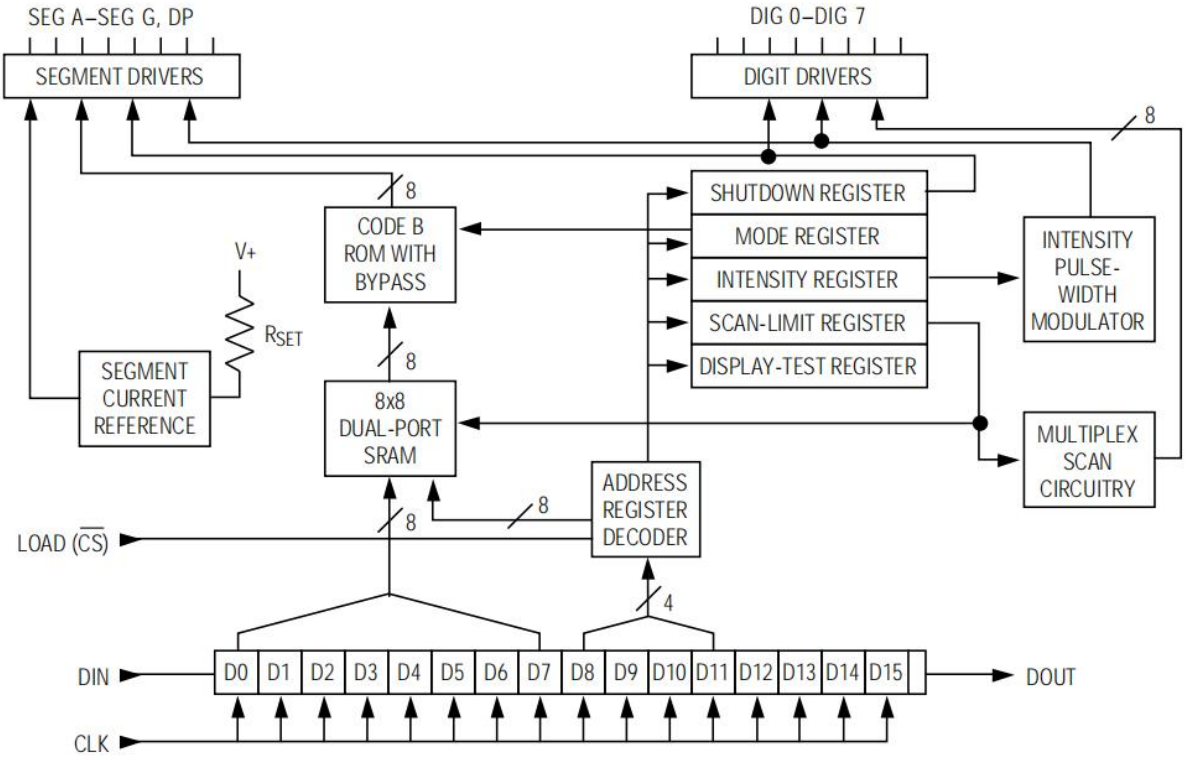


Figure 3.1：MAX7219 Function Diagram

3.2 Timing Diagram

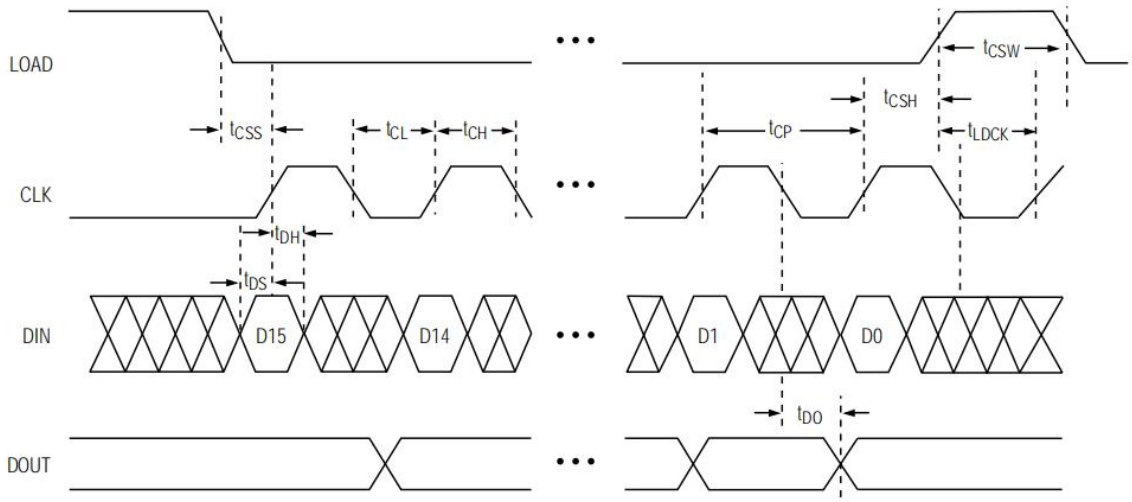


Figure 3.2：MAX7219 Timing Diagram

4. Specifications

4.1 Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Unit
V+	Supply Voltage	-0.3	6	V
DIN, CLK, LOAD	Input Voltage (Referenced to GND)	-0.3	6	V
All Other Pins	Input Voltage (Referenced to GND)	-0.3	V+ + 0.3	V
DIG0–DIG7 Sink Current	Sink Current	-	500	mA
SEGA–G, DP Source Current	Source Current	-	100	mA
T_J	Junction Temperature Range	-	150	℃
T_{OP}	Operating Temperature Range	-40	85	℃
T_{stg}	Storage Temperature	-65	150	℃

Absolute maximum ratings are those values beyond which the device could be permanently damaged,These are stress ratings only,which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions..

4.2 Recommended Operating Conditions

Symbol	Parameter	Test Condition	MIN	MAX	Unit
V+	Operating Supply Voltage		4	5.5	V

4.3 Electrical Characteristics

(V+ = 5V ±10%, RSET = 9.53kΩ ±1%, TA = 25℃, unless otherwise noted.)

Symbol	Parameter	Test Condition	MIN	TYP	MAX	Unit
DC Specifications						
I+	Shutdown Supply Current	All digital inputs at V+ or GND, TA= +25°C	-	-	150	uA
I+	Operating Supply Current	RSET = open circuit	-	-	8	mA
		All segments and decimal point on, $I_{SEG\_}$ = -40mA	-	330	-	
f_{OSC}	Display Scan Rate	8 digits scanned	500	800	1300	Hz
I_{DIGIT}	Digit Drive Sink Current	V+ = 5V, VOUT = 0.65V	320	--	-	mA
I_{SEG}	Segment Drive Source Current	TA = +25°C, V+ = 5V, VOUT = (V+ - 1V)	-30	-40	-45	mA
I_{DIGIT}	Digit Drive Source Current	Digit off, V_{DIGIT} = (V+ - 0.3V)	-2	-	-	mA
I_{SEG}	Segment Drive Sink Current	Segment off, VSEG = 0.3V	5	-	-	mA
LOGIC INPUTS						
I_{IH}, I_{IL}	Input Current DIN, CLK,LOAD	VIN = 0V or V+	-1	-	1	uA
V_{IH}	Logic High Input Voltage		3.5	-	-	V
V_{IL}	Logic Low Input Voltage		-	-	0.8	V
V_{OH}	Output High Voltage	DOUT, I_{SOURCE}= -1mA	V+ - 1	-	-	V
V_{OL}	Output Low Voltage	DOUT, I_{SINK} = 1.6mA	-	-	0.4	V
ΔVI	Hysteresis Voltage	DIN, CLK, LOAD	-	1	-	V

5. Detailed Description

5.1 Serial-Addressing Modes

For the MAX7219, serial data at DIN, sent in 16-bit packets, is shifted into the internal 16-bit shift register with each rising edge of CLK regardless of the state of LOAD.Data at DIN is propagated through the shift register and appears at DOUT 16.5 clock cycles later. The data is then latched into either the digit or control registers on the rising edge of LOAD. LOAD must go high concurrently with or after the 16th rising clock edge, but before the next rising clock edge or data will be lost. Data at DIN is propagated through the shift register and appears at DOUT 16.5clock cycles later. Data is clocked out on the falling edge of CLK. Data bits are labeled D0–D15 (Table 1).D8–D11 contain the register address. D0–D7 contain the data, and D12–D15 are “don’t care” bits. The first received is D15, the most significant bit (MSB).

Table1. Serial-Data Format (16 Bits)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	ADDRESS				MSB			DATA				LSB

5.2 Digit and Control Registers

Table 2 lists the 14 addressable digit and control registers. The digit registers are realized with an on-chip,8x8 dual-port SRAM. They are addressed directly sothat individual digits can be updated and retain data as long as V+ typically exceeds 2V. The control registers consist of decode mode, display intensity, scan limit (number of scanned digits), shutdown, and display test (all LEDs on).

Table 2. Register Address Map

REGISTER	ADDRESS					HEX CODE
	D15–D12	D11	D10	D9	D8	
No-Op	X	0	0	0	0	X0
Digit 0	X	0	0	0	1	X1
Digit 1	X	0	0	1	0	X2
Digit 2	X	0	0	1	1	X3
Digit 3	X	0	1	0	0	X4
Digit 4	X	0	1	0	1	X5
Digit 5	X	0	1	1	0	X6
Digit 6	X	0	1	1	1	X7
Digit 7	X	1	0	0	0	X8
Decode Mode	X	1	0	0	1	X9
Intensity	X	1	0	1	0	XA
Scan Limit	X	1	0	1	1	XB
Shutdown	X	1	1	0	0	XC
Display Test	X	1	1	1	1	XF

5.3 Shutdown Mode

When the MAX7219 is in shutdown mode, the scan oscillator is halted, all segment current sources are pulled to ground, and all digit drivers are pulled to V+, thereby blanking the display. Data in the digit and control registers remains unaltered. Shutdown can be used to save power or as an alarm to flash the display by successively entering and leaving shutdown mode. For minimum supply current in shutdown mode, logic inputs should be at ground or V+ (CMOS-logic levels).

Typically, it takes less than 250us for the MAX7219 to leave shutdown mode. The display driver can be programmed while in shutdown mode, and shutdown mode can be overridden by the display-test function.

Table 3. Shutdown Register Format (Address (Hex) = XC)

MODE	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Shutdown Mode	XC	X	X	X	X	X	X	X	0
Normal Operation	XC	X	X	X	X	X	X	X	1

5.4 Initial Power-Up

On initial power-up, all control registers are reset, the display is blanked, and the MAX7219 enter shutdown mode. Program the display driver prior to display use. Otherwise, it will initially be set to scan one digit, it will not decode data in the data registers, and the intensity register will be set to its minimum value.

5.5 Decode-Mode Register

The decode-mode register sets BCD code B (0-9, E, H,L, P, and -) or no-decode operation for each digit. Each bit in the register corresponds to one digit. A logic high selects code B decoding while logic low bypasses the decoder. Examples of the decode mode control-register format are shown in Table 4.

When the code B decode mode is used, the decoder looks only at the lower nibble of the data in the digit registers (D3–D0), disregarding bits D4–D6. D7, which sets the decimal point (SEG DP), is independent of the decoder and is positive logic (D7 = 1 turns the decimal point on). Table 5 lists the code B font.

When no-decode is selected, data bits D7–D0 correspond to the segment lines of the MAX7219

Table 6 shows the one-to-one pairing of each data bit to the appropriate segment line.

Table 4. Decode-Mode Register Examples (Address (Hex) = X9)

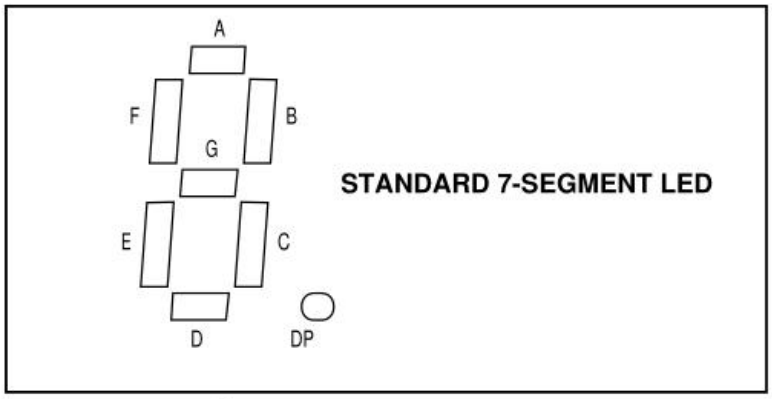
DECODE MODE	REGISTER DATA								HEX CODE
	D7	D6	D5	D4	D3	D2	D1	D0	
No decode for digits 7–0	0	0	0	0	0	0	0	0	00
Code B decode for digit 0 No decode for digits 7–1	0	0	0	0	0	0	0	1	01
Code B decode for digits 3–0 No decode for digits 7–4	0	0	0	0	1	1	1	1	0F
Code B decode for digits 7–0	1	1	1	1	1	1	1	1	FF

Table 5. Code B Font

7-SEGMENT CHARACTER	REGISTER DATA						ON SEGMENTS = 1							
	D7*	D6–D4	D3	D2	D1	D0	DP*	A	B	C	D	E	F	G
0		X	0	0	0	0		1	1	1	1	1	1	0
1		X	0	0	0	1		0	1	1	0	0	0	0
2		X	0	0	1	0		1	1	0	1	1	0	1
3		X	0	0	1	1		1	1	1	1	0	0	1
4		X	0	1	0	0		0	1	1	0	0	1	1
5		X	0	1	0	1		1	0	1	1	0	1	1
6		X	0	1	1	0		1	0	1	1	1	1	1
7		X	0	1	1	1		1	1	1	0	0	0	0
8		X	1	0	0	0		1	1	1	1	1	1	1
9		X	1	0	0	1		1	1	1	1	0	1	1
—		X	1	0	1	0		0	0	0	0	0	0	1
E		X	1	0	1	1		1	0	0	1	1	1	1
H		X	1	1	0	0		0	1	1	0	1	1	1
L		X	1	1	0	1		0	0	0	1	1	1	0
P		X	1	1	1	0		1	1	0	0	1	1	1
blank		X	1	1	1	1		0	0	0	0	0	0	0

*The decimal point is set by bit D7 = 1

Table 6. No-Decode Mode Data Bits and Corresponding Segment Lines



	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Corresponding Segment Line	DP	A	B	C	D	E	F	G

5.6 Intensity Control and Interdigit Blanking

The MAX7219 allow display brightness to be controlled with an external resistor (RSET) connected between V+ and ISET. The peak current sourced from the segment drivers is nominally 100 times the current entering ISET. This resistor can either be fixed or variable to allow brightness adjustment from the front panel. Its minimum value should be 9.53Ω, which typically sets the segment current at 40mA. Display brightness can also be controlled digitally by using the intensity register.

Digital control of display brightness is provided by an internal pulse-width modulator, which is controlled by the lower nibble of the intensity register. The modulator scales the average segment current in 16 steps from a maximum of 31/32 down to 1/32 of the peak current set by RSET . Table 7 lists the intensity register format. The minimum interdigit blanking time is set to 1/32 of a cycle.

Table 7. Intensity Register Format (Address (Hex) = XA)

DUTY CYCLE	D7	D6	D5	D4	D3	D2	D1	D0	HEX CODE
1/32 (min on)	X	X	X	X	0	0	0	0	X0
3/32	X	X	X	X	0	0	0	1	X1
5/32	X	X	X	X	0	0	1	0	X2
7/32	X	X	X	X	0	0	1	1	X3
9/32	X	X	X	X	0	1	0	0	X4
11/32	X	X	X	X	0	1	0	1	X5
13/32	X	X	X	X	0	1	1	0	X6
15/32	X	X	X	X	0	1	1	1	X7
17/32	X	X	X	X	1	0	0	0	X8
19/32	X	X	X	X	1	0	0	1	X9
21/32	X	X	X	X	1	0	1	0	XA
23/32	X	X	X	X	1	0	1	1	XB
25/32	X	X	X	X	1	1	0	0	XC
27/32	X	X	X	X	1	1	0	1	XD
29/32	X	X	X	X	1	1	1	0	XE
31/32	X	X	X	X	1	1	1	1	XF

5.7 Scan-Limit Register

The scan-limit register sets how many digits are displayed, from 1 to 8. They are displayed in a multiplexed manner with a typical display scan rate of 800Hz with 8 digits displayed. If fewer digits are displayed, the scan rate is 8 f_{OSC}/N, where N is the number of digits scanned. Since the number of scanned digits affects the display brightness, the scan-limit register should not be used to blank portions of the display (such as leading zero suppression). Table 8 lists the scan-limit register format.scanned. Since the number of scanned digits affects the display brightness, the scan-limit register should not be used to blank portions of the display (such as leading zero suppression). Table 8 lists the scan-limit register format.

If the scan-limit register is set for three digits or less, individual digit drivers will dissipate excessive amounts of power. Consequently, the value of the RSET resistor must be adjusted according to the number of digits displayed, to limit individual digit driver power dissipation.Table 9 lists the number of digits displayed and the corresponding maximum recommended segment current when the digit drivers are used.

Table 8. Scan-Limit Register Format (Address (Hex) = XB)

SCAN LIMIT	REGISTER DATA								HEX CODE
	D7	D6	D5	D4	D3	D2	D1	D0	
Display digit 0 only*	X	X	X	X	X	0	0	0	X0
Display digits 0 & 1*	X	X	X	X	X	0	0	1	X1
Display digits 0 1 2*	X	X	X	X	X	0	1	0	X2
Display digits 0 1 2 3	X	X	X	X	X	0	1	1	X3
Display digits 0 1 2 3 4	X	X	X	X	X	1	0	0	X4
Display digits 0 1 2 3 4 5	X	X	X	X	X	1	0	1	X5
Display digits 0 1 2 3 4 5 6	X	X	X	X	X	1	1	0	X6
Display digits 0 1 2 3 4 5 6 7	X	X	X	X	X	1	1	1	X7

*See *Scan-Limit Register* section for application.

Table 9. Maximum Segment Current for 1-, 2-, or 3-Digit Displays

NUMBER OF DIGITS DISPLAYED	MAXIMUM SEGMENT CURRENT (mA)
1	10
2	20
3	30

5.8 Display-Test Register

The display-test register operates in two modes: normal and display test. Display-test mode turns all LEDs on by overriding, but not altering, all controls and digit registers (including the shutdown register). In display-test mode, 8 digits are scanned and the duty cycle is 31/32. Table 10 lists the display-test register format.

Table 10. Display-Test Register Format(Address (Hex) = XF)

MODE	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Normal Operation	X	X	X	X	X	X	X	0
Display Test Mode	X	X	X	X	X	X	X	1

Note: The MAX7219 remain in display-test mode(all LEDs on) until the display-test register is reconfigured for normal operation.

5.9 No-Op Register

The no-op register is used when cascading MAX7219s . Connect all devices' LOAD inputs together and connect DOUT to DIN on adjacent devices. DOUT is a CMOS logic-level output that easily drives DIN of successively cascaded parts. (Refer to the Serial Addressing Modes section for detailed information on serial input/output timing.) For example, if four MAX7219s are cascaded, then to write to the fourth chip, sent the desired 16-bit word, followed by three no-op codes (hex XX0X, see Table 2). When LOAD goes high, data is latched in all devices. The first three chips receive no-op commands, and the fourth receives the intended data.

6. Applications Information

6.1 Supply Bypassing and Wiring

To minimize power-supply ripple due to the peak digit driver currents, connect a 10µF electrolytic and a 0.1µF ceramic capacitor between V+ and GND as close to the device as possible. The MAX7219 should be placed in close proximity to the LED display, and connections should be kept as short as possible to minimize the effects of wiring inductance and electromagnetic interference. Also, both GND pins must be connected to ground.

6.2 Selecting RSET Resistor and Using External Drivers

The current per segment is approximately 100 times the current in ISET. To select RSET, see Table 11. The MAX7219's maximum recommended segment current is 40mA. For segment current levels

above these levels, external digit drivers will be needed. In this application, the MAX7219 serve only as controllers for other high-current drivers or transistors. Therefore, to conserve power, use RSET = 47kΩ when using external current sources as segment drivers.

Table 11. RSET vs. Segment Current and LED Forward Voltage

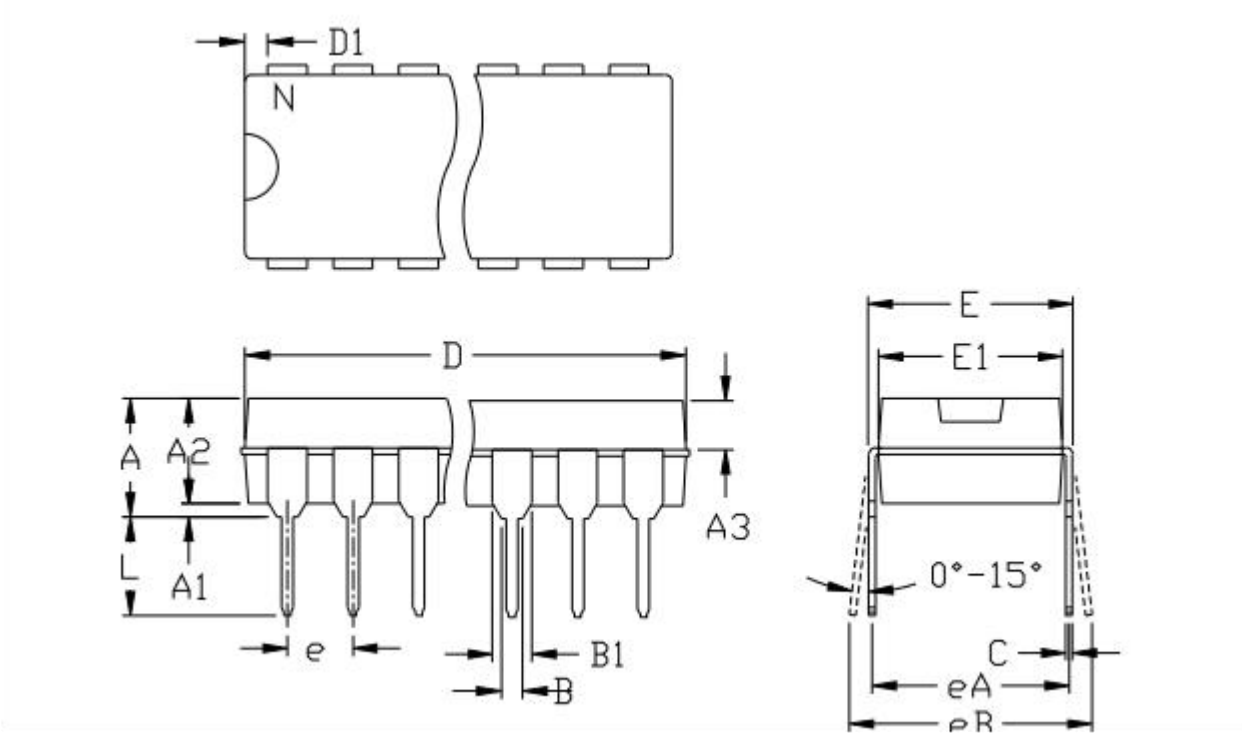
I_{SEG} (mA)	V_{LED} (V)				
	1.5	2.0	2.5	3.0	3.5
40	12.2	11.8	11.0	10.6	9.69
30	17.8	17.1	15.8	15.0	14.0
20	29.8	28.0	25.9	24.5	22.6
10	66.7	63.7	59.3	55.4	51.2

7. Ordering Information

Orderable Device	Package Type	Pins	Packing	Package Qty
MAX7219ND24ATAE	DIP	24	Tube	15
MAX7219WS24ARAE	SOP-W	24	Tape & Reel	1500
MAX7219SS24ARCQ	SSOP	24	Tape & Reel	3000

8. Package Information

8.1 DIP24

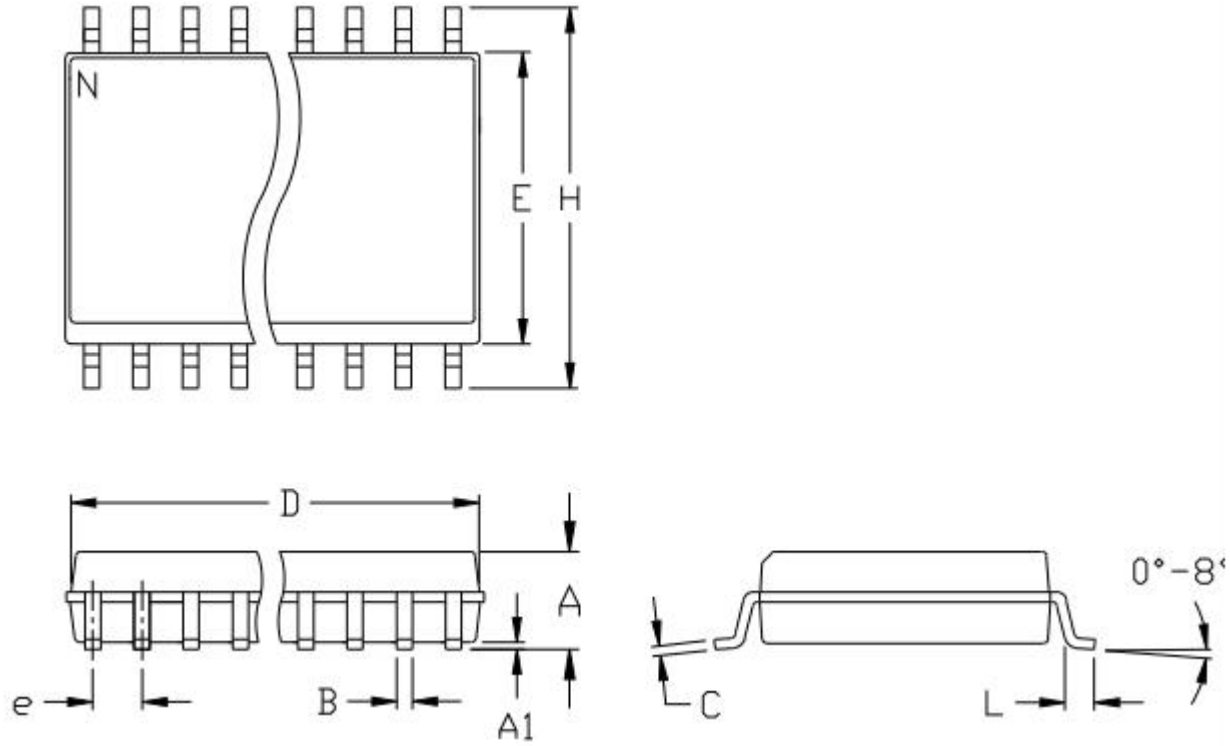


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

8.2 SOP24 - W

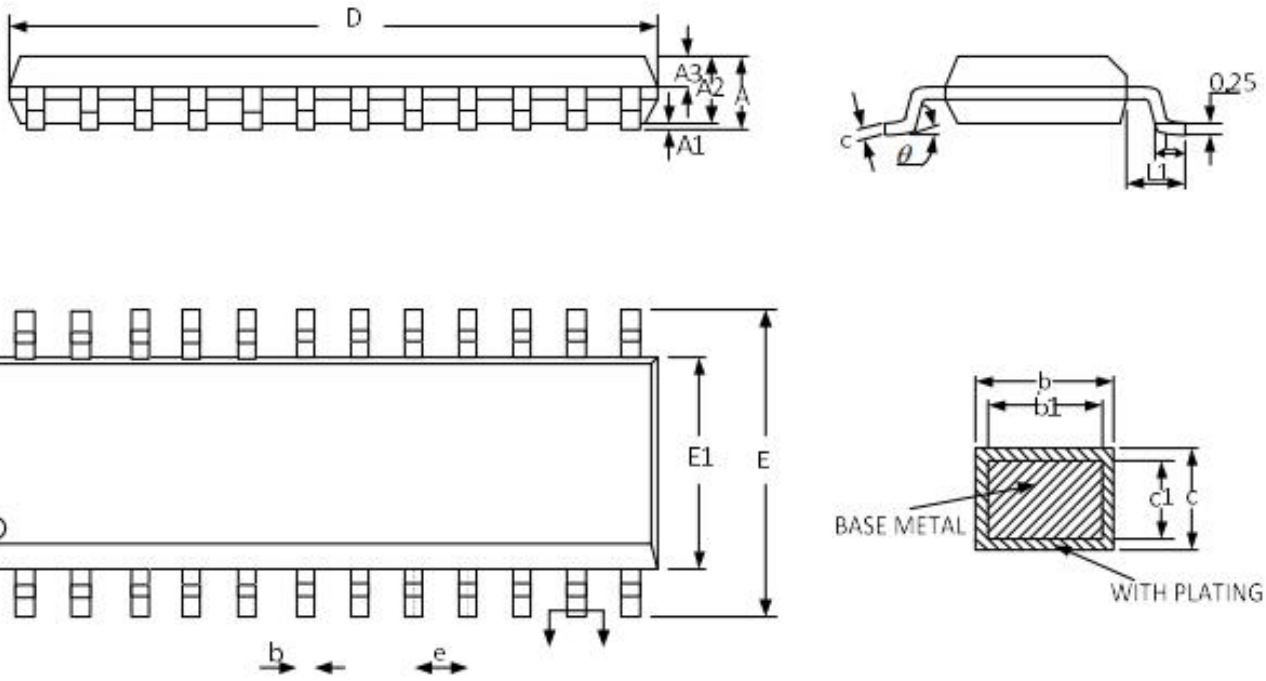


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
e	0.050		1.27	
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS013
D	0.398	0.413	10.10	10.50	16	AA
D	0.447	0.463	11.35	11.75	18	AB
D	0.496	0.512	12.60	13.00	20	AC
D	0.598	0.614	15.20	15.60	24	AD
D	0.697	0.713	17.70	18.10	28	AE

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS013-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

8.3 SSOP24



SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	-	-	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.23	-	0.33
b1	0.22	0.25	0.28
c	0.21	-	0.26
c1	0.19	0.20	0.21
D	8.45	8.65	8.85
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	0.635BSC		
L	0.50	0.65	0.80
L1	1.05BSC		
θ	0°	-	8°