

Dual N-channel Enhancement Mode Power MOSFET

Features

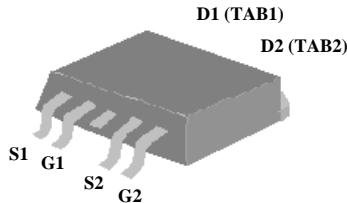
- $V_{DS} = 30V$, $I_D = 32A$
- $R_{DS(ON)} < 10 \text{ m}\Omega @ V_{GS} = 10V$
- $R_{DS(ON)} < 15 \text{ m}\Omega @ V_{GS} = 4.5V$

General Features

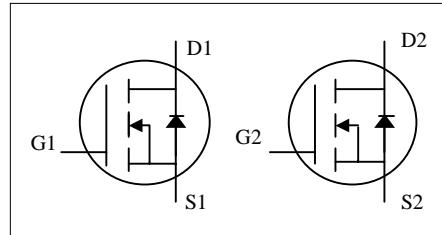
- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free and Green Available

100% UIS TESTED!

100% ΔV_{ds} TESTED!



TO252-4L



Schematic Diagram

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175^\circ\text{C}$)	I_D	32	A
		24	
		25.8 ^{b, c}	
		20 ^{b, c}	
Pulsed Drain Current	I_{DM}	100	
Avalanche Current Pulse	I_{AS}	39	
Single Pulse Avalanche Energy	E_{AS}	94.8	mJ
Continuous Source-Drain Diode Current	I_S	90 ^{a, e}	A
		3.13 ^{b, c}	
Maximum Power Dissipation	P_D	250 ^a	W
		175	
		3.75 ^{b, c}	
		2.63 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typ.	Max.	Unit
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	32	40	°C/W
Maximum Junction-to-Case	R_{thJC}	0.5	0.6	

SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

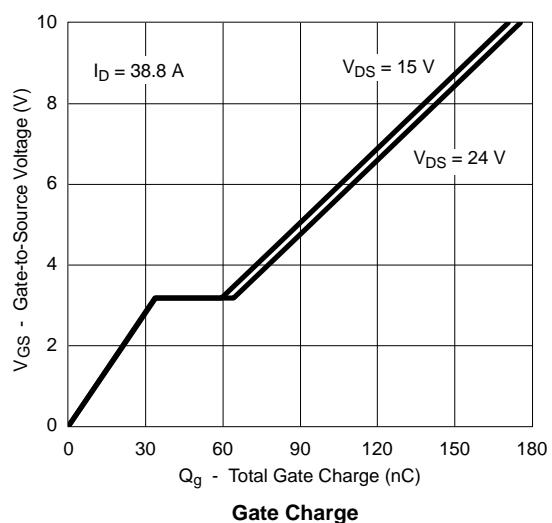
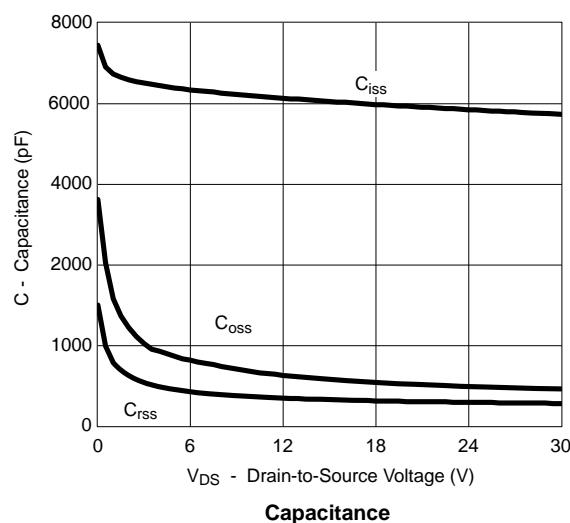
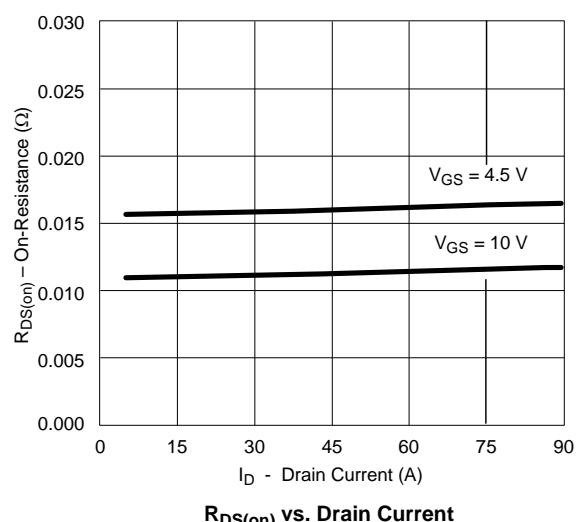
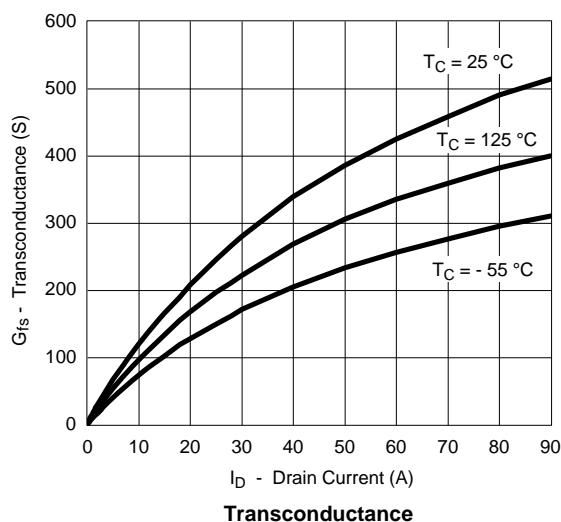
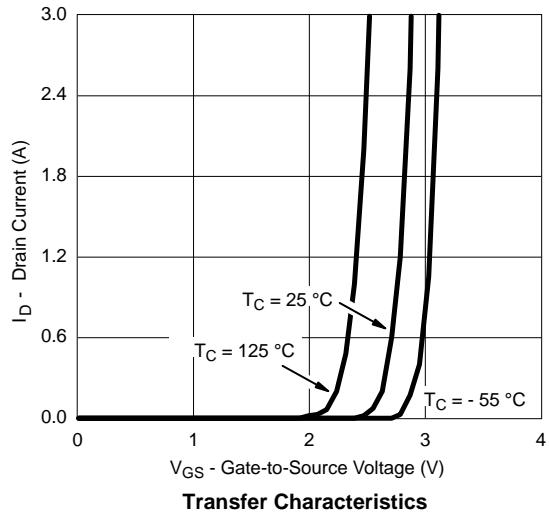
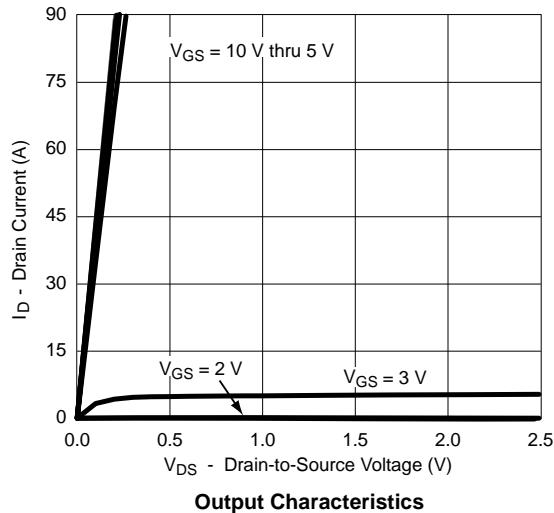
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$		35		mV/°C
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$			- 7.5		
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.0		2.5	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	90			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}, I_D = 38.8 \text{ A}$		0.010		Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 37 \text{ A}$		0.015		
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 38.8 \text{ A}$		160		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		1200		pF
Output Capacitance	C_{oss}			520		
Reverse Transfer Capacitance	C_{rss}			140		
Total Gate Charge	Q_g	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 38.8 \text{ A}$		171		nC
Gate-Source Charge	Q_{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 28.8 \text{ A}$		81		
Gate-Drain Charge	Q_{gd}			34		
Gate Resistance	R_g	$f = 1 \text{ MHz}$		29		
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 15 \text{ V}, R_L = 0.625 \Omega$ $I_D \geq 24 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		1.4	2.1	Ω
Rise Time	t_r			18	27	ns
Turn-Off Delay Time	$t_{d(\text{off})}$			11	17	
Fall Time	t_f			70	105	
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 15 \text{ V}, R_L = 0.67 \Omega$ $I_D \geq 22.5 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		10	15	ns
Rise Time	t_r			55	83	
Turn-Off Delay Time	$t_{d(\text{off})}$			180	270	
Fall Time	t_f			55	83	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			120	A
Pulse Diode Forward Current ^a	I_{SM}				120	
Body Diode Voltage	V_{SD}	$I_S = 22 \text{ A}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 20 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$		52	78	ns
Body Diode Reverse Recovery Charge	Q_{rr}			70.2	105	nC
Reverse Recovery Fall Time	t_a			27		ns
Reverse Recovery Rise Time	t_b			25		

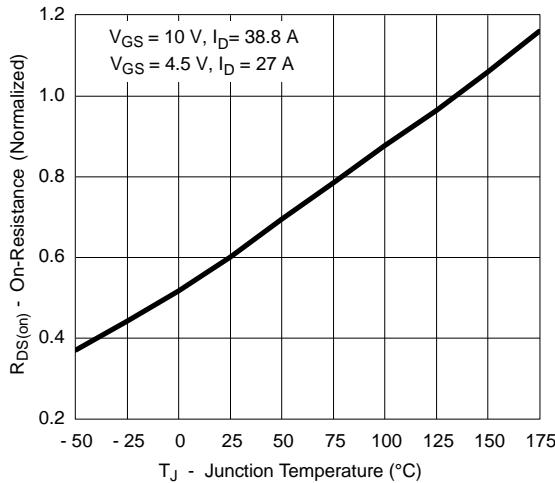
Notes:

a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

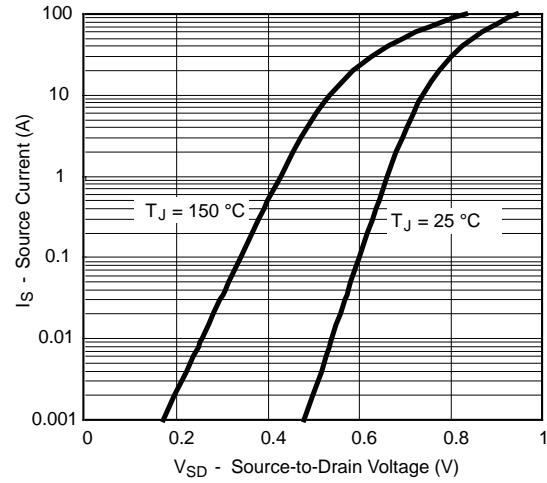
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

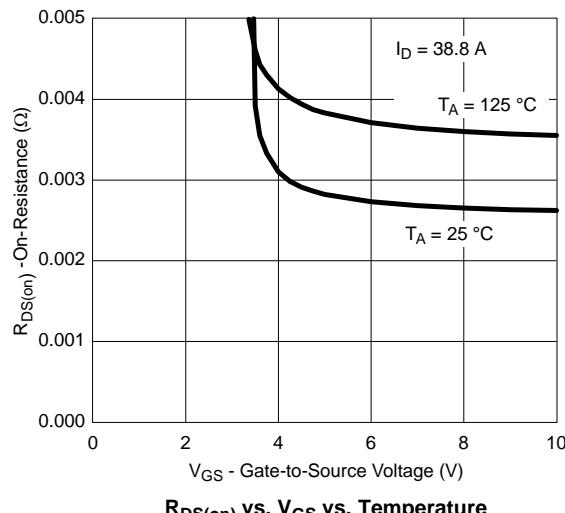
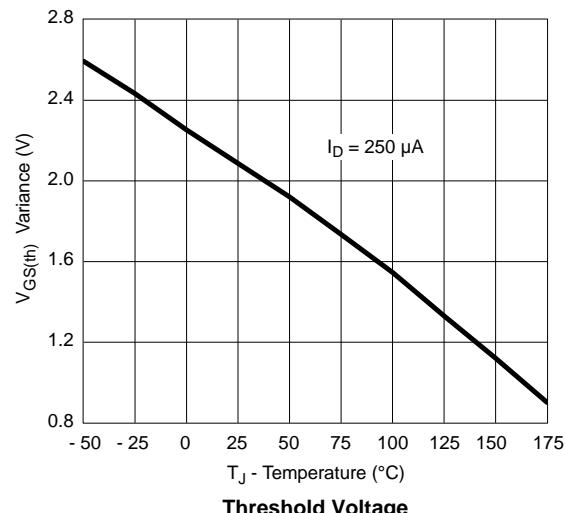
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

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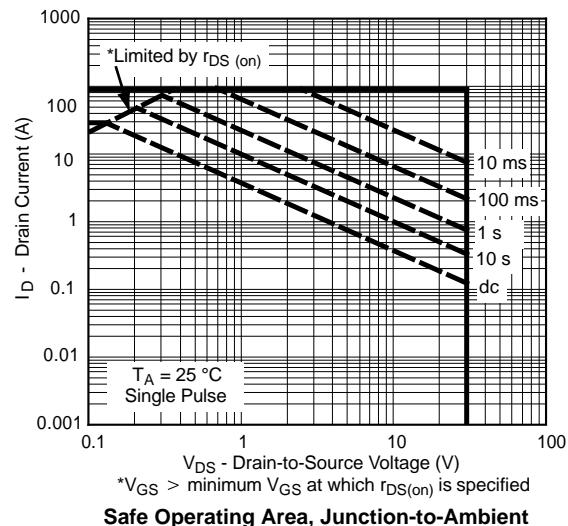
On-Resistance vs. Junction Temperature



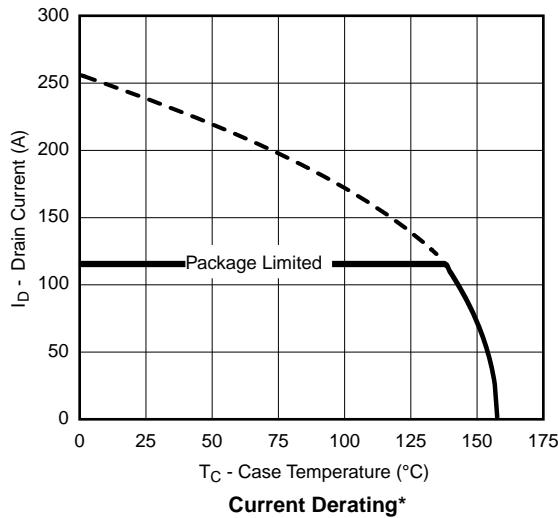
Forward Diode Voltage vs. Temperature

 $R_{DS(on)}$ vs. V_{GS} vs. Temperature

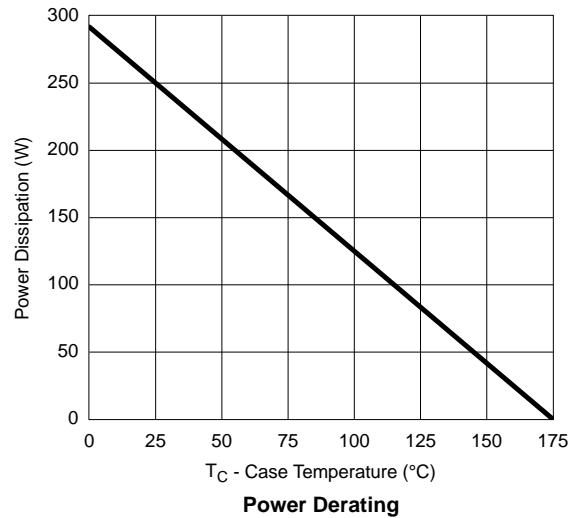
Threshold Voltage



Safe Operating Area, Junction-to-Ambient

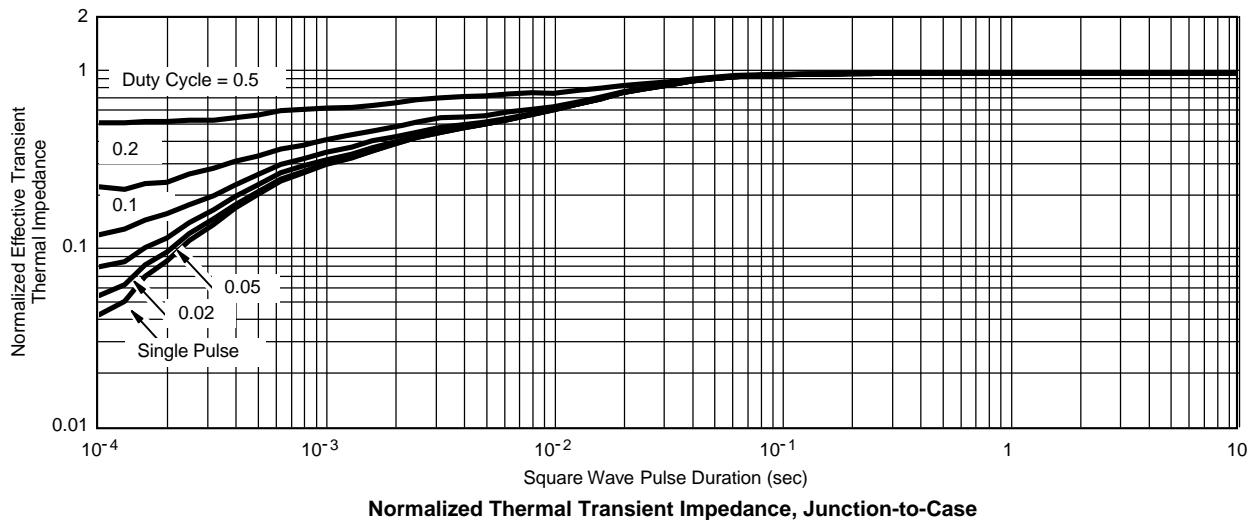
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


Current Derating*



Power Derating

*The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



Normalized Thermal Transient Impedance, Junction-to-Case