Features

- Dual bidirectional Translator for SDA and SCL Lines in I2C Applications and SMBus Compatible
- Support multi-mode: Standard-mode (SM), Fast-mode (FM), and Fast-mode Plus (FM+)
- Less than 1.5 ns (max) Delay to Accommodate SM and FM I2C devices and multiple masters
- Allows Voltage-Level Translation Between
  - 3.3V V_{REF1} and 5V V_{REF2}
  - 2.5V V_{REF1} and 3.3V or 5 V V_{REF2}
  - 1.8V V_{REF1} and 2.5V, 3.3V, or 5V V_{REF2}
  - 1.2V V_{REF1} and 1.8V, 2.5V, 3.3V, or 5V V_{REF2}
- Provides bidirectional voltage translation with no direction pin
- High-impedance SCL1, SDA1, SCL2 and SDA2 pins for EN = LOW
- Latch-Up performance exceeds 400 mA per JESD 78
- ESD Protection Exceeds JESD 22
  - 4000-V Human-Body Model
  - 1000-V Charged-Device Model

Description

The TPT29306 device is a dual bidirectional I2C and SMBus voltage-level translator with an enable (EN) input, and work from 1.2V to 3.6V V_{REF1} and 1.8V to 5.5V V_{REF2}.

The 3.5Ω R_{on} make the minimal propagation delay <1.5ns. If EN is high, the translator switch is ON, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, will allow bidirectional data flow between ports. If EN is low, the translator switch is off, and a high-impedance state exists between ports to isolate both sides.

The TPT29306 can also be used to run two buses, one is 400 kHz and the other is 100 kHz. If the two buses are operating at different frequency, the 100 kHz bus must be isolated when the other 400 kHz bus is required. If the master is running at 400 kHz, the maximum system frequency may be less than 400 kHz because of the delays added by the translator.

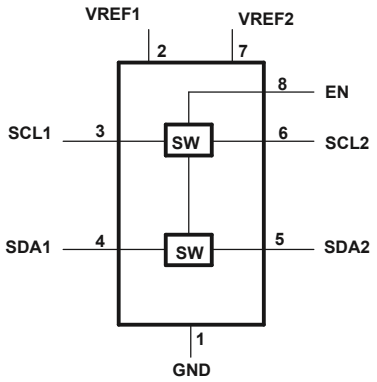
As with the standard I2C-bus system, pull-up resistors are required in both sides, to provide the logic HIGH levels on the translator's bus. The device is designed to work with SM, FM and FM+ I2C-bus devices in addition to SMBus devices. The maximum frequency is dependent on the RC time constant, but generally supports > 2 MHz.

TPT29306 is available in MSOP8, VSSOP8, DFN1.4X1-8L and DFN3X4-8L(none e-pad) package, and is characterized from –40°C to +85°C.

Applications

- I2C, SMBus, PMBus, MDIO, UART, Low-Speed SDIO, GPIO, and Other Two-Signal Interfaces
- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer handsets
- Industrial Automation

Function block

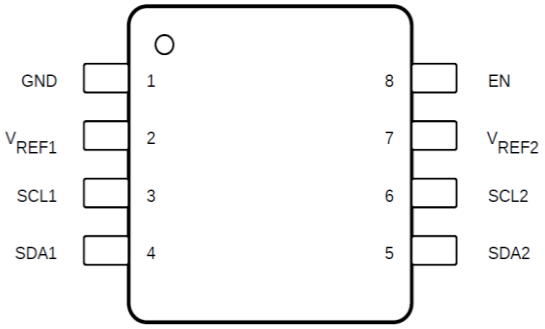


Revision History

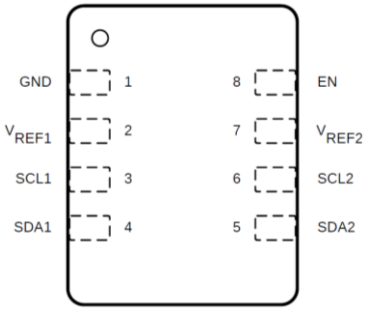
Date	Revision	Notes
2019/4/12	Rev. Pre 0.1	Initial Version
2019/9/7	Rev. Pre 0.2	Add DFN3X4-8L No e-pad package
2019/9/25	Rev. Pre 0.3	Add application notes
2019/12/23	Rev. Pre 0.4	Add ESD data
2020/4/20	Rev. Pre 0.5	Add test data
2020/10/26	Rev. Pre 0.6	Add VSSOP8 package information
2021/5/6	Rev. A.0	Release version
2021/12/9	Rev. B	Update the order information
2022/2/9	Rev. B.1	Update the tape and reel information
2022/5/8	Rev. B.2	Update the MSL of TPT29306L1-DFER from MSL3 to MSL1

Pin Configuration and Functions

TPT29306-VS1R
(MSOP8, 3.0 x 3.0 x 0.9 mm)
TPT29306L1-VS3R
(VSSOP8, 2.0 x 2.3 x 1.0 mm)



TPT29306L1-DFGR
(DFN1.4X1-8L)
TPT29306L1-DFER
(DFN3X4-8L)



Pin Functions

Pin name	Pin No	I/O	Description
GND	1	—	Ground, 0 V
V_{REF1}	2	I	Low-voltage-side reference supply voltage for SCL1 and SDA1
SCL1	3	I/O	Serial clock, low-voltage side
SDA1	4	I/O	Serial data, low-voltage side
SDA2	5	I/O	Serial data, high-voltage side
SCL2	6	I/O	Serial clock, high-voltage side
V_{REF2}	7	I	High-voltage-side reference supply voltage for SCL2 and SDA2, connect to power supply through external 200kΩ pull up resistor
EN	8	I	Switch enable input, directly connect to V_{REF2}

Absolute Maximum Ratings (1)

Parameter		MIN	MAX	UNIT
V_{REF1}	DC reference voltage range	–0.5	7	V
V_{REF2}	DC reference bias voltage range	–0.5	7	V
V_I	Input voltage range(2)	–0.5	7	V
$V_{I/O}$	Input/output voltage range(2)	–0.5	7	V
	Continuous channel current		128	mA
I_{IK}	Input clamp current $V_I < 0$		–50	mA
$T_{j(max)}$	Maximum junction temperature		125	°C
T_{stg}	Storage temperature range	–65	150	°C

* Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(1) This data was taken with the JEDEC low effective thermal conductivity test board.
(2) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	1	kV

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
MSOP8	205	45	°C/W
VSSOP8	210	82	°C/W
DFN1.4X1.0-8L	261	152	°C/W
DFN3X4-8L	71	29	°C/W

Recommended Operating Conditions

Symbol	Description	MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage SCL1, SDA1, SCL2, SDA2	0	5.5	V
V_{REF1} (1)	Reference voltage	0	5.5	V
V_{REF2} (1)	Reference voltage	0	5.5	V
EN	Enable input voltage	0	5.5	V
I_{PASS}	Pass switch current		64	mA
T_A	Operating ambient temperature	–40	85	°C

(1) To support translation, V_{REF1} suggest to be 0.6V lower than V_{REF2}. Please see the Application information as reference.

Electrical Characteristics

All test condition is VDD = 3.3V, TA = +25°C, RL = 150Ω to GND

Symbol	Description	Test Conditions		Min	Typ	Max	Unit
V_{IK}	Input clamp voltage [note1]	I_I = –18 mA, EN = 0 V				–1.2	V
I_{IH}	Input leakage current	V_I = 5 V, EN = 0 V				5	μA
$C_{i(EN)}$	Input capacitance	V_I = 3 V or 0			11		pF
$C_{io(off)}$	Off capacitance, SCLn, SDAn	V_O = 3 V or 0, EN = 0 V			4	6	pF
$C_{io(on)}$	On capacitance, SCLn, SDAn	V_O = 3 V or 0, EN = 3 V			10.5	12.5	pF
R_{ON}	On-state resistance, SCLn, SDAn	V_I = 0 I_O = 64 mA	EN = 4.5 V		3.5	5.5	Ω
			EN = 3 V		4.7	7	
			EN = 2.3 V		6.3	9.5	
		V_I = 0 I_O = 15 mA	EN = 1.5 V		25.5	32	
		V_I = 2.4 V(3) I_O = 15 mA	EN = 4.5 V	1	6	15	
			EN = 3 V	20	60	140	
		V_I = 1.7 V(3) I_O = 15 mA	EN = 2.3 V	20	60	140	

Note1: symbol '-' means direction, sink current 18mA, input voltage 1.2V, typical value: input voltage 0.8V

Switching Characteristics AC Performance, TA = +25°C (Translating Down) (Fig. 1)

AC Electrical Specifications, Translating Down, EN = 3.3 V, VIH = 3.3 V; VIL = 0 V; VM = 1.15 V									
Parameter	**From (Input)**	**To (Output)**	**C_L = 50 pF**		**C_L = 30 pF**		**C_L = 15 pF**		**Unit**
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{PLH}	SCL2 or SDA2	SCL1 or SDA1	0	0.8	0	0.6	0	0.3	ns
t_{PHL}			0	1.2	0	1	0	0.5	

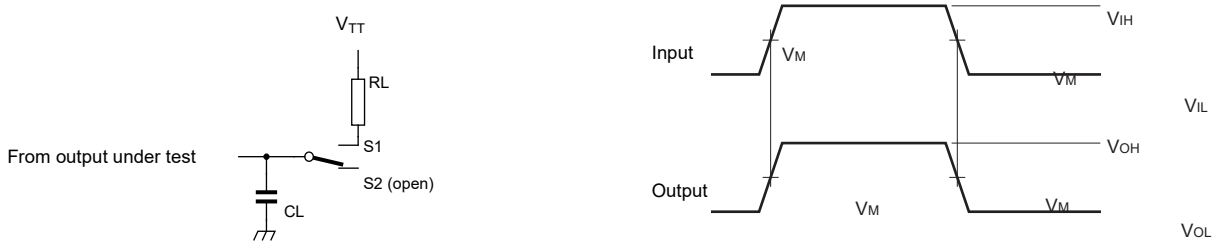
AC Electrical Specifications, Translating Down, EN = 2.5 V, VIH = 2.5 V; VIL = 0 V; VM = 0.75 V									
Parameter	**From (Input)**	**To (Output)**	**C_L = 50 pF**		**C_L = 30 pF**		**C_L = 15 pF**		**Unit**
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{PLH}	SCL2 or SDA2	SCL1 or SDA1	0	0.8	0	0.6	0	0.3	ns
t_{PHL}			0	1.2	0	1	0	0.5	

Switching Characteristics AC Performance, TA = +25°C (Translating Up) (Fig. 6)

AC Electrical Specifications, Translating Up, EN = 3.3 V, VIH = 2.3 V; VIL = 0 V; VTT = 3.3 V; VM = 1.15 V; RL = 300									
Parameter	**From (Input)**	**To (Output)**	**C_L = 50 pF**		**C_L = 30 pF**		**C_L = 15 pF**		**UNIT**
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{PLH}	SCL2 or SDA2	SCL1 or SDA1	0	0.9	0	0.6	0	0.4	ns
t_{PHL}			0	1.4	0	1.1	0	0.7	

AC Electrical Specifications, Translating Up, EN = 2.5 V, VIH = 1.5 V; VIL = 0 V; VTT = 2.5 V; VM = 0.75 V; RL = 300									
Parameter	**From (Input)**	**To (Output)**	**C_L = 50 pF**		**C_L = 30 pF**		**C_L = 15 pF**		**UNIT**
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{PLH}	SCL2 or SDA2	SCL1 or SDA1	0	0.9	0	0.6	0	0.4	ns
t_{PHL}			0	1.4	0	1.1	0	0.7	

Typical Performance Characteristics-TPT29306



a. Load circuit

b. Timing diagram

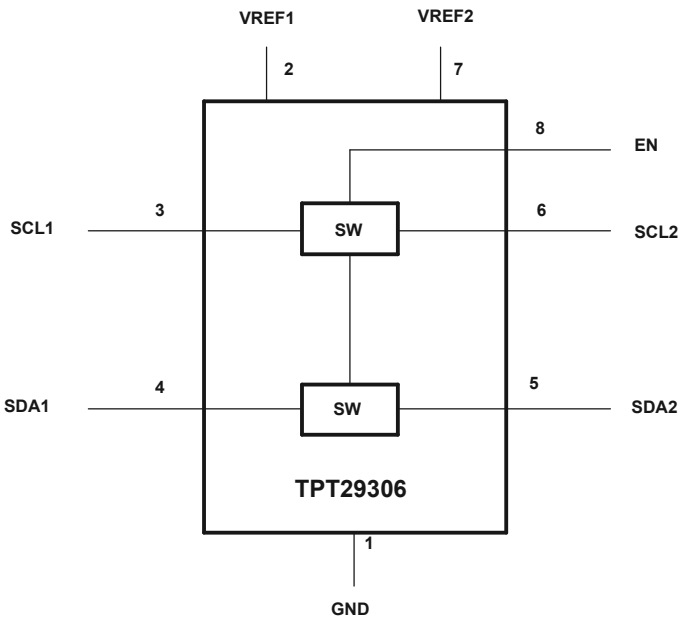
S1 = translating up; S2 = translating down.

C_L includes probe and jig capacitance.

The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load circuit for outputs

Function Block Diagram



Theory of Operation

The TPT29306 device is a dual bidirectional I2C and SMBus voltage-level translator with an enable (EN) input and operates without use of a direction pin. The voltage supply range for V_{REF1} is 1.0 V to 3.6 V and the supply range for V_{REF2} is 1.65 V to 5.5 V.

The TPT29306 device can also be used to run two buses, one at 400 kHz frequency and the other at 100 kHz frequency. If the two buses are operating at different frequencies, the 100 kHz bus must be isolated by using the EN pin when the 400 kHz operation of the main bus is required. If the master is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the level translator.

In I2C applications, the bus capacitance limit of 400 pF decides the number of devices and bus length. The capacitive load on both sides of the TPT29306 device must be calculated together, including the total load of the system, then make sure the sum of both sides is under 400 pF.

Both the SDA and SCL channels of the TPT29306 device have the same electrical characteristics, and there is minimal deviation from one output to another in voltage or propagation delay. Compared to the discrete transistor voltage-translation solutions, TPT29306 is a good benefit because of the symmetric design and accurate manufacture. The level shifter provides excellent ESD protection to lower-voltage devices and also protects low-level ESD devices.

Enable (EN) Pin

The TPT29306 device is an open-drain circuit in which the gate of the transistors is controlled by the voltage on the EN pin. In Figure 2 the TPT29306 device is always enabled when power is applied to V_{REF2}. In Figure 3, the device is enabled when a control signal from a processor is in a logic-high state.

Voltage Translation

The primary feature of the TPT29306 device is translating voltage from an I2C bus V_{REF1} to I2C bus V_{REF2}. Side-1 is referenced to V_{REF1} up to an I2C bus referenced to V_{DPU}(VCC1), and side-2 V_{REF2} is connected through a 200 kΩ pullup resistor. Translation on a standard, open-drain I2C bus is achieved by simply connecting pullup resistors from SCL1 and SDA1 to V_{REF1}, and connecting pullup resistors from SCL2 and SDA2 to VCC2.

Device Function table

Input EN(1)	Translator Function
H	SCL1 = SCL2, SDA1 = SDA2
L	Disconnect

(1) The SCL switch conducts if EN is ≥ 1 V higher than SCL1 or SCL2. The same is true of SDA.

Application information

General Applications of I2C

As with the standard I2C system, pullup resistors are required to provide the logic-high levels on the translator bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with standard-mode and fast-mode I2C devices, in addition to SMBus devices. Standard-mode I2C devices only specify 3 mA in a generic I2C system where standard-mode devices and multiple masters are possible. Under certain conditions, high termination currents can be used. When the SDA1 or SDA2 port is low, the clamp is in the ON state, and a low-resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is high, the voltage on the SDA1 port is limited to the voltage set by V_{REF1}. When the SDA1 port is high, the SDA2 port is pulled to the pullup supply voltage of the drain by the pullup resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control. The SCL1-SCL2 channel also functions in the same way as the SDA1-SDA2 channel.

Typical Application

Figure 2 and Figure 3 show how these pullup resistors are connected in a typical application, as well as two options for connecting the EN pin.

Power Supply Requirements

For supplying power to the TPT29306 device, the V_{REF1} pin can be connected directly to a power supply. The V_{REF2} pin **MUST** be connected to the VCC2 power supply through a 200 kΩ resistor. Failure to have a high impedance resistor between V_{REF2} and V_{DPU} results in excessive current draw and unreliable device operation. It is also worth noting, that in order to support voltage translation, the TPT29306 **MUST** have the EN and VREF2 pins shorted and then pulled up to VCC2 through a high-impedance resistor (200 kΩ).

Bidirectional Voltage Translation

For the bidirectional clamping configuration, could be higher voltage to lower voltage or lower voltage to higher voltage, the EN input must be connected to V_{REF2} and both pins pulled to high-side power supplier through a pullup resistor (typically 200 kΩ as recommend above). This allows V_{REF2} to regulate the EN input and a 100 pF filter capacitor connected to V_{REF2} is recommended. The I2C bus master output can be push-pull, if it is open-drain output then it should connect to pullup resistors. However, if either output is push-pull, data(SDA) must be unidirectional or the outputs must be 3-state capable and be controlled by some direction-control circuit to prevent high-to-low competition in either direction. If both outputs are open-drain, no direction control is needed.

The reference supply voltage (V_{REF1}) is connected to the core power-supply voltage of the I2C master, and V_{REF2} is connect to the I2C slave through 200 kΩ pullup resistor.

Design Requirements

		Min	Typ(1)	Max	UNIT
V_{REF2}	Reference voltage	V_{REF1} + 0.6	2.1	5	V
EN	Enable input voltage	V_{REF1} + 0.6	2.1	5	V
V_{REF1}	Reference voltage	1.2	1.5	4.4	V

I_{PASS}	Pass switch current	6	mA
I_{REF}	Reference-transistor current	5	μA

(1) All typical values are at T_A = 25°C.

Typical Application Circuit

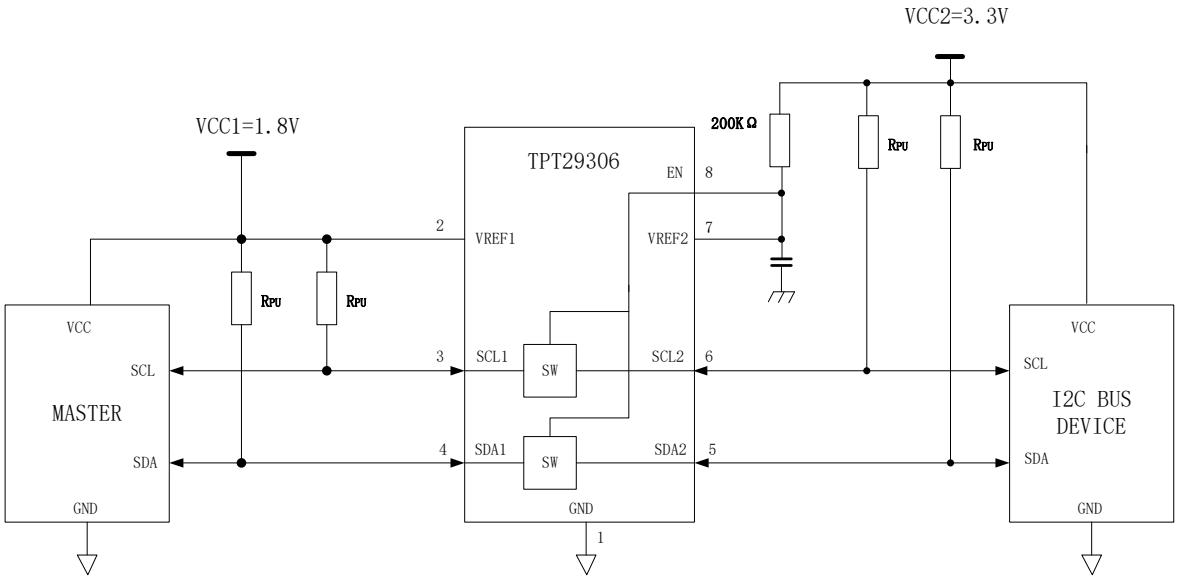


Figure 2. Typical application circuit, switch always Enable

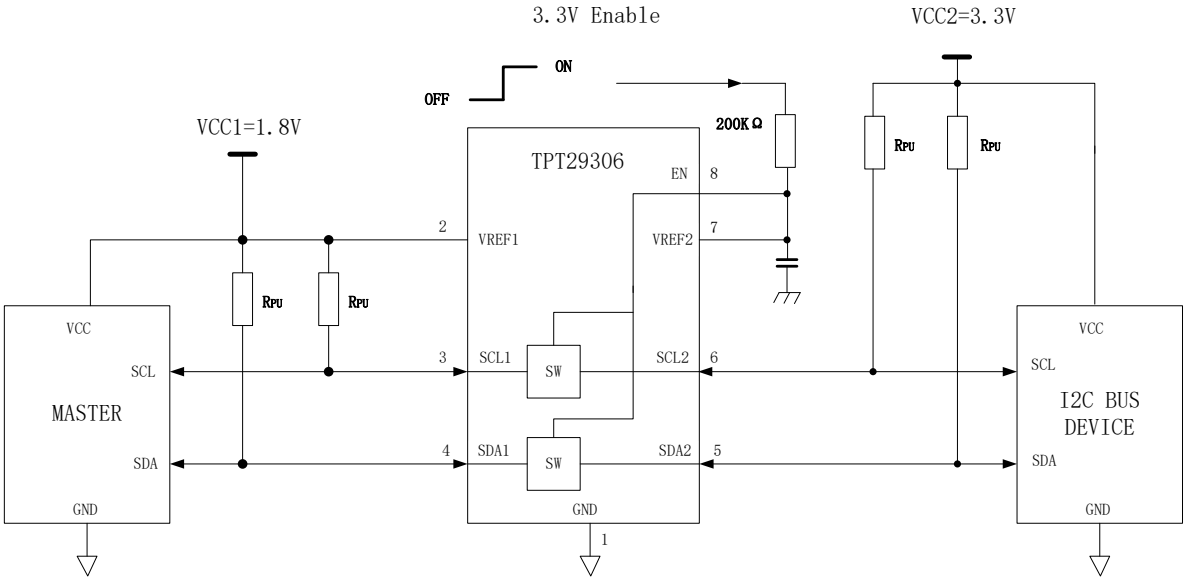


Figure 3. Typical application circuit, switch Enable control by I/O input

Pullup Resistors

To get an estimate for the range of values that can be used for the pullup resistor, please refer to Figure 4 and Figure 5, which shows the maximum and minimum pullup resistance allowable by the I2C specification for standard-mode (100 kHz) and fast-mode (400 kHz) operation.

No pullup resistor is needed on the host side (3.3 V) if the TPT29306 device is being driven by standard CMOS push-pull output driver.

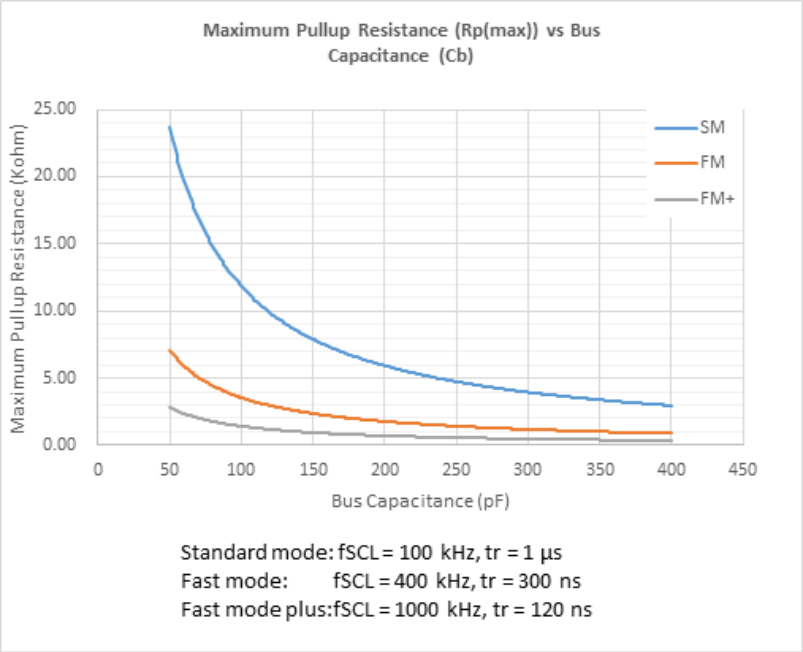


Figure 4. Maximum Pullup Resistance ($R_{pu(max)}$) vs Bus Capacitance (C_b)

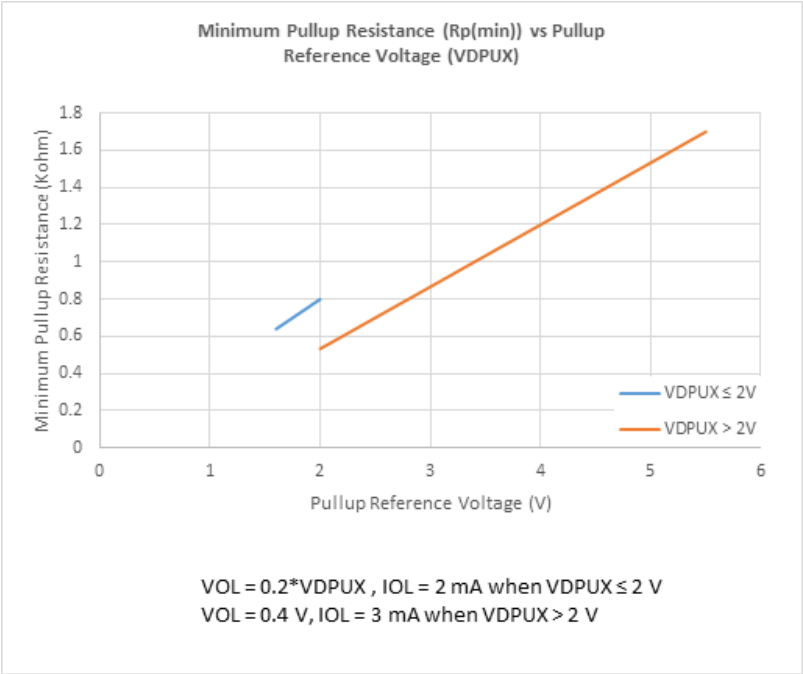


Figure 5. Minimum Pullup Resistance ($R_{pu(min)}$ as VCC1) vs Pullup Reference Voltage (V_{DPUX} as VCC2)

Bandwidth

The maximum frequency of the TPT29306 device depends on the application. The device can operate at speeds of > 100 MHz given the correct conditions. The maximum frequency is dependent upon the loading of the application. The TPT29306 device acts as a standard switch, and the bandwidth of the device is decided by the on-resistance and on-capacitance of the device.

Figure 6 shows a bandwidth measurement of the TPT29306 device using a two-port network analyzer.

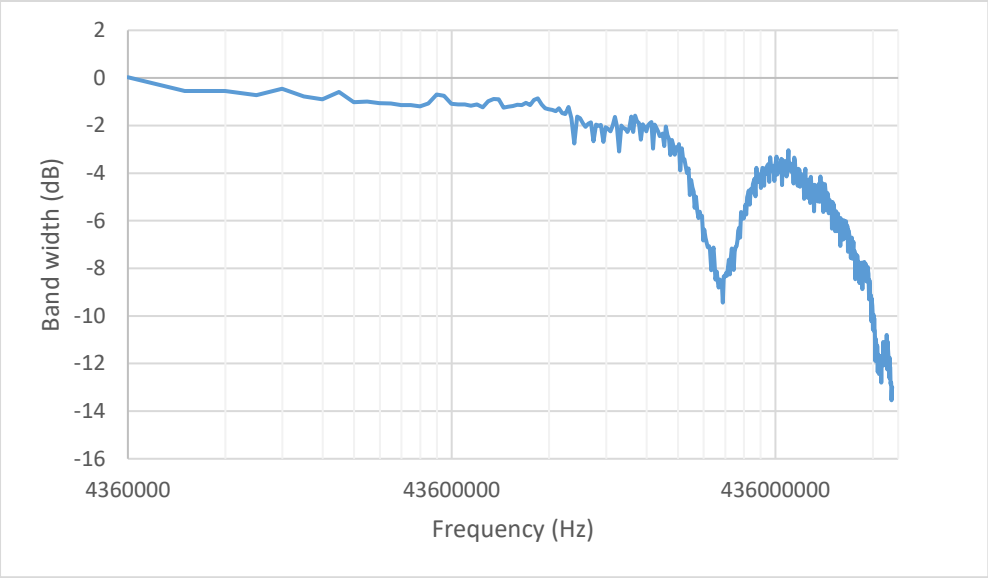


Figure 6. Typical bandwidth reference

You can then use a simple formula to calculate the maximum frequency component (F0).

F0= 0.5 / RT (10%–90%)

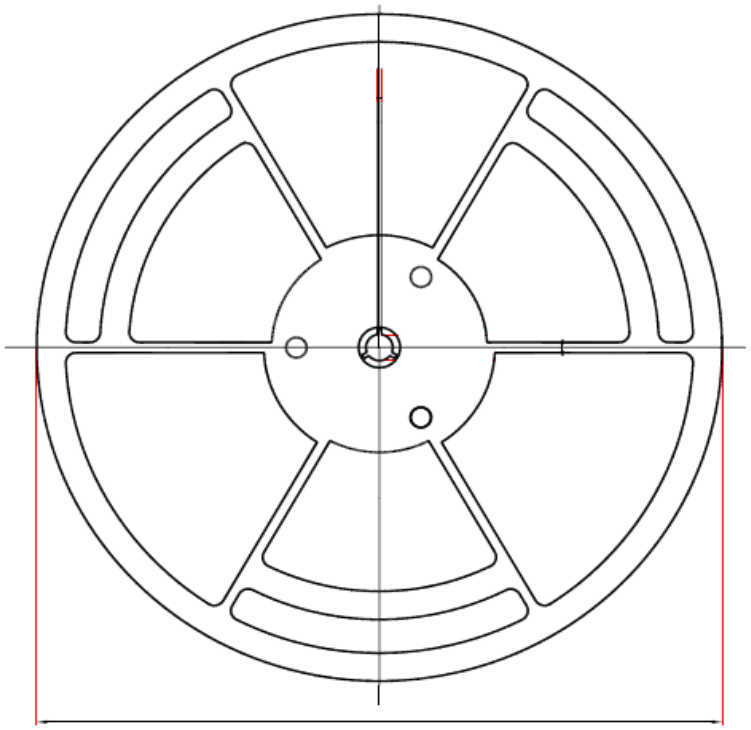
F0 = 0.4 / RT (20%–80%)

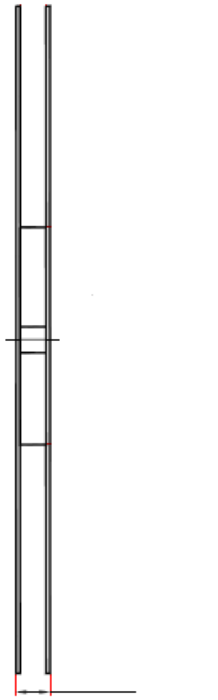
For signals with rise-time characteristics based on 10% to 90% thresholds, F0 is equal to 0.5 divided by the rise time of the signal. For signals with rise-time characteristics based on 20% to 80% thresholds, which is very common in many current device specifications, F0 is equal to 0.4 divided by the rise time of the signal. The digital clock frequency of >100 MHz can be achieved.

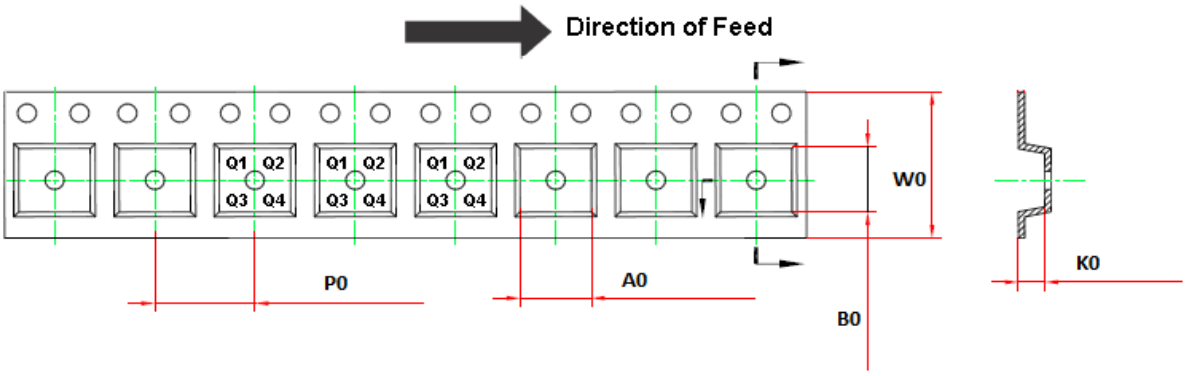
Some guidelines to follow that help maximize the performance of the device:

- Keep trace length to a minimum by placing the TPT29306 device close to the I^2C output of the master.
- The trace length should be less than half the time of flight to reduce ringing and line reflections or nonmonotonic behavior in the switching region.
- To reduce overshoots, a pullup resistor can be added on the VREF1 side, then it will result a slower fall time.

Tape and Reel Information



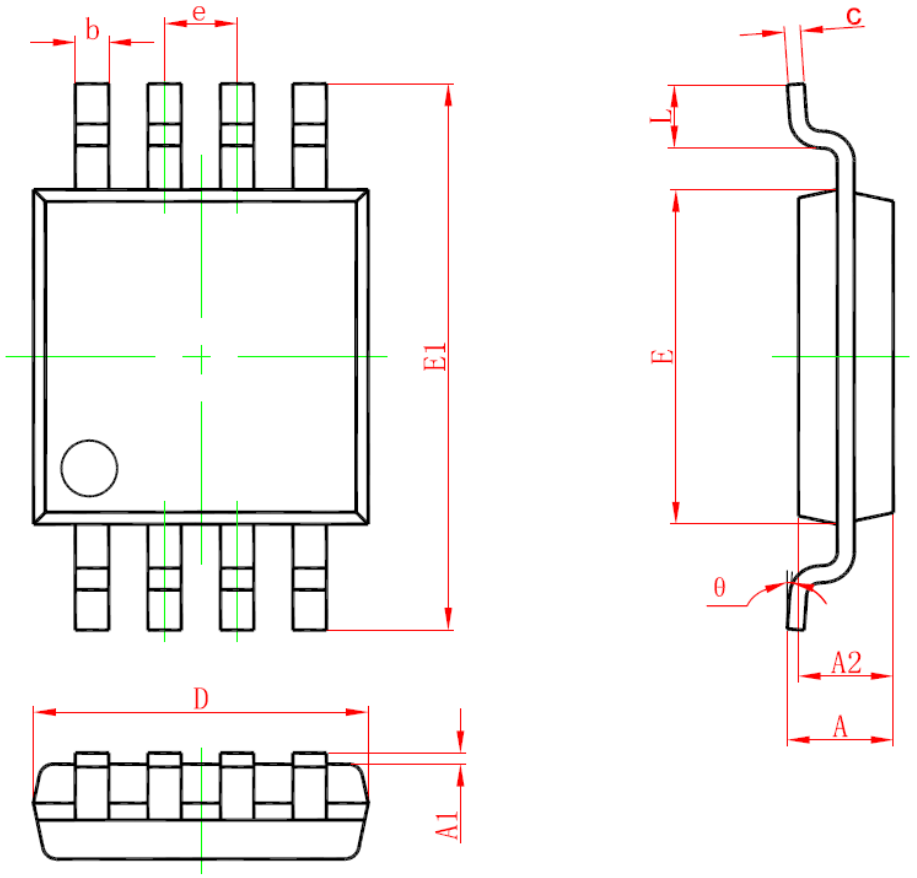




Order Number	Package	D1	W1	A0	B0	K0	P0	W0	Pin1 Quadrant
TPT29306-VS1R	8-Pin MSOP	330.0	17.6	5.2	3.3	1.5	8.0	12.0	Q1
TPT29306L1-VS3R	8-Pin VSSOP	178.0	15	2.25	3.35	1.4	4.0	8.0	Q3
TPT29306L1-DFGR	DFN1.4X1.0-8L	180	13.1	1.6	2	0.85	4	8	Q1
TPT29306L1-DFER	DFN3X4-8L	330	12.8	3.3	4.3	1	8	12	Q2

Package Outline Dimensions

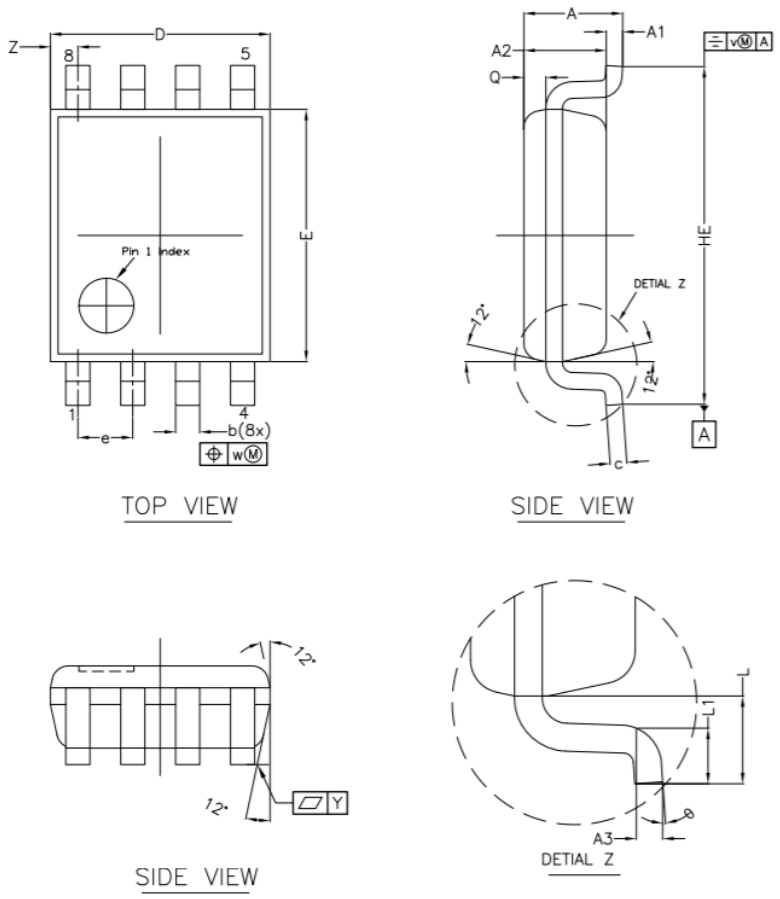
VS1R (MSOP8)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650(BSC)		0.026(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

Package Outline Dimensions

VS3R (VSSOP8)

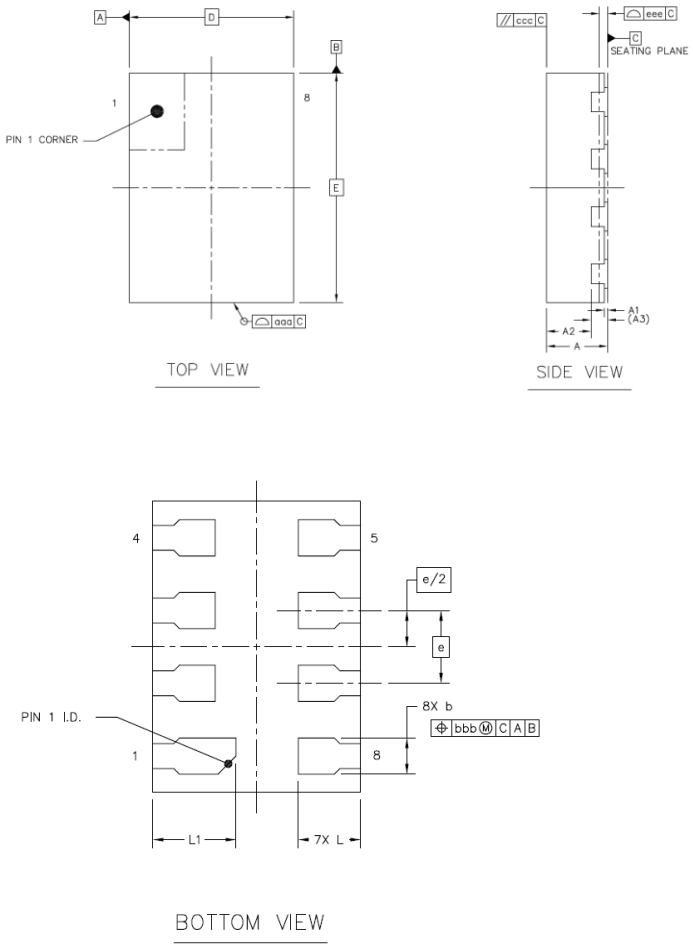


* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	1.00
A1	0.00	---	0.15
A2	0.60	0.75	0.85
A3	---	0.12	---
Q	0.19	0.20	0.21
b	0.17	0.22	0.27
c	0.08	---	0.23
D	1.90	2.00	2.10
E	2.20	2.30	2.40
HE	3.00	3.10	3.20
e	0.50 bsc		
L	0.40 bsc		
L1	0.15	---	0.40
Y	---	0.10	---
v	---	0.20	---
w	---	0.08	---
Z	0.10	---	0.40
θ	0°	---	8°

Package Outline Dimensions

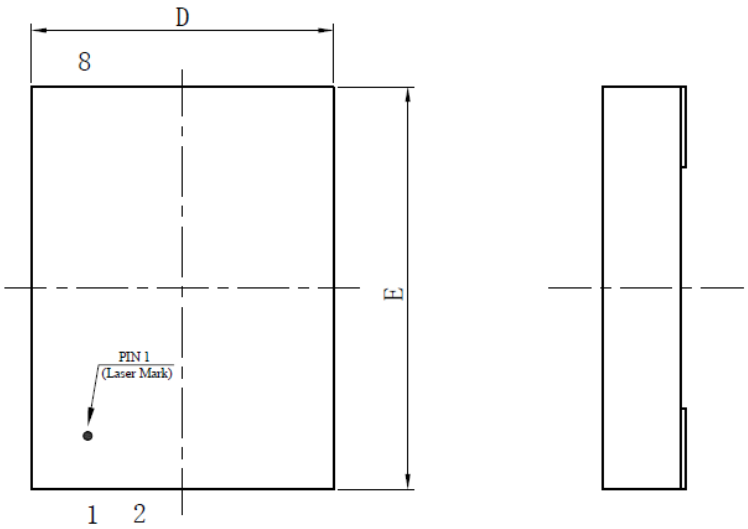
DFGR (DFN1.4X1.0-8L)



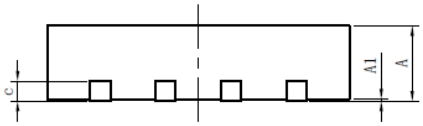
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.32	0.37	0.4
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.27	---
L/F THICKNESS		A3	0.102 REF		
LEAD WIDTH		b	0.125	0.175	0.225
BODY SIZE	X	D	1 BSC		
	Y	E	1.4 BSC		
LEAD PITCH		e	0.35 BSC		
LEAD LENGTH		L	0.25	0.3	0.35
		L1	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.05		
LEAD OFFSET		bbb	0.07		

Package Outline Dimensions

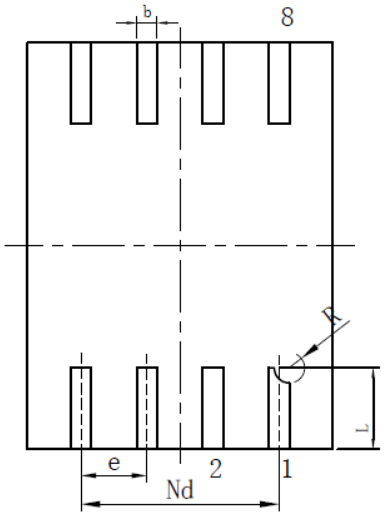
DFER (DFN3X4-8L, no e-pad)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	0	0.02	0. 05
b	0. 15	0. 20	0. 25
c	0. 20REF		
D	2. 90	3. 00	3. 10
e	0. 65BSC		
Nd	1. 95BSC		
E	3. 90	4. 00	4. 10
L	0. 75	0.80	0. 85
R	0. 10	0.15	0. 20

**特殊设计：基岛不外露.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT29306-VS1R	-40 to 85°C	8-Pin MSOP	9306	MSL3	Tape and Reel, 3000	Green
TPT29306L1-VS3R	-40 to 85°C	8-Pin VSSOP8	9306	MSL1	Tape and Reel, 3000	Green
TPT29306L1-DFGR	-40 to 85°C	8-Pin DFN1.4X1.0	T26	MSL1	Tape and Reel, 4000	Green
TPT29306L1-DFER	-40 to 85°C	8-Pin DFN3X4 No e-pad	9306	MSL1	Tape and Reel, 3000	Green

(1). Future product, contact 3PEAK factory for more information and sample

(2). Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

3PEAK CONFIDENTIAL

IMPORTANT NOTICE AND DISCLAIMER

Copyright© 3PEAK 2012-2023. All rights reserved.

Trademarks. Any of the 思瑞浦 or 3PEAK trade names, trademarks, graphic marks, and domain names contained in this document /material are the property of 3PEAK. You may NOT reproduce, modify, publish, transmit or distribute any Trademark without the prior written consent of 3PEAK.

Performance Information. Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

Disclaimer. 3PEAK provides technical and reliability data (including data sheets), design resources (including reference designs), application or other design recommendations, networking tools, security information and other resources "As Is". 3PEAK makes no warranty as to the absence of defects, and makes no warranties of any kind, express or implied, including without limitation, implied warranties as to merchantability, fitness for a particular purpose or non-infringement of any third-party's intellectual property rights. Unless otherwise specified in writing, products supplied by 3PEAK are not designed to be used in any life-threatening scenarios, including critical medical applications, automotive safety-critical systems, aviation, aerospace, or any situations where failure could result in bodily harm, loss of life, or significant property damage. 3PEAK disclaims all liability for any such unauthorized use.

3PEAK CONFIDENTIAL