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Product Specification

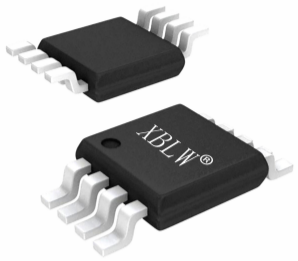
XBLW PCF8563T

1.2V I²C Real Time Clock/Calendar Chip

WEB | www.xinboleic.com

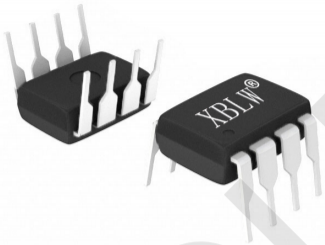
Descriptions

The PCF8563T is a low-power CMOS real-time clock/calendar chip that provides a programmable clock output, an interrupt output, and a power-down detector, all of which are serially transmitted via the I²C bus interface. The maximum bus speed is 400K bits/s, and the embedded word address register is automatically incremented each time data is read or written.



MSOP-8

SOP-8



DIP-8

Feature

- Featuring the symbol of the century
- Alarm and Timer
- Power outage detector
- Internally integrated oscillating capacitor
- Open drain interrupt pin
- Wide working voltage range: 1.2V~5.5V
- Low standby current: typical value is 0.22 μ A
- I²C bus slave address: read, 0A3H; Write, 0A2H
- The programmable clock output frequency is:
  --32.768kHz，1024Hz，32Hz，1Hz
- Timeable based on 32.768kHz crystal output:
  --Seconds, minutes, hours, weeks, days, months, years

Applications

- Mobile phone
- Portable instrument
- Fax machine
- Battery power products
- Television
- Payment rate electricity meter,IC card water meter,IC card gas meter

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW PCF8563T	SOP-8	PCF8563T	Tape	2500Pcs/Reel
XBLW PCF8563TS	MSOP-8	8563	Tape	3000Pcs/Reel
XBLW PCF8563P	DIP-8	PCF8563P	Tube	2000Pcs/Box

Typical application circuit diagram

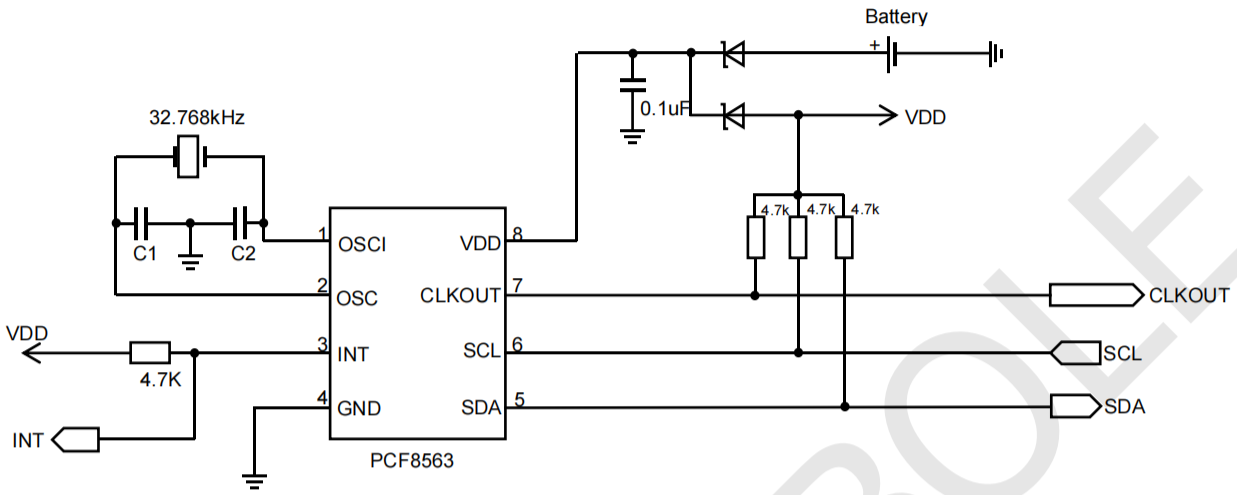


Fig 1.Typical application circuit diagram

Note: In typical application circuits, the load capacitors C1 and C2 of the crystal oscillator can be selected as capacitors of around 20pF, and the actual value of the capacitors can be fine tuned to obtain the best clock accuracy.

Block Diagram

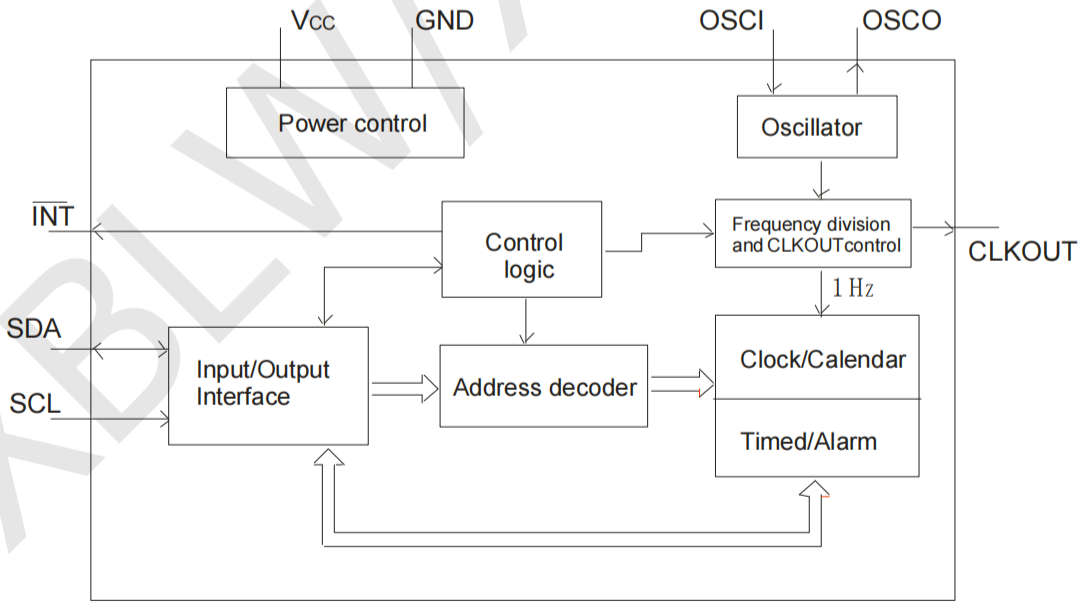
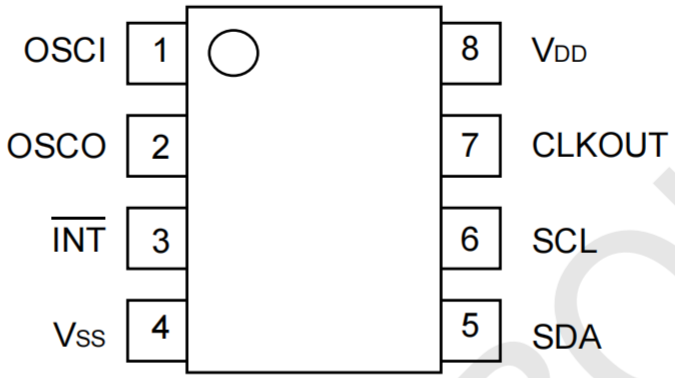


Fig 2. Block diagram

Pin Configurations

SOP-8/MSOP-8/DIP-8
(Top View)



Pin Description

NO.	Symbol	Description	NO.	Symbol	Description
1	OSCI	Oscillator Input	5	SDA	Serial Data I / O
2	OSCO	Oscillator Output	6	SCL	Serial Clock Input
3	$\overline{INT}$	Input Cut	7	CLKOUT	Clock Output
4	V_{SS}	Ground	8	V_{DD}	Power Supply

Extreme Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{DD}	-0.5	+6.5	V
Supply Current	I_{DD}	-50	+50	mA
DC Input Current For All Inputs	I_I	-10	+10	mA
DC Output Current For All Outputs	I_O	-10	+10	mA
Total Power Loss	P	-	300	mW
Operating Temperature	T_A	-40	+85	℃
Storage Temperature	T_S	-65	+150	℃
CLKOUT and $\overline{INT}$ Pin Output Voltage	V_O	-0.5	+6.5	V
SCL and SDA Pin Input Voltage	V_I	-0.5	+6.5	V
OSCI Pin Input Voltage		-0.5	V_{DD}+ 0.5	V

Electrical Characteristic Parameter

DC Characteristics

(Unless not specified, V_{DD} =1.2~5.5V, V_{SS} =0V; T_A =-40~+85°C; fosc =32.768kHz;quartz chip R_S=40kΩ , C_L =8pF)

Parameters	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power Supply						
Operating voltage	V_{DD}	I²C Bus valid, f = 400 kHz [1]	1.8	-	5.5	V
Operating voltage for reliable Clock/Calendar Data		T_A=25°C	1.2	-	5.5	V
Operating current 1 CLKOUT valid (FE=1)	I_{DD1}	f_{SCL}=400kHz	-	-	800	μA
		f_{SCL}=100kHz	-	-	200	μA
Operating current 2 CLKOUT disable(FE=0)	I_{DD2}	f_{SCL} = 0Hz, T_A = 25°C [2]				
		V_{DD}=3.0V	-	0.22	0.6	μA
		V_{DD}=2.0V	-	0.2	0.5	μA
Operating current 3 CLKOUT= 32.768kHz	I_{DD3}	f_{SCL} = 0Hz, T_A = 25°C [2]				
		V_{DD}=3.0V	-	0.7	1	uA
		V_{DD}=2.0V	-	0.6	0.9	uA
Low level input voltage	V_{IL}		V_{SS}	-	0.3V_{DD}	V
High level input voltage	V_{IH}		0.7V_{DD}	-	V_{DD}	V
Input leakage current	I_{LI}	VI =V_{DD} or V_{SS}	-1	0	+1	μA
Input capacitance	C_I	[3]	-	-	7	pF
Output						
SDA low level output current	I_{OLS}	V_{OL} = 0.4V, V_{DD} = 5.0V	-3	-	-	mA
INT Low level output current	I_{OLI}	V_{OL}=0.4V, V_{DD}=5.0V	-1	-	-	mA
CLKOUT low level output current	I_{OLC}	V_{OL}=0.4V, V_{DD}=5.0V	-1	-	-	mA
CLKOUT high level output current	I_{OHC}	V_{OL}=4.6V, V_{DD}=5.0V	1	-	-	mA
Output leakage current	I_{LO}	V_O=V_{DD} or V_{SS}	-1	0	+1	μA
Voltage Detector						
Power-down detection voltage	V_{LOW}	T_A = 25°C	-	1.0	-	V

1.Oscillator starts reliably on power-up: V_{DD} (min., on power-up) = V_{DD} (min.) + 0.3V

2.Timer source clock = 1/ 60Hz; SCL and SDA are both V_{DD}.

3.Testing on a sample basis

AC Characteristics

Unless specified, V_{DD}=1.2~ 5.5V, V_{SS}= 0V; T_A =-40 + 85°C; f_{OSC}=32.768kHz; quartz crystal Rs=40kΩ, C_L =8pF)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Oscillator						
Precision load capacitance	C_{INT}		15	25	35	pF
Oscillator stability	$\Delta f_{OSC}/f_{OSC}$	ΔV_{DD} =200mV,T_A=25°C	-	0.2	-	ppm
Quartz crystal parameters (f=32.768kHz)						
Series resistance	R_S		-	-	100	kΩ
Shunt load capacitance	C_L		7	-	12.5	pF
Trimmer capacitors	C_T		5	-	25	pF
CLKOUT Output						
CLKOUT Duty factor	δ_{CLKOUT}	[1]	-	50	-	%
I²C Bus Timer Characteristics[2]						
SCL clock period	f_{SCL}	[3]	-	-	400	kHz
Holding time for starting conditions	t_{HDSTA}		0.6	-	-	μs
Repeat start condition establishment time	t_{SUSTA}		0.6	-	-	μs
SCL low level time	t_{LOW}		1.3	-	-	μs
SCL high level time	t_{HIGH}		0.6	-	-	μs
Rising time of SCL and SDA	t_r		-	-	0.3	μs
Falling time of SCL and SDA	t_f		-	-	0.3	μs
Bus load capacitance	C_b		-	-	400	pF
Data setup time	t_{SUDAT}		100	-	-	ns
Data hold time	t_{HDDAT}		0	-	-	ns
Stop condition set up time	t_{SUSTO}		0.6	-	-	μs
Acceptable bus spike width	t_{SW}		-	-	50	ns

1.Unless special description f_{CLKOUT} = 32 .768kHz
2. All timing values are valid within the operating voltage range (under TA conditions), and the reference input voltage changes from V_{SS} to V_{DD} are the values of V_{IL} and V_{IH}.
3. The access time of the I²C bus must be less than 1s for two start and one stop conditions

I²C Bus Timing Waveforms

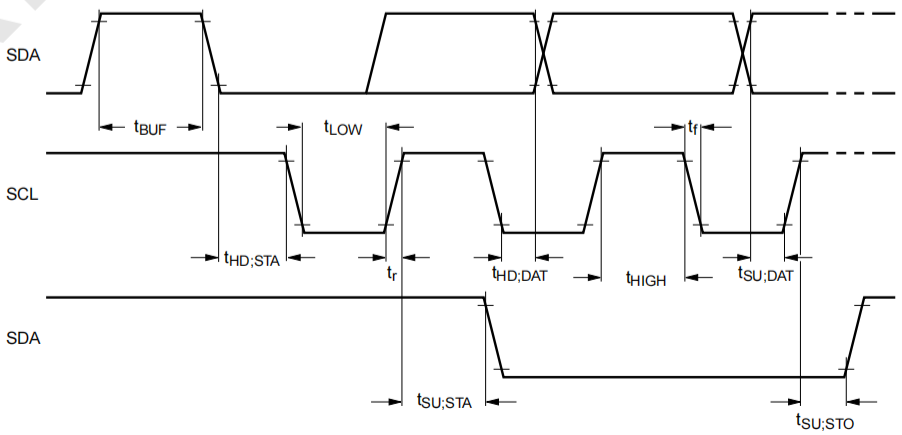
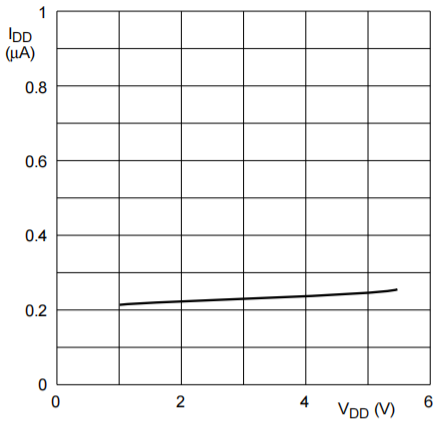
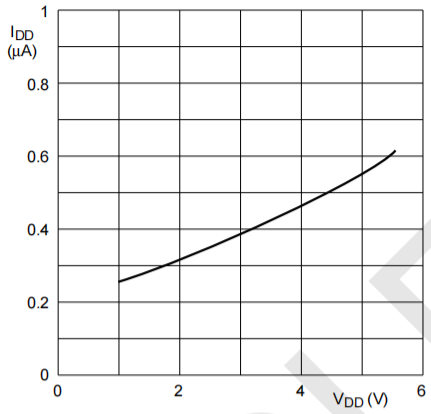


Fig 3 . I²C-bus timing waveforms



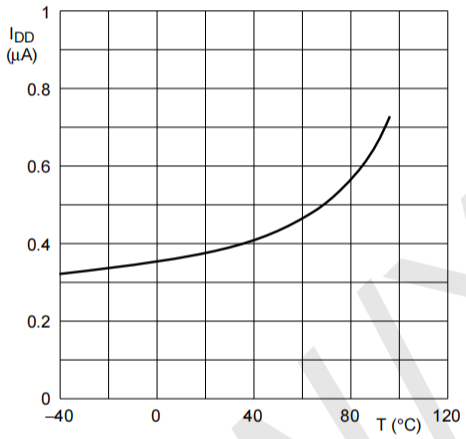
T_{amb} = 25 °C; Timer = 1 minute.

Fig 4 . Supply current I_{DD} as a function of supply voltage V_{DD}; CLKOUT disabled



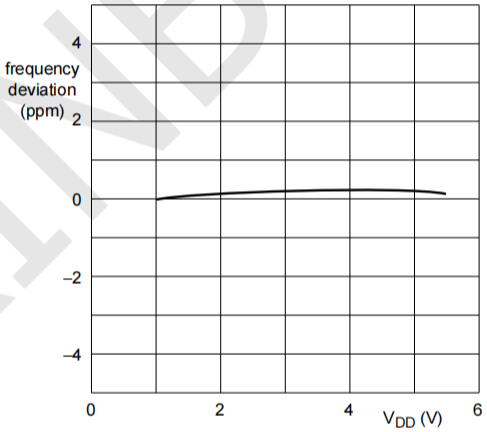
T_{amb} = 25 °C; Timer = 1 minute.

Fig 5 . Supply current I_{DD} as a function of supply voltage V_{DD}; CLKOUT = 32 kHz



V_{DD} = 3 V; Timer = 1 minute.

Fig 6 . Supply current I_{DD} as a function of temperature T; CLKOUT = 32 kHz



T_{amb} = 25 °C; normalized to V_{DD} = 3 V.

Fig 7. Frequency deviation as a function of supply voltage V_{DD}

Functional Description

The PCF8563T has 16 8-bit registers, an auto-incrementable address register, a built-in 32.768kHz oscillator (with an internal integrated capacitor), a frequency divider (used to clock the real-time clock RTC), a programmable clock output, a timer, an alarm, a brown-out detector, and a 400kHz I²C-bus interface.
All 16 registers are designed as addressable 8-bit parallel registers, but not all bits are useful. The first two registers (internal address 00H,01H) used as control register and state register. Address 02H~08H are used for clock counter (second to year counter), address 09H~0CH are used for alarm register (defining alarm conditions), address 0DH is used for controlling the output frequency of CLKOUT pin, address 0EH and 0FH are used for timer control register and timer register respectively. The encoding format of seconds, minutes, hours, days, months, years, minute alarms, hour alarms, and day alarm registers is BCD code, while the week and day of the week alarm registers are not encoded in BCD format.

Alarm Function

When one or more of the alarm registers MSB (AE=Alarm Enable) is cleared, the corresponding alarm condition is valid, so that an alarm is generated once per minute to once per week. Setting the alarm flag bit AF (bit 3 of control/status register 2) is used to generate an interrupt, and AF can only be cleared by software.

Timers

The 8-bit countdown counter (address 0FH) is controlled by the timer control register (address 0EH, see Table 22), which is used to set the frequency of the timer (4096Hz, 64Hz, 1Hz, or 1/60Hz) and to set the timer to be active or inactive. The timer counts down from the 8-bit binary number set by the software. At the end of each countdown, the timer sets the flag bit TF (see Table 4), which is used to generate an interrupt ($\overline{INT}$)that generates a pulse as an interrupt signal for each countdown cycle, and can only be cleared by the software. TI/TP (see Table 4) controls the conditions for interrupt generation. When the timer is read, the current countdown value is returned.

Clkout Output

The CLKOUT frequency register (address 0DH, see Table 20) determines the frequency of the output square wave, which can be 32.768 kHz (default), 1024 Hz, 32 Hz and 1 Hz. CLKOUT is an open-drain output pin that is active when energized and has a high impedance when inactive.

Reset

XBLW PCF8563T has a built-in reset circuit, which starts to work when the oscillator stops working. In the reset state, the I²C bus is initialized, and all registers (including the address pointer) are cleared to zero except for the TF, VL, TD1, TD0, TESTC, and AE bits which are set to logic one.

Power-Down Detection And Clock Monitoring

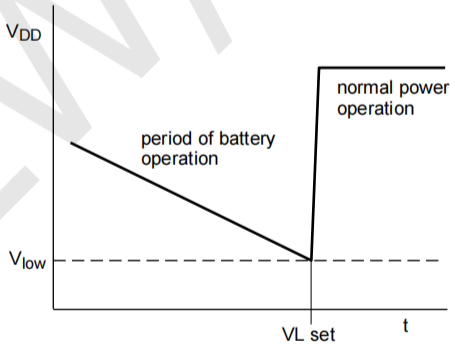


Fig 8. Voltage-low detection

The PCF8563T has an embedded power-down detection circuitry. When V_{DD} is lower than V_{LOW}, bit V_L (Voltage Low, bit 7 of the seconds register) is set to 1 to indicate that inaccurate clock/calendar information may be generated, and the VL flag bit can be cleared only by software. The V_L flag bit can only be cleared by software. When V_{DD} slowly decreases (e.g. on battery power) to V_{LOW}, V_L is set to indicate that an interrupt may be generated at this time.

Register Structure

Table 1 . Overview Of Registers

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00H	Control/Status Register 1	TEST	0	STOP	0	TESTC	0	0	0
01H	Control/Status Register 2	0	0	0	TI/ TP	AF	TF	AIE	TIE
0DH	CLKOUT Frequency Register	FE	-	-	-	-	-	FD1	FD0
0EH	Timer Control Register	TE	-	-	-	-	-	TD1	TD0
0FH	Timer Countdown Register	Timer Countdown Value							

Bits labeled " - " are invalid and bits labeled "0" shall be set to a logic 0.

Table 2 Overview Of BCD Format Registers

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02H	Second	VL	00~59BCD Code format number						
03H	Minutes	-	00~59BCD Code format number						
04H	Hourly	-	-	00~23BCD Code format number					
05H	Date	-	-	0 1~31BCD code format number					
06H	Week	-	-	-	-	-	0—6		
07H	Months/Century	C	-	-	0 1~12BCD code format number				
08H	Year	00~99BCD code format number							
09H	Minute Alarm	AE	00~59BCD Code format number						
0AH	Hourly Alarm	AE	-	00~23BCD Code format number					
0BH	Daily Warning	AE	-	0 1~31BCD code format number					
0CH	Weekly Alarm	AE	-	-	-	-	0-6		

Bits marked "-" are not valid

Control/Status Register 1

Table 3 . Control/Status Register 1 (Address 00H) Bit Descriptions

Bit Number	Symbol	Description
7	TEST1	TEST1=0: Normal mode TEST1=1 : EXT_CLK test mode
5	STOP	STOP=0: RTC clock is running; STOP=1: all RTC dividers are asynchronously set to logic 0 and the RTC clock stops running (CLKOUT is still available at 32.768kHz).
3	TESTC	TESTC=0: Power reset function disabled (set to logic 0 in normal mode) TESTC=1 : Power reset function is effective.
6,4,2~0		The default value is logic 0

Control/Status Register 2

Bits TF and AF: AF is set to a logic 1 when an alarm occurs. Similarly, TF is set to a logic 1 at the end of the timer countdown. These two values can only be changed by software. If an application requires both a timer and an alarm interrupt, it can be changed by reading both values.
Bytes are used to determine the source of the interrupt. When the bit is cleared during a write cycle, a logical AND operation is performed to prevent the flag bit from being rewritten.
Bits TIE and AIE: These two bits are used to activate the generation of interrupts. When AIE and TIE are set, the interrupt is the logical or of these two bits.

Table 4 . Bit Description of Control/Status Register 2 (Address 01H)

Bit Number	Symbol	Description
7,6,5		The default value is logic 0
4	TI/ TP	TI/TP=0: $\overline{INT}$ is active when TF is active (depends on the state of the TIE) TI/TP=1: $\overline{INT}$, pulse valid, see Table 5 (depends on the state of the TIE) Note: $\overline{INT}$ is always active when both AF and AIE are active.
3	AF	AF= 0: Alarm flag is invalid for read operation; Alarm flag is cleared for write operation. AF=1: Alarm flag is valid during read operation; alarm flag remains unchanged during write operation.
2	TF	TF=0: Timer flag is invalid for read operation; Timer flag is cleared for write operation. TF= 1: Timer flag is valid for read operation; Timer flag remains unchanged for write operation.
1	AIE	AIE=0:Alarm interrupt disabled AIE=1: Alarm interrupt enabled
0	TIE	TIE=0:Timer interrupt is disabled TIE=1:Timer interrupt enabled

Table 5 . $\overline{INT}$ Operation (Bit TI/TP = 1)

Clock Source (Hz)	$\overline{INT}$ Cycle[1]	
	n=1[2]	n >1
4096	1/8192	1/4096
64	1/128	1/64
1	1/64	1/64
1/60	1/64	1/64

[1], TF and $\overline{INT}$ are valid at the same time.
[2], n is the value of the countdown timer, when n=0, the timer stops working.

Minute And Hour Registers

Table 6 . Sec/VL Register (Address 02H) Bit Descriptions

Bit Number	Symbol	Description
6 ~ 0	(seconds)	Represents the current second value in BCD format, the value is 00~99, e.g.: 1011001 represents 59 seconds.
7	VL	VL= 0 : Ensure accurate clocks/calendar data VL= 1 : Accurate clock/calendar data not guaranteed

Table 7 . Minute Register (Address 03H) Bit Descriptions

Bit Number	Symbol	Description
7	—	null
6 ~ 0	(minutes)	Represents the current minute value in BCD format, with values from 00 to 59.

Table 8 . Hour Register (Address 04H) Bit Descriptions

Bit Number	Symbol	Description
7, 6	—	null
5 ~ 0	(Hourly)	Represents the current hour value in BCD format, with values from 00 to 23.

Day, Week, Month/Century And Year Registers

Table 9. Day Register (Address 05H) Bit Descriptions

Bit Number	Symbol	Description
7, 6	—	null
5 ~ 0	(day)	Represents the current day value in BCD format, with values from 01 to 31. The current year counter value for leap year is , TS9083 Automatically adds a value to February to make it 29 days

Table 10 . Week Register (Address 06H) Bit Descriptions

Bit Number	Symbol	Description
7 ~ 3	—	null
2 ~ 0	(weeks)	represents the current day of the week value, with values from 0 to 6. See Table 11, these bits can also be reassigned by the user.

Table 11 . Distribution of days of the week

Date	Bit 2	Bit 1	Bit 0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesdays	0	1	1
Thursdays	1	0	0
Fridays	1	0	1
Saturdays	1	1	0

Table 12 . Month/Century Register (Address 07H) Bit Descriptions

Bit Number	Symbol	Description
7	C	Century bit: C=0 designates the century as 20 XX; C=1 designates the century as 19 XX, "XX" is the value in the year register, see Table 14. XX" is the value in the year register, see Table 14. When the year is changed from 99 to 00, the century will be changed.
6, 5	—	null
4 ~ 0	(months)	Represents the value of the current month in BCD format, the value is 01~12, see Table 13.

Table 13 . Distribution of months

Months	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

Table 14 . Year Register (Address 08H) Bit Descriptions

Bit Number	Symbol	Description
7 ~ 0	(years)	Represents the current year value in BCD format, with values from 00 to 99.

Alarm Control Register

When one or more alarm registers are written with a legal minute, hour, day, or week value and their corresponding AE (Alarm Enable) bit is a logic 0, and these values are equal to the current minute, hour, day, or week value, the flag bit AF (Alarm Flag) is set, and the AF holds the set value until cleared by the software, after which it is cleared, and can only be set again if the time increment matches the alarm condition again. After AF is cleared, it can only be set again when the time increment matches the alarm condition again. Alarm registers are ignored when their corresponding bit AE is set to a logic 1.

Table 15 . Minute Alarm Register (Address 09H) Bit Descriptions

Bit Number	Symbol	Description
7	AE	AE= 0, the minute alarm is valid; AE= 1, the minute alarm is invalid.
6 ~ 0	Minute Alarm	Minute alarm value in BCD format with values from 00 to 59.

Table 16 . Hourly Alarm Register (Address 0AH) Bit Descriptions

Bit Number	Symbol	Description
7	AE	AE= 0, the hourly alarm is valid; AE= 1, the hourly alarm is invalid.
5 ~ 0	Hourly Alarm	Represents hourly alarm values in BCD format, values from 00 to 23.

Table 17 . Day Alarm Register (Address 0BH) Bit Descriptions

Bit Number	Symbol	Description
7	AE	AE=0, the daily alarm is valid; AE=1, the daily alarm is invalid.
5 ~ 0	daily warning	Represents the daily alarm value in BCD format, with values from 01 to 31.

Table 18 . Weekly Alarm Register (Address 0CH) Bit Descriptions

Bit Number	Symbol	Description
7	AE	AE= 0, week alarm valid; AE= 1, week alarm invalid
2 ~ 0	Weekly Alarm	Represents the weekly alarm value in BCD format, with values from 0 to 6.

Clkout Frequency Register

Table 19 . CLKOUT Frequency Register (Address 0DH) Bit Descriptions

Bit Number	Symbol	Description
7	FE	FE= 0 ： CLKOUT output is disabled and set to high impedance FE= 1: CLKOUT output is valid.
6 ~ 2	—	null
1	FD1	Frequency output pin (fCLKOUT) used to control CLKOUT, see Table 20
0	FD0	Frequency output pin (fCLKOUT) used to control CLKOUT, see Table 20

Table 20 .CLKOUT Frequency Selection Table

FD1	FD0	f_{CLKOUT}
0	0	32 .768kHz
0	1	1024Hz
1	0	32Hz
1	1	1Hz

Countdown Timer Register

The timer register is an 8-bit byte countdown timer which is active or inactive as determined by bit TE in the timer controller. The timer clock can also be selected by the timer controller, and other timer functions, such as interrupt generation, are controlled by control/status register 2. Other timer functions, such as interrupt generation, are controlled by control/status register 2.To accurately read back the value of the countdown , the frequency of the I²C bus clock SCL should be at least twice the frequency of the selected timer clock.

Table 21 . Timer Control Register (Address 0EH) Bit Descriptions

Bit Number	Symbol	Description
7	TE	TE= 0: Timer is invalid; TE= 1: Timer is valid.
6 ~ 2	—	null
1	TD1	Timer Clock Frequency Selection Bit, determines the clock frequency of the countdown timer, see Table 22, TD1 and TD0 should be set to "11" (1/60Hz) when not in use to minimize power loss.
0		

Table 22 . Timer Clock Frequency Selection

TD1	TD0	Timer Clock Frequency (Hz)
0	0	4096
0	1	64
1	0	1
1	1	1/60

Table 23 . Timer Countdown Value Register (Address 0FH) Bit Descriptions

Bit Number	Symbol	Description
7 ~ 0	Timer countdown value	Countdown value " n ", countdown period = n/clock frequency

Ext_Clk Test

Test mode is used for in-circuit testing, establishing test patterns, and controlling the operation of the RTC. The test mode is set by bit TEST1 of Control/Status Register 1, which makes the CLKOUT pin an input pin. In the test mode state， the frequency signal input through the CLKOUT pin replaces the on-chip 64 Hz frequency signal, with a 1-second time increment every 64 uplinks
NOTE: The clock is not synchronized to the on-chip 64Hz clock when entering the EXT_CLK test mode, and the prescaled state is not determined.

Example

1. Enter EXT_CLK test mode, set bit 7 of control/status register (TEST=1)
2. Set bit 5 of control/status register 1 (STOP=1).
3. Clear bit 5 of Control/Status Register 1 (STOP=0).
4. Set the time registers (seconds, minutes, hours, days, weeks, months/centuries, and years) to their desired values.
5. Provide 32 clock pulses to CLKOUT.
6. read the time register to observe the first change.
7. provide 64 clock pulses to CLKOUT. 8, read the time register to observe the first change.
8. read the time register to observe the second change, need to read the time register additional increments, repeat steps 7 and 8.

Source Reset(Por) Failure

The duration of the POR is directly related to the start-up time of the oscillator. An embedded long-start circuit can disable the POR to speed up device testing. The setup for this mode requires that the signal waveforms for the I²C bus pins SDA and SCL be as shown in Figure 9, with all time values in the figure being the minimum required.

When the chip enters the fail mode, it immediately stops resetting and operates in the EXT_CLK test mode via the I²C bus. Setting bit TESTC to logic 0 removes the failure mode, and failure mode can only be re-entered by setting TESTC to logic 1. Setting TESTC to a logic 0 in normal mode has no meaning unless it is intended to prevent entry into the POR failure mode.

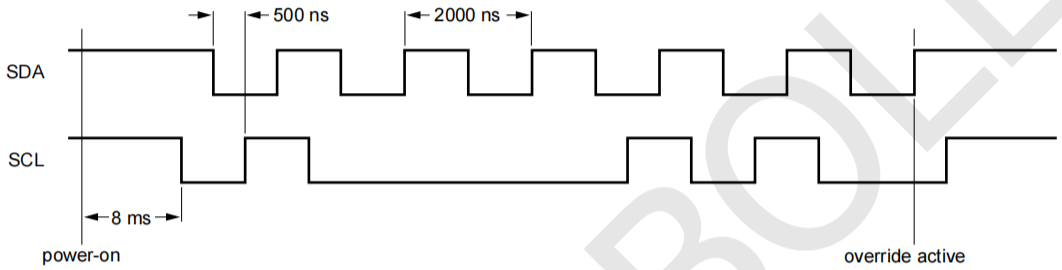


Fig 9. POR override sequence

Line Interface

The XBLW PCF8563T utilizes a serial I²C bus interface.

I²C Bus Features

The I²C bus passes information between the different chips and modules through two lines, SDA and SCL. SDA is the serial data line and SCL is the serial clock line, which must be connected to the positive supply with a pull-up resistor. Data can only be transferred when the bus is not busy.

See Figure 10 for the system configuration. The device that generates the information is the transmitter, the device that receives the information is the receiver, the device that controls the information is the master, and the device that is controlled is the slave.

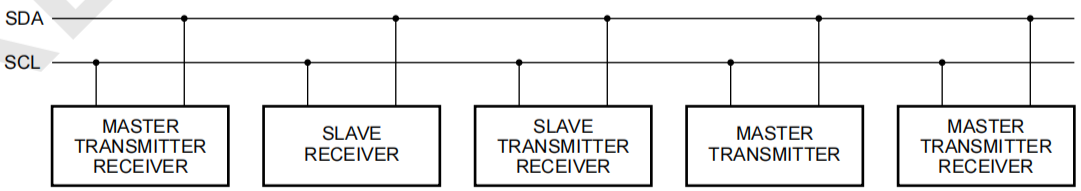


Fig 10. System configuration

Start And Stop Conditions

When the bus is not busy, the data and clock lines are held high. A start condition (S) occurs when the data line is high on the falling edge and the clock line, and a stop condition (P) occurs when the data line is high on the rising edge and the clock line, see Figure 11.

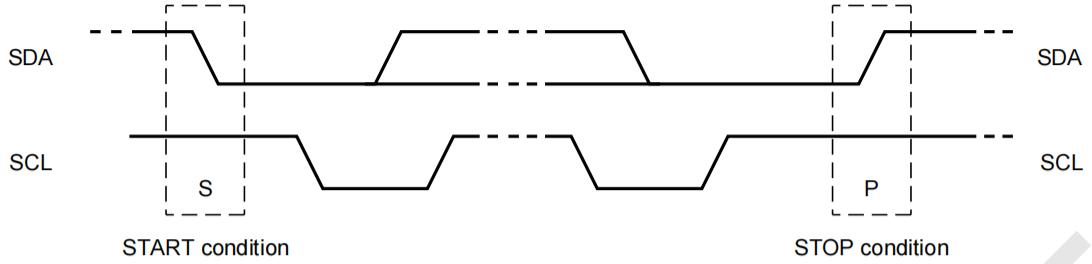


Fig 11. Definition of START and STOP conditions

Bit Transfer

Each clock pulse transmits one data bit, and the data on the SDA line should remain stable while the clock pulse is high, otherwise the data on the SDA line will not be transmitted. The data will become the control signal mentioned above , see Figure 12.

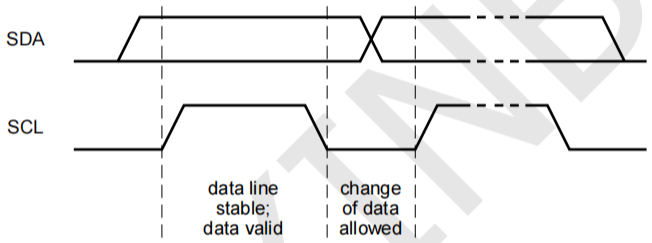


Fig 12. Bit transfer

Transponder Bit

There is no limit to the amount of data that the transmitter can send to the receiver between start and stop conditions. Each 8-bit byte is followed by an answer flag
bit, the transmitter generates a high answer flag bit, at which point the master generates an additional answer flag clock pulse. The slave receiver must generate an answer flag bit after receiving each byte, and the master receiver must generate an answer flag after receiving each byte sent from the transmitter. When the clock pulse of the response flag appears, the SDA line should remain at a low level (considering the start and hold time). The transmitter should release SDA after receiving the last byte from the slave device, causing the receiver to generate a response flag, at which point the master device can generate a stop condition.

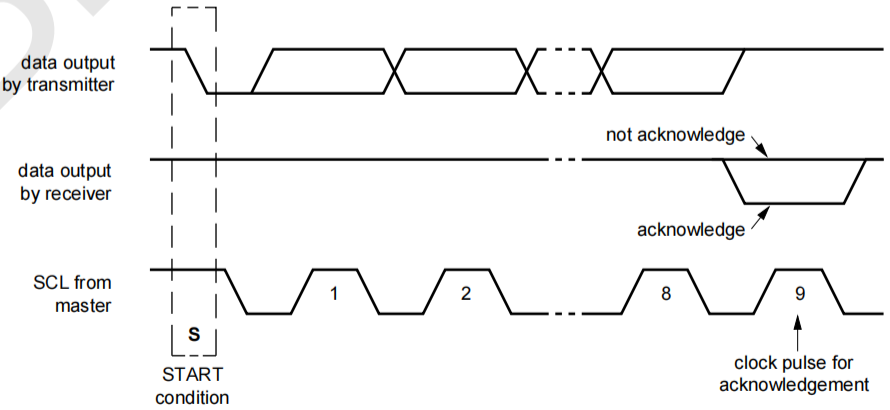


Fig 13. Acknowledgement on the I²C-bus

I²C Bus Protocol

Note: Before transferring data on the I²C bus, the receiver device should be labeled with an address, which is transmitted together with the first byte after the I²C bus has been activated. The XBLW PCF8563T can be used as a slave receiver or a slave transmitter, in which case the clock signal line SCL can only be an input signal line. Data Signal Line SDA is a bidirectional signal line.
See Figure 14 for the slave address of the XBLW PCF8563T .

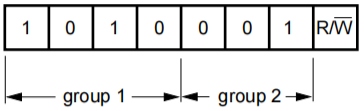


Fig 14. Slave address

Time/Calendar Read/Write Cycles

The XBLW PCF8563T has three configurations of serial I²C bus read/write cycles, see Figures 15, 16, and 17, where the word address is 4 bits.The first four bits of the word address are not used to indicate the next register to be accessed.

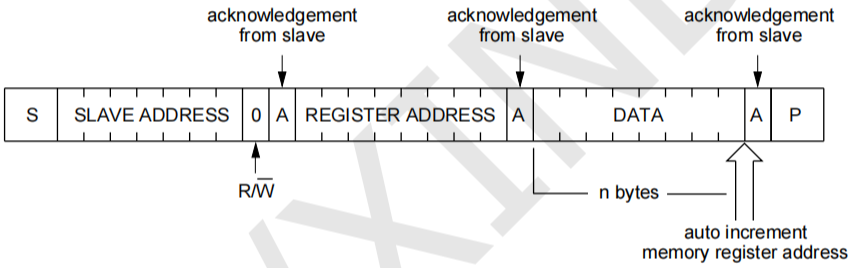
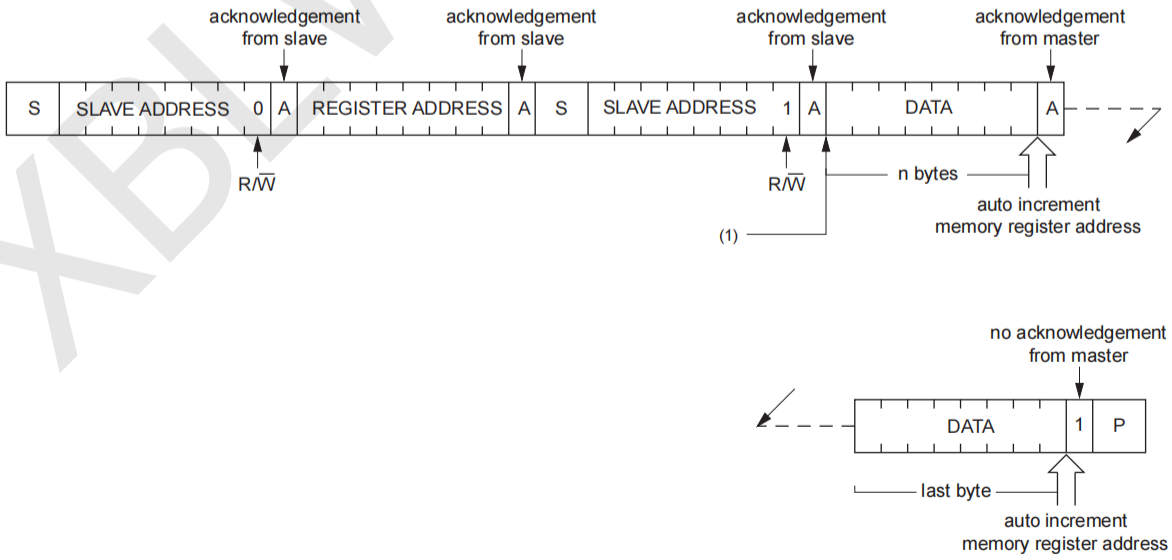


Fig 15. Master transmits to slave receiver (WRITE mode)



(1) At this moment master transmitter becomes master receiver and XBLW PCF8563T slave receiver becomes slave transmitter.

Fig 16. Master reads after setting register address (write register address; READ data)

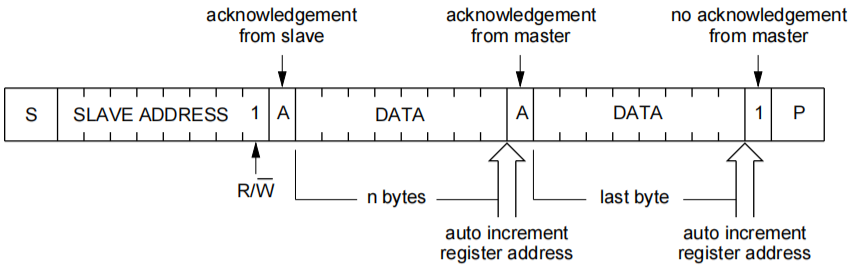


Fig 17. Master reads slave immediately after first byte (READ mode)

In-Crystal Frequency Adjustment

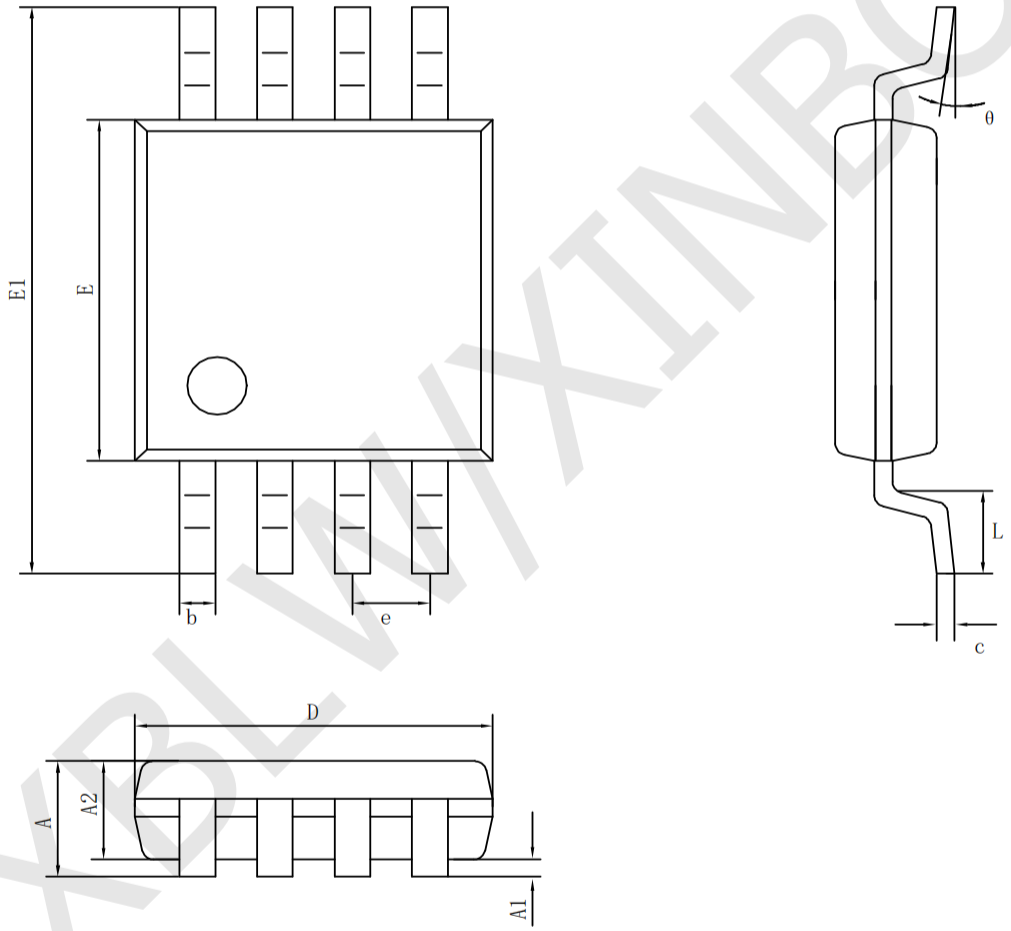
Method 1: Constant OSCI Capacitance - Calculate the average value of capacitance required, use a constant capacitance of this value, and measure it on the CLKOUT pin after powering up the device. The frequency should be 32.768 kHz, and the deviation of the measured frequency value depends on the quartz crystal, capacitance deviation, and inter-device deviation (average ± 5×10^{-6}).
The average deviation can be controlled within ±5 minutes/year.

Method 2: OSCI Trimming Capacitor - The oscillator frequency can be adjusted to an accurate value by adjusting the trimming capacitor on the OSCI pin, and the frequency value on the CLKOUT pin can be measured to be 32.768kHz when power is applied.
Method 3: OSCO Output - Measure the OSCO output directly (taking into account the capacitance of the test probe).

Package Information

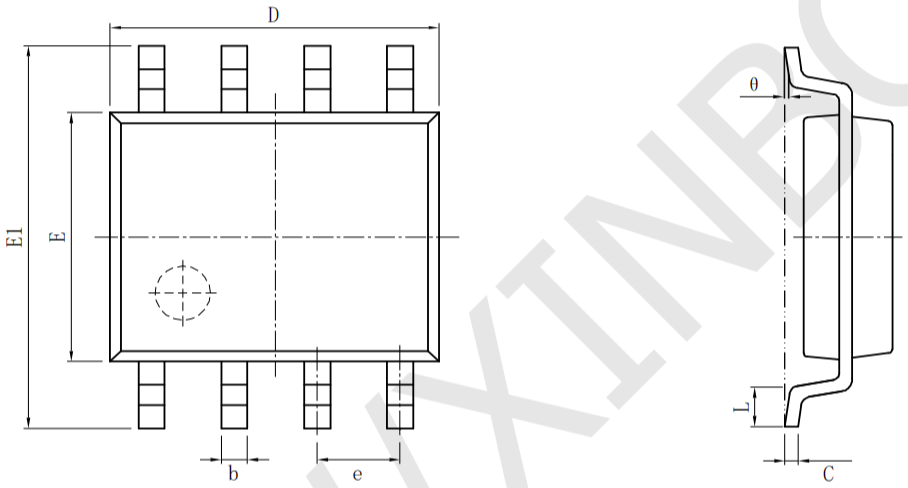
· MSOP-8

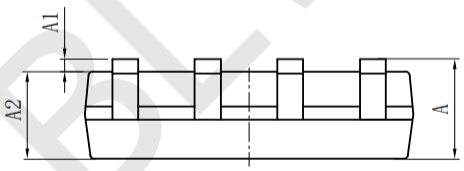
Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	0.820	1.100	A	0.320	0.043
A1	0.020	0.150	A1	0.001	0.006
A2	0.750	0.950	A2	0.030	0.037
b	0.250	0.380	b	0.010	0.015
c	0.090	0.230	c	0.004	0.009
D	2.900	3.100	D	0.114	0.122
e	0.65 (BSC)		e	0.026(BSC)	
E	2.900	3.100	E	0.114	0.122
E1	4.750	5.050	E1	0.187	0.199
L	0.400	0.800	L	0.016	0.031
θ	0°	6°	θ	0°	6°



- SOP-8

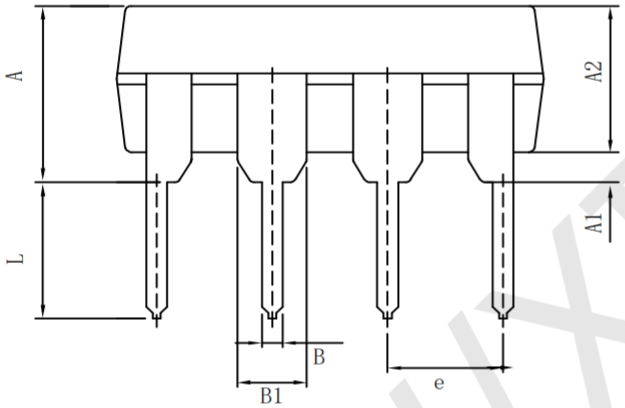
Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	1.350	1.750	A	0.053	0.069
A1	0.100	0.250	A1	0.004	0.010
A2	1.350	1.550	A2	0.053	0.061
b	0.330	0.510	b	0.013	0.020
c	0.170	0.250	c	0.006	0.010
D	4.700	5.100	D	0.185	0.200
E	3.800	4.000	E	0.150	0.157
E1	5.800	6.200	E1	0.228	0.224
e	1.270(BSC)		e	0.050(BSC)	
L	0.400	1.270	L	0.016	0.050
θ	0°	8°	θ	0°	8°

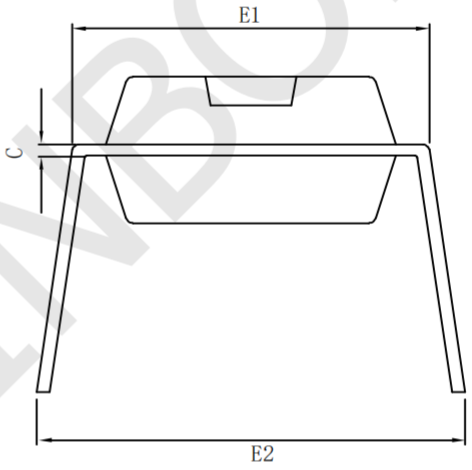


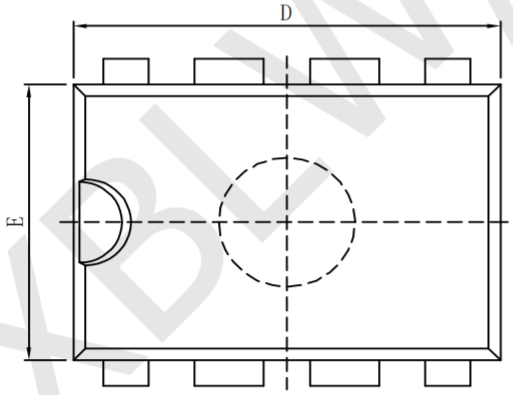


• DIP-8

Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	3.710	4.310	A	0.146	0.170
A1	0.510		A1	0.020	
A2	3.200	3.600	A2	0.126	0.142
B	0.380	0.570	B	0.015	0.022
B1	1.524(BSC)		B1	0.060(BSC)	
C	0.204	0.360	C	0.008	0.014
D	9.000	9.400	D	0.354	0.370
E	6.200	6.600	E	0.244	0.260
E1	7.320	7.920	E1	0.288	0.312
e	2.540(BSC)		e	0.100(BSC)	
L	3.000	3.600	L	0.118	0.142
E2	8.400	9.000	E2	0.331	0.354







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