EVAL-ADuM4221-1EBZ User Guide

UG-1857

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Evaluating the ADuM4221-1 Isolated, Half Bridge Gate Driver with Adjustable Dead Time, 4 A Output

FEATURES

Adjustable dead time
Output voltage range to 35 V
Screw terminals for easy connectivity
Pad placement for external series gate resistors
Pad placement for capacitive load testing
Supports TO-220 or TO-252 IGBTs or MOSFETs
Bootstrap option
Jumper placement for easy half bridge setup

EVALUATION KIT CONTENTS

EVAL-ADuM4221-1EBZ evaluation board

EQUIPMENT NEEDED

Suggested test equipment
- **Primary side power supply: 0 V to 6.5 V at 100 mA**
- **2 secondary side supplies: 0 V to 35 V at 250 mA**
- **Square wave generator: 0 V to 5 V**

GENERAL DESCRIPTION

The EVAL-ADuM4221-1EBZ supports the ADuM4221-1 half bridge gate driver that employs Analog Devices, Inc., *i*Coupler® technology to provide independent and isolated high-side and low-side output. The EVAL-ADuM4221-1EBZ is populated with the ADuM4221-1, which has a single PWM input and dead time control. The EVAL-ADuM4221-1EBZ supplies jumpers and screw terminals to configure different drive conditions. The EVAL-ADuM4221-1EBZ operates with square waves and dc values on the PWM and DISABLE pins.

The ADuM4221-1 operates with an input supply ranging from 2.5 V to 6.5 V, providing compatibility with lower voltage systems. The logic level voltage at the input PWM pin controls the V_{OA} and V_{OB} outputs. The driver has a DISABLE input pin that, if held high, shuts the device off regardless of the input on the channels. The input on the PWM pin generates the complementary outputs, V_{OA} and V_{OB}, with basic overlap protection, and the dead time (DT) pin on the primary side allows an adjustable dead time between these output transitions.

The ADuM4221-1 provides operation with voltages of up to 35 V on the secondary side. The EVAL-ADuM4221-1EBZ has a provision for the high-side supply to be bootstrapped to the low-side supply. The EVAL-ADuM4221-1EBZ facilitates testing of the propagation delay, drive strength, dead time operation, and input logic of the device. Because the EVAL-ADuM4221-1EBZ has footprints for insulated gate bipolar transistors (IGBTs) and metal-oxide semiconductor field effect transistors (MOSFETs) in TO-220 and TO-252 packages, the ADuM4221-1 can be evaluated with many different power devices.

For complete information about the ADuM4221-1, refer to the ADuM4221-1 data sheet in conjunction with this user guide when using the EVAL-ADuM4221-1EBZ.

EVAL-ADUM4221-1EBZ PHOTOGRAPH

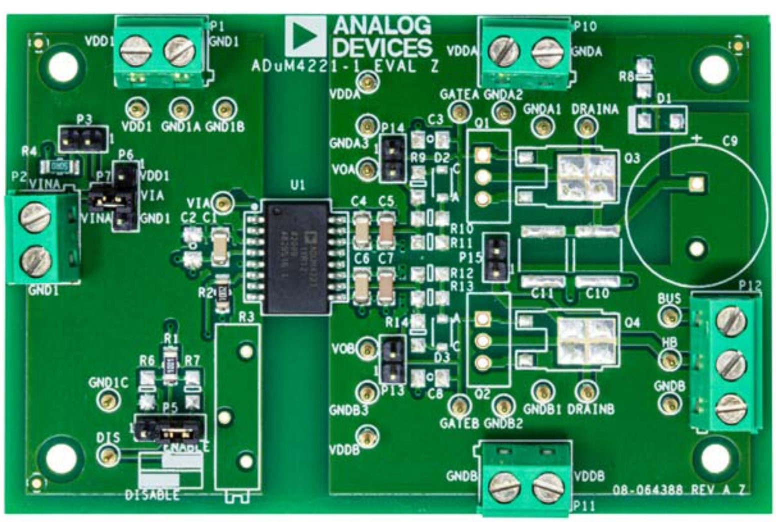

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Figure 1.

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REVISION HISTORY

8/2020—Revision 0: Initial Version

EVAL-ADUM4221-1EBZ HARDWARE

INITIAL CONFIGURATION

In stock configuration (see Figure 1), the EVAL-ADuM4221-1EBZ is set up for testing the basic gate driver functionality under a no load condition. Either screw terminals or test pins can be used for the input, output, and signal connections to the board. The R9 to R14 resistors are not populated. These locations of the series external resistors serve as the charging and discharging paths of the device being driven. R9 to R11 are for the high-side output, and R12 to R14 are for the low-side output. However, before initial use, it is recommended to complete certain steps to prepare the EVAL-ADuM4221-1EBZ for operation.

PAD LAYOUT FOR THE DEVICE UNDER TEST (DUT)

The EVAL-ADuM4221-1EBZ provides placement for supporting components to facilitate evaluation of the gate driver. The available pad placements are as follows:

- U1 is the footprint for the ADuM4221-1.
- C1, C4, and C6 are 0.1 µF bypass capacitors, C5 and C7 are 10 µF bypass capacitors, and C2 (not populated) is 1 µF, in a surface-mount device (SMD), Size 1206 package.
- Q1 and Q2 can be populated with TO-220 package MOSFETs or IGBTs, and Q3 and Q4 with TO-252 package MOSFETs or IGBTs (see Figure 2). In Figure 2, C/D is collector/drain, G is gate, and E/S is emitter/source.
- R9 to R14 are gate resistors that control the slew rate of the outputs, and can be populated with Size 1206, SMD resistors in the 1 Ω to 10 Ω range.
- The C3 and C8 capacitor pad placements provide land patterns for placing a capacitor load to simulate gate capacitance.
- D1 and R8 can be populated for using a bootstrap supply for the high side driver.
- R3 (not populated) is a variable resistor up to 500 kΩ.

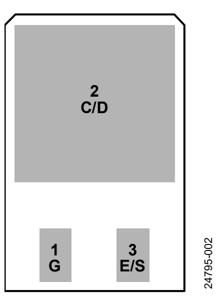

Figure 2. IGBT/MOSFET Footprint

SETTING UP THE EVAL-ADUM4221-1EBZ

It is recommended to use Size 1206, surface-mount, external gate resistors with values between approximately 1 Ω and 10 Ω, depending on the required drive strength for the load being driven. Diode D2 and Diode D3 are not populated but can be used for providing a different turn on and turn off path. An IGBT or MOSFET can be placed in the provided Q1 or Q3 and Q2 or Q4 landing patterns. Jumpers P13 and P14 allow shorting across the series external resistors on the low side and the high side, respectively, to observe overshoot or allow the user to probe the voltage to quantify peak currents.

A 10 kΩ dead time resistor is placed at R2, but it can be replaced with any value in the range of 10 kΩ to 500 kΩ to provide a corresponding dead time between the high-side and the low-side outputs of the ADuM4221-1. Potentiometer R3 (not populated) can be used instead of R2 for faster dead time adjustment.

The combination of Resistor R4 and Jumper P3 allows the user to terminate the logic input with a 50 Ω load. R4 is not required, and, if not connected through the jumper, the EVAL-ADuM4221-1EBZ accepts high impedance, generator signals from an external source.

A jumper on P6 allows the user to easily connect PWM (labeled VIA on the EVAL-ADuM4221-1EBZ board) to V_{DD1} or GND_1, (see Figure 3).

Figure 3. Example of P6 Configured to Connect Input to DC Values

Screw terminals are the preferred method to connect the logic level input on the EVAL-ADuM4221-1EBZ because this method provides added flexibility for making a connection to the input pin of the device.

Placing a Jumper between P6 and P7 connects PWM to an external input voltage signal (labeled VINA) on the EVAL-ADuM4221-1EBZ (see Figure 1). The VIA test pin directly connects to the input PWM pin of the device under test (DUT) and eliminates the need to use the screw terminals or any combination of jumpers when the device is driven by an external signal. The user can choose to utilize either a direct pin connection or the screw terminal method to make the connection. However, when the VIA test pin is used to connect to an external source, care must be taken to ensure that there is no jumper on P6, which connects to dc values. Connection between P6 and P7 can still be made if termination is required in combination with placing the jumper on P3.

POWER CONNECTIONS

Follow these steps to connect the EVAL-ADuM4221-1EBZ to a power supply (see Figure 4):

1. Connect the input V_{DD1} supply (2.5 V to 6.5 V) with the positive terminal to the V_{DD1} pin and ground to the GND_1 pin.
2. Connect the V_{DDB} supply (4.5 V to 35 V) with the positive terminal to the V_{DDB} pin and ground to the GND_B pin.
3. Connect the V_{DDA} supply (4.5 V to 35 V) with the positive terminal to the V_{DDA} pin and ground to the GND_A pin.

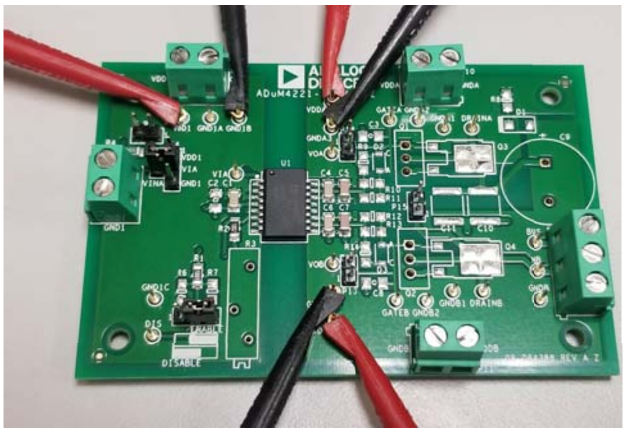

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Figure 4. Power Supply Connections

GND_1, GND_A, and GND_B are all isolated from each other. The high-side IGBT emitter/MOSFET source is connected to GND_A, and low-side IGBT emitter/MOSFET source is tied to GND_B.

INPUT/OUTPUT CONNECTIONS

The PWM pin is a logic level input compatible with 3.3 V and 5 V systems. If using a screw terminal, connect PWM to VINA by connecting P7 and Pin 2 (center pin) of P6 with a jumper or by using the VIA test pin. Only one of the outputs is high at any given time due to the built in overlap protection, and the default dead time is about 62 ns with a 10 kΩ resistor at R2.

In stock configuration, the P5 header jumper connects Pin 2 and Pin 3 (two pins on the right side) to enable operation of the device outputs. Connecting Pin 1 and Pin 2 of P5 disables the device. The disable function can be controlled externally by connection to the disable (DIS) test pin. R6 and R7 can be used as pull-up and pull-down resistors, respectively, for the disable input.

The half bridge output (HB) test pin on the EVAL-ADuM4221-1EBZ is the Q2/Q4 collector/drain node. If the device is used in the half bridge configuration, the Q1/Q3 emitter/source can be connected to HB with a jumper across P15. The bus voltage (BUS) test pin on the EVAL-ADuM4221-1EBZ connects to the drain of the high-side Q1 and Q3 MOSFET/IGBT. It is recommended to use a 100 μF electrolytic capacitor for C9 and 2.2 μF ceramic capacitors for C10 and C11.

The EVAL-ADuM4221-1EBZ comes with screw terminals for both the input and output connections. These terminals facilitate connection options but are not ideal for recording transient measurements to assess the ADuM4221-1 performance. Using the output screw terminals as the sensing node often results in overshoot during measurement. When conducting measurements on the load, whether through the IGBT, MOSFET, or load capacitor, small loop measurements are recommended for optimal results. Thus, use the output screw terminals only for connection of the external load.

BOOTSTRAPPING V_{DDB} TO V_{DDA}

To use a single supply on the secondary side in a bootstrap setup, populate the bootstrap diode, D1, and Resistor R8 with a value typically in the 1 Ω to 20 Ω range. In this setup, both outputs of the ADuM4221-1 can be powered by the V_{DDB} supply when a half bridge is configured with Q1 and Q2 or Q3 and Q4. When the switch node (GND_A) is low, C4 and C5 are charged through the forward biased bootstrapping diode. When the switch node rises to the bridge voltage, the diode becomes reverse biased, and because of the charge on C4 and C5, V_{DDA} to GND_A almost equals V_{DDB}, accounting for the forward drop of the diode. For bootstrapping to work, Q1 and Q2 or Q3 and Q4 must be populated instead of the load capacitors, C3 and C8, and a jumper must be placed on P15. To supply C4 and C5 with the charge required to drive the Q1 or Q3 gate, the switching frequency must be sufficiently high, and the duty cycle must be limited.

EVALUATION BOARD SCHEMATIC AND ARTWORK

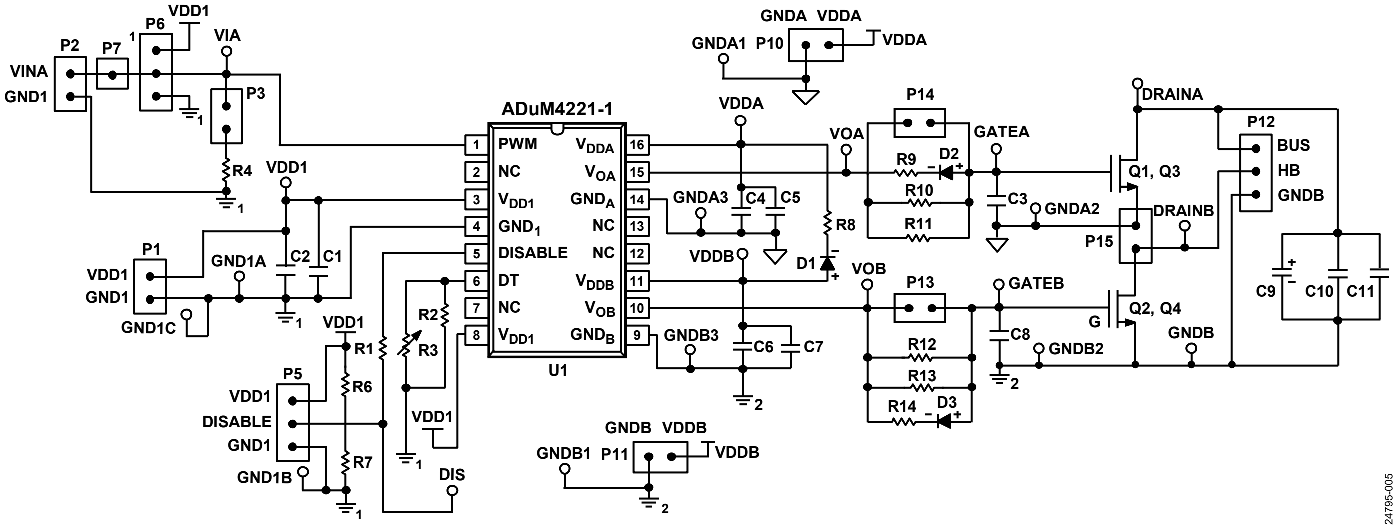

Figure 5. Schematic of the EVAL-ADuM4221-1EBZ

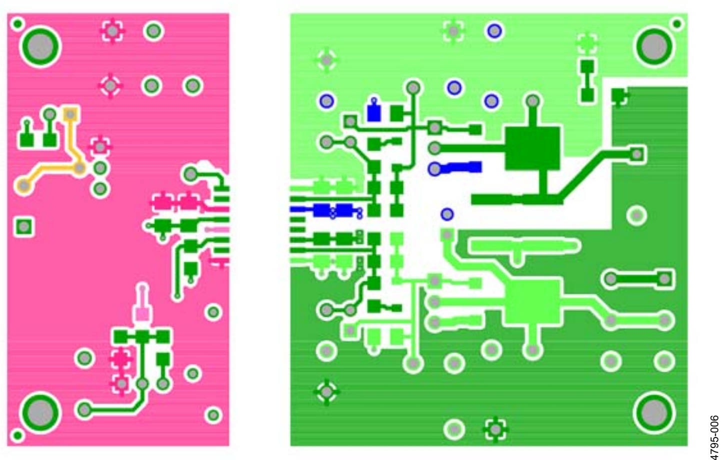

Figure 6. EVAL-ADuM4221-1EBZ Top Layer

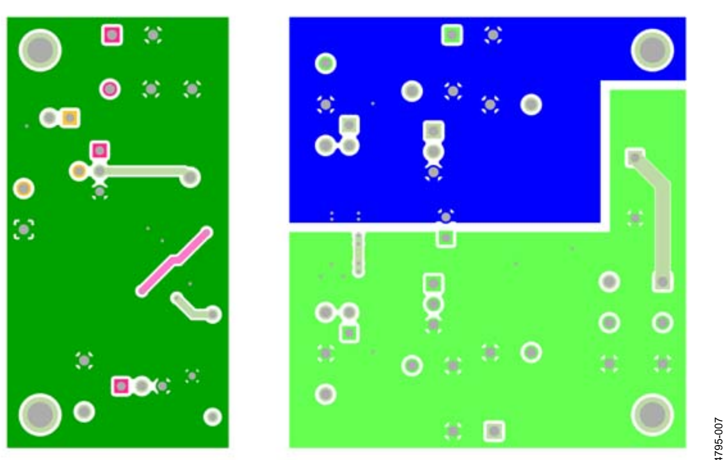

Figure 7. EVAL-ADuM4221-1EBZ Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 1. Bill of Materials

Reference Designator	Description
U1	ADuM4221-1, RI-16-2
R1	Resistor, 1 kΩ, 1206
R2	Resistor, 10 kΩ, 1206
R4	Resistor, 50 Ω, 1206
C1, C4, C6	Capacitor, 0.1 µF, 10%, 1206
C5, C7	Capacitor, 10 µF, 10%, 1206
D1	Diode, not installed, DO214AC package
D2, D3	Diode, not installed, SOD123FL package
R3	Resistor, not installed, 0.190 in. × 0.750 in. package
R6 to R14	Resistor, not installed, 1206
C2, C3, C8,	Capacitor, not installed, 1206
C9	Capacitor, not installed, 0.630 in. diameter
C10, C11	Capacitor, not installed, 2220
Q1, Q2	IGBT or MOSFET, not installed, TO-220
Q3, Q4	IGBT or MOSFET, not installed, TO-252