TECH PUBLIC
台舟电子

SN74LVC2G04DRLR-G
DUAL INVERTER GATE

WWW.TECHPUBLIC.COM

Features

- Operation voltage range: 1.65~5.5V
- Inputs Accept Voltages up to 5.5 V Allowing Down Translation to VCC
- ±24mA output drive (VCC=3.3V)
- Low Power Consumption, 10-μA Max ICC
- ESD Protection Exceeds JESD 22
  -2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  -1000-V Charged-Device Model (C101)

Applications

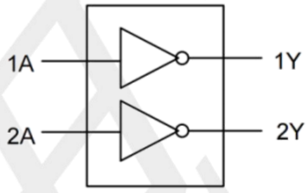
- AV Receiver
- Audio Dock:Portable
- IP Phones: Wired and Wireless
- Embedded PC
- Personal Digital Assistant(PDA)
- Power: Telecom DC/DC Module: Analog and Digital

General Description

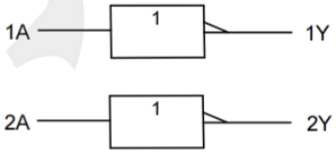
he TP74LVC2G04 is a dual inverter gate, it provides the function $Y = \overline{A}$.

This device has power-down protective circuit, preventing device destruction when it is powered down.

Logic Diagram



Logic symbol

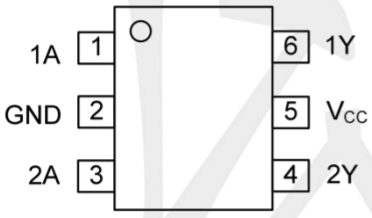


IEC logic symbol

Ordering Information

ORDER NUMBER	PACKAGE DESCRIPTION	PACKAGE OPTION	Marking
SN74LVC2G04DRLR-G	SOT563	Tape and Reel,4000	1K7

Pin Configuratio



SOT563

Function Table

INPUT(nA)	OUTPUT(nY)
H	L
L	H

Note:H: HIGH voltage level;L: LOW voltage level.

Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +6.5	V
Input Voltage	V_{IN}		-0.5 ~ +6.5	V
Output Voltage	V_{OUT}	Power-Down Mode	-0.5 ~ +6.5	V
		Active Mode	-0.5 ~ V_{CC}+0.5	V
VCC or GND Current	I_{CC}		±100	mA
Continuous Output Current	I_{OUT}	V_{OUT}=0~V_{CC}	±50	mA
Input Clamp Current	I_{IK}	V_{IN}<0	-50	mA
Output Clamp Current	I_{OK}	(V_{OUT}>V_{CC} or V_{OUT}<0)	-50	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	℃
Operating Junction Temperature	T_J		-40 ~ +125	℃
Junction to Ambient	θ_{JA}	SOT563	250	℃/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65	--	5.5	V
Input Voltage	V_{IN}		0	--	5.5	V
Output Voltage	V_{OUT}	Power-Down Mode	0	--	5.5	V
		Active Mode	0	--	VCC	V
Input Transition Rise or Fall Rate	t_R / t_F	V_{CC}=1.65V to 2.7V	--	--	20	ns/V
		V_{CC}=2.7V to 5.5V	--	--	10	ns/V

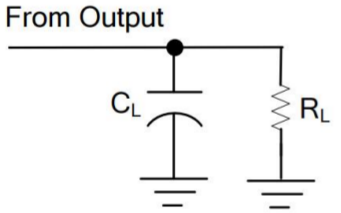
Electrical Characteristics (TA =25°C， unless otherwise specified)

PARAMETER	SYMBOL	TEST Conditions	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	VCC=1.65V ~ 1.95V	0.65×V_{CC}	--	--	V
		VCC=2.3V ~ 2.7V	1.7	--	--	V
		VCC=2.7V ~ 3.6V	2	--	--	V
		VCC=4.5V ~ 5.5V	0.7×V_{CC}	--	--	V
Low-Level Input Voltage	V_{IL}	V_{CC}=1.65V ~ 1.95V	--	--	0.35×V_{CC}	V
		V_{CC}=2.3V ~ 2.7V	--	--	0.7	V
		V_{CC}=2.7V ~ 3.6V	--	--	0.8	V
		V_{CC}=4.5V ~ 5.5V	--	--	0.3×V_{CC}	V
High-Level Output Voltage	V_{OH}	V_{CC}=1.65 ~ 5.5V, I_{OH}=-100μA	V_{CC}-0.1	--	--	V
		V_{CC}=1.65V, I_{OH}=-4mA	1.2	--	--	V
		V_{CC}=2.3V, I_{OH}=-8mA	1.9	--	--	V
		V_{CC}=2.7V,I_{OH}=-12mA	2.2	--	--	V
		V_{CC}=3.0V,I_{OH}=-24mA	2.3	--	--	V
		V_{CC}=4.5V, I_{OH}=-32mA	3.8	--	--	V
Low-Level Output Voltage	V_{OL}	V_{CC}=1.65 ~ 5.5V, I_{OL}=100μA	--	--	0.1	V
		V_{CC}=1.65V, I_{OL}=4mA	--	--	0.45	V
		V_{CC}=2.3V, I_{OL}=8mA	--	--	0.3	V
		V_{CC}=2.7V,I_{OH}=12mA	--	--	0.4	V
		V_{CC}=3.0V,I_{OH}=24mA	--	--	0.55	V
		V_{CC}=4.5V, I_{OH}=32mA	--	--	0.55	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=0 ~ 5.5V, V_{IN}=5.5V or GND	--	±0.1	±5	uA
Power OFF Leakage Current	I_{OFF}	V_{CC}=0V, V_{IN} or V_{OUT}=5.5V	--	±0.1	±10	uA
Quiescent Supply Current	I_Q	VCC= 5.5V, VIN=VCC or GND, IOUT=0A	--	0.1	10	uA
Additional Quiescent Supply ent Per Input Pin	ΔI_Q	V_{CC}=2.3 ~ 5.5V, One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND	--	5	500	uA

SWITCHING CHARACTERISTICS (TA =25°C , unless otherwise specified)

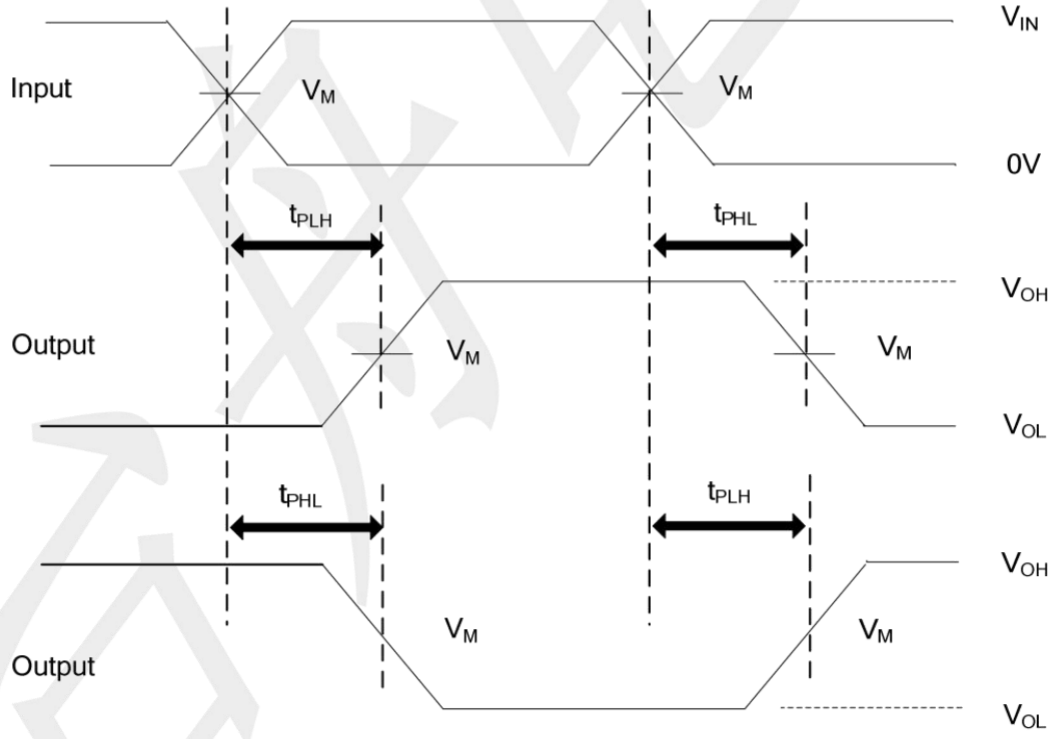
PARAMETER	SYMBOL	TEST Conditions		MIN	TYP	MAX	UNIT
Propagation delay from input (A) to output(Y)	t_{PLH} / t_{PHL}	C_L=30pF	V_{CC}=1.8±0.15V,R_L=1K Ω	1.0	3.5	8.0	nS
			V_{CC}=2.5±0.2V,R_L=500 Ω	1.0	2.2	4.4	nS
		C_L=50pF	V_{CC}=2.7 R_L=500 Ω	1.0	2.7	5.2	nS
			V_{CC}=3.3±0.3V, R_L=500 Ω	0.5	2.7	4.1	nS
			V_{CC}=5.0±0.5V,R_L=500 Ω	1.0	1.9	3.2	nS

TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

V_{CC}	Inputs		V_M	C_L	R_L
	V_{IN}	t_R, t_F			
1.8V±0.15V	V_{CC}	≤2ns	V_{CC}/2	30pF	1KΩ
2.5V±0.2V	V_{CC}	≤2ns	V_{CC}/2	30pF	500Ω
2.7V	2.7V	≤2.5ns	1.5V	50pF	500Ω
3.3V±0.3V	2.7V	≤2.5ns	1.5V	50pF	500Ω
5V±0.5V	V_{CC}	≤2.5ns	V_{CC}/2	50pF	500Ω



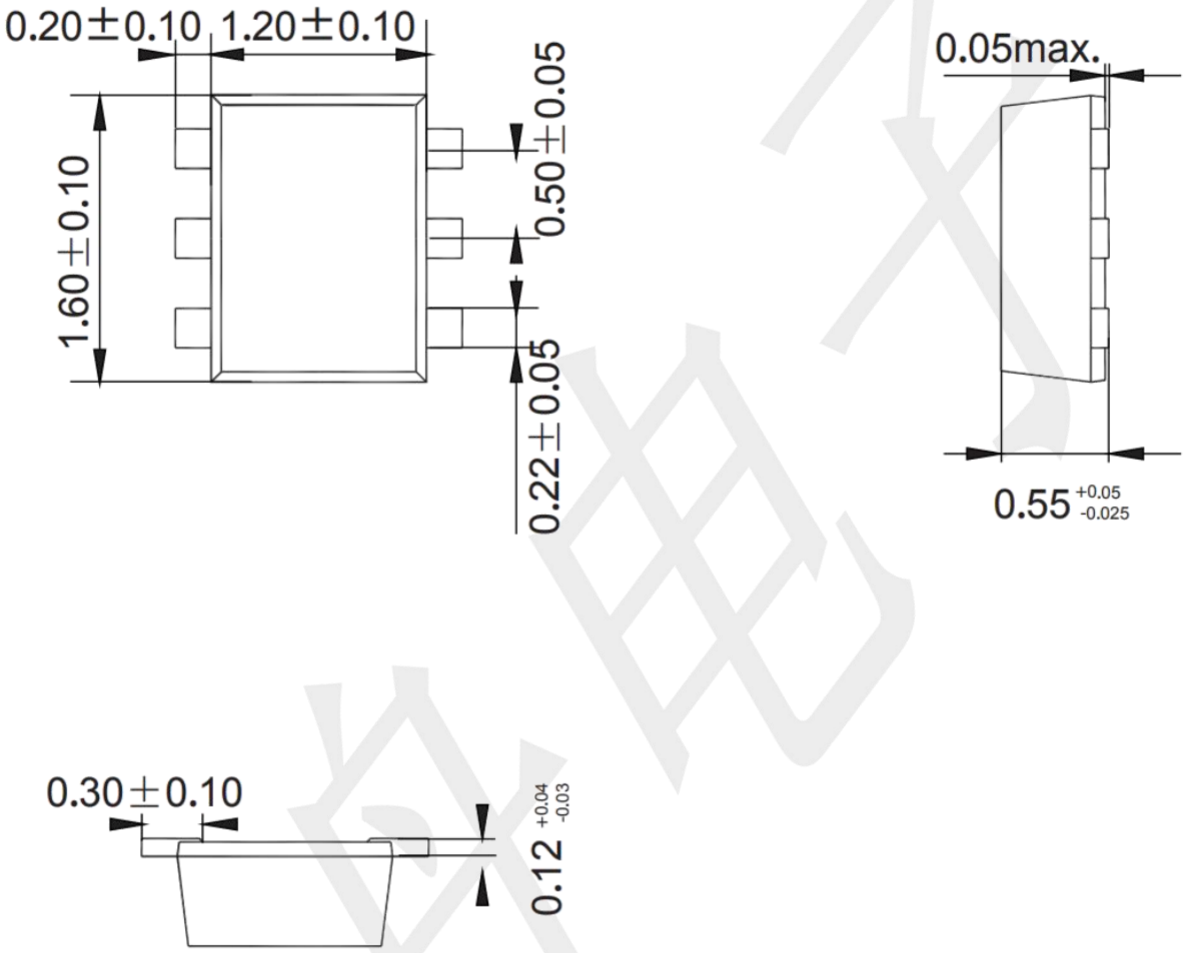
PROPAGATION DELAY TIMES

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O=50Ω.

Package information

SOT563 (unit: mm)



Mounting Pad Layout (unit: mm)