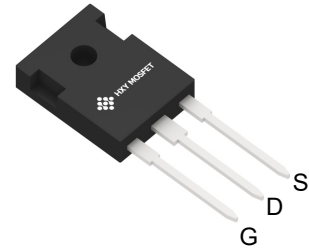




Description

The NVHL095N65S3F use super junction technology and design to provide excellent RDS(ON) with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

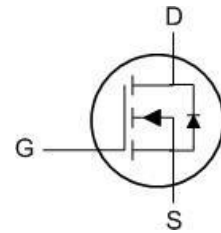
The NVHL095N65S3F meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.



TO-247

Features

- Super Low Gate Charge
- 100% EAS Guaranteed
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced trench gate super junction technology



Ordering Part Number	Package	Qty(PCS)
NVHL095N65S3F	TO-247	30



Maximum Ratings (T_c = 25 °C unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	650	V
V _{GS}	Gate-Source Voltage	±30	V
I _D @T _C =25°C	Continuous Drain Current, V _{GS} @ 10V ^{1,6}	40	A
I _D @T _C =100°C	Continuous Drain Current, V _{GS} @ 10V ^{1,6}	29	A
I _{DM}	Pulsed Drain Current ²	160	A
EAS	Single Pulse Avalanche Energy ³	750	mJ
I _{AS}	Avalanche Current	---	A
P _D @T _C =25°C	Total Power Dissipation ⁴	470	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C
R _{θJA}	Thermal Resistance Junction-ambient ¹	41	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	0.27	°C/W



Electrical Characteristics (at $T_J = 25^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	650	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1mA$	---	---	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=21.5A$	---	75	90	$m\Omega$
		$V_{GS}=4.5V, I_D=21.5A$	---	---	---	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	3.2	---	4.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	---	---	$mV/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=650V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	5	μA
		$V_{DS}=650V, V_{GS}=0V, T_J=150^\circ\text{C}$	---	1000	---	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 30V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=20V, I_D=21.5A$	---	30	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	1	---	Ω
Q_g	Total Gate Charge	$V_{DS}=480V, V_{GS}=10V, I_D=21.5A$	---	84	---	nC
Q_{gs}	Gate-Source Charge		---	28	---	
Q_{gd}	Gate-Drain Charge		---	36	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{GS}=10V, V_{DS}=400V,$ $R_G=27\Omega, I_D=21.5A$	---	89	---	ns
T_r	Rise Time		---	131	---	
$T_{d(off)}$	Turn-Off Delay Time		---	204	---	
T_f	Fall Time		---	69	---	
C_{iss}	Input Capacitance	$V_{DS}=100V, V_{GS}=0V, f=1MHz$	---	3445	---	pF
C_{oss}	Output Capacitance		---	134	---	
C_{rss}	Reverse Transfer Capacitance		---	0.6	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	40	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=21.5A, T_J=25^\circ\text{C}$	0.7	0.9	1.1	V
t_{rr}	Reverse Recovery Time	$I_F=21.5, di/dt=100A/\mu s,$ $T_J=25^\circ\text{C}$	---	113	---	nS
Q_{rr}	Reverse Recovery Charge		---	0.6	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $T_J = 25^\circ\text{C}, V_{DD}=200V, V_{GS}=10V, L=30mH$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.



Typical Performance Characteristics

Fig 1. Output Characteristics ($T_J=25^\circ\text{C}$)

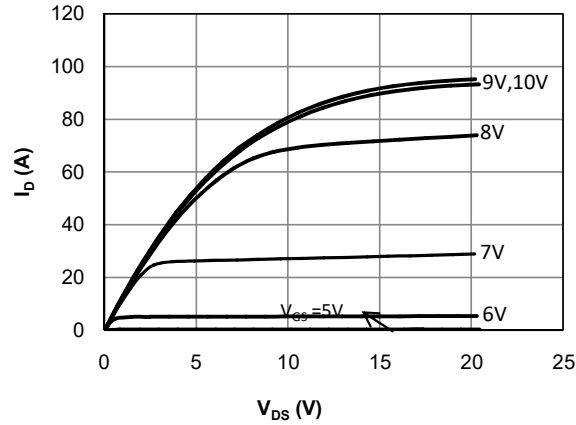


Fig 2. Output Characteristics ($T_J=150^\circ\text{C}$)

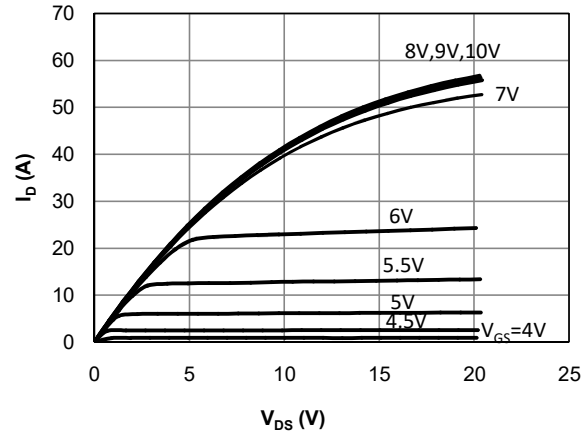


Fig 3: Transfer Characteristics

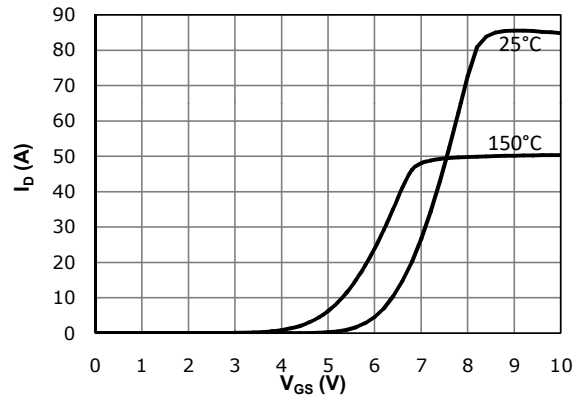


Fig 4: V_{TH} vs. T_J Temperature Characteristics

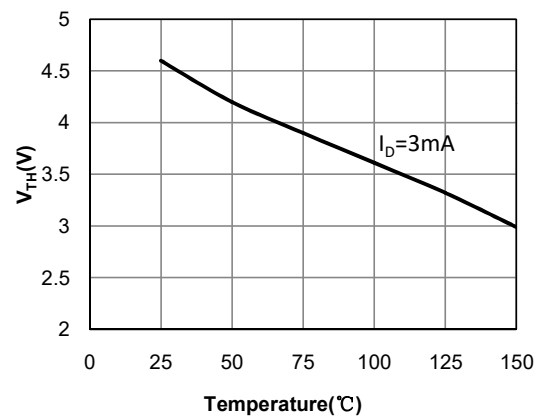


Fig 5: $R_{DS(on)}$ vs. I_{DS} Characteristics ($T_J=25^\circ\text{C}$)

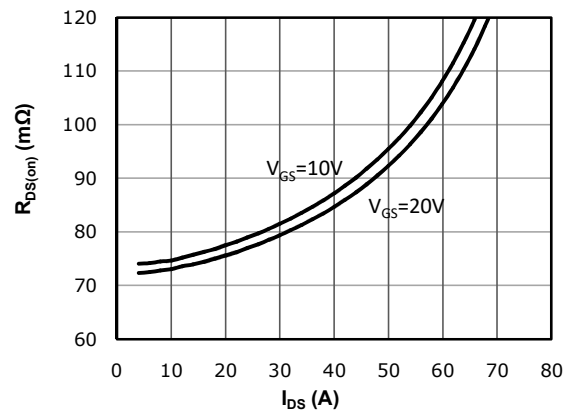


Fig 6: $R_{DS(on)}$ vs. Temperature

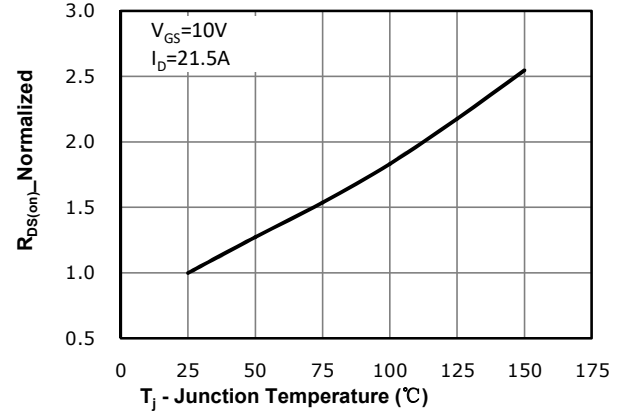




Fig 7: BV_{DSS} vs. Temperature

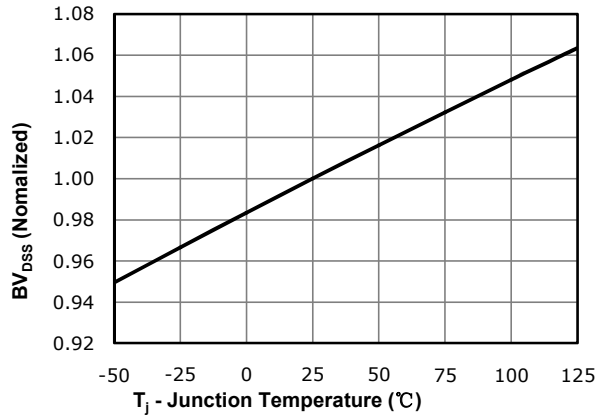


Fig 8: $R_{DS(on)}$ vs. Gate Voltage

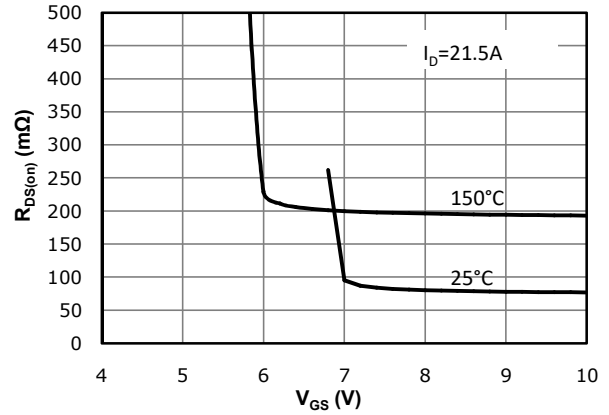


Fig 9: Body-diode Forward Characteristics

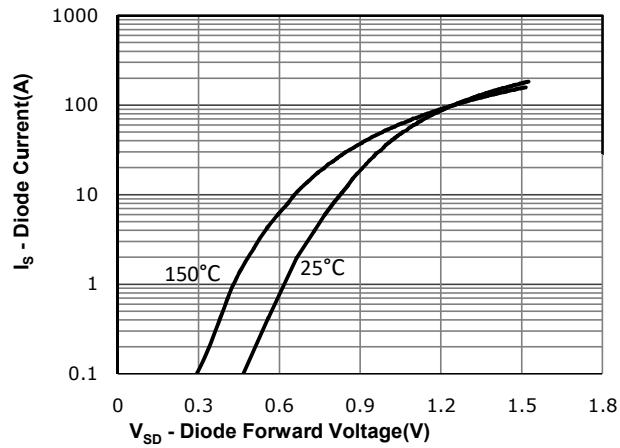


Fig 10: Gate Charge Characteristics

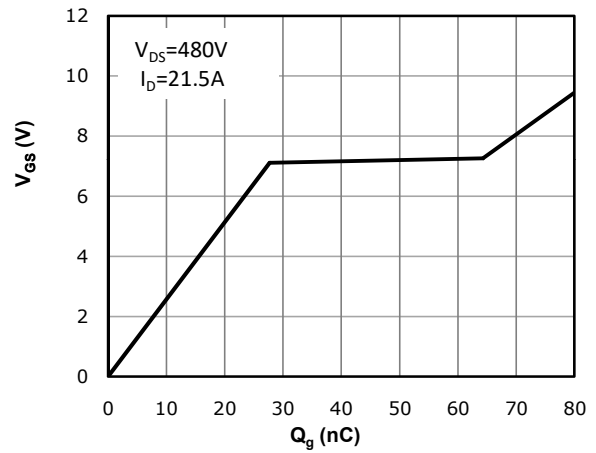


Fig 11: Capacitance Characteristics

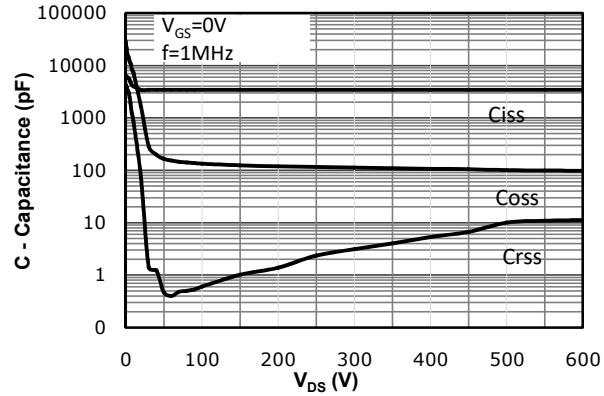
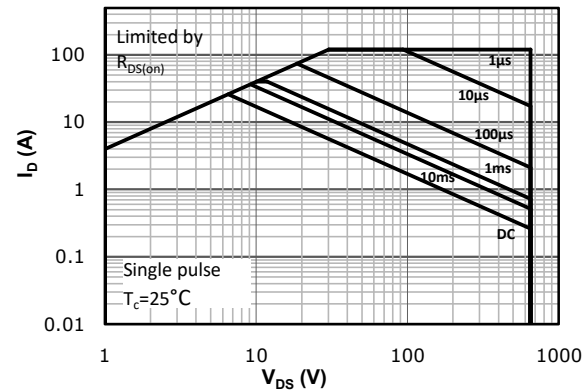
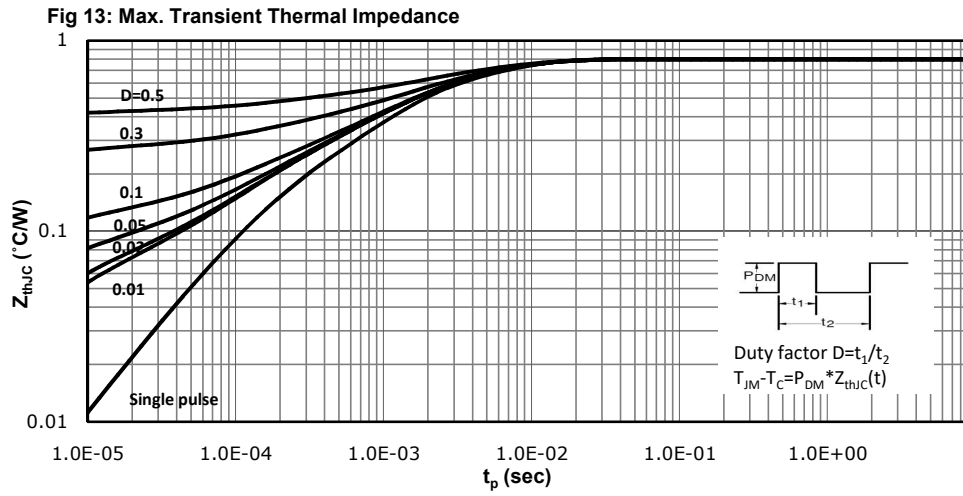


Fig 12: Safe Operating Area

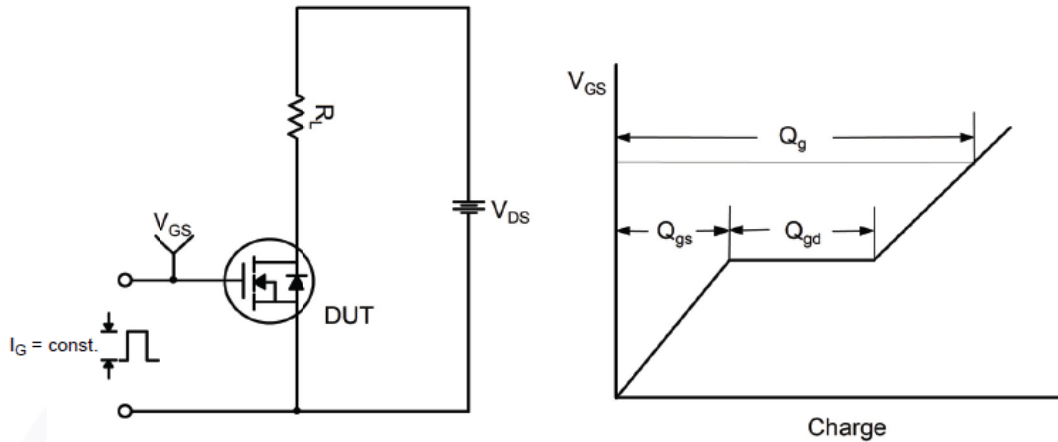




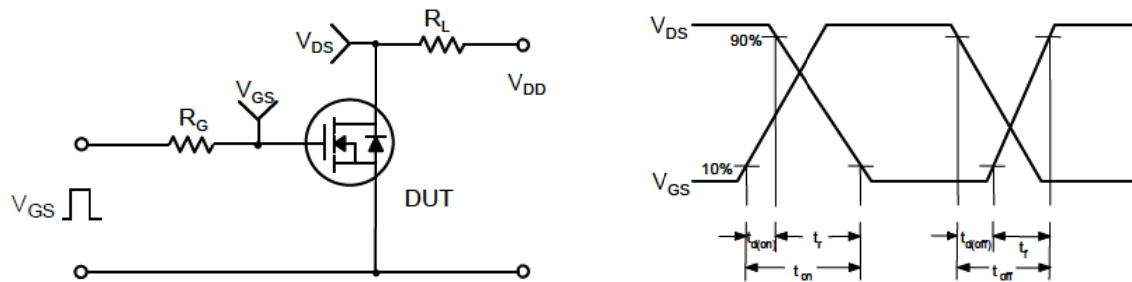


Test Circuit Schematic

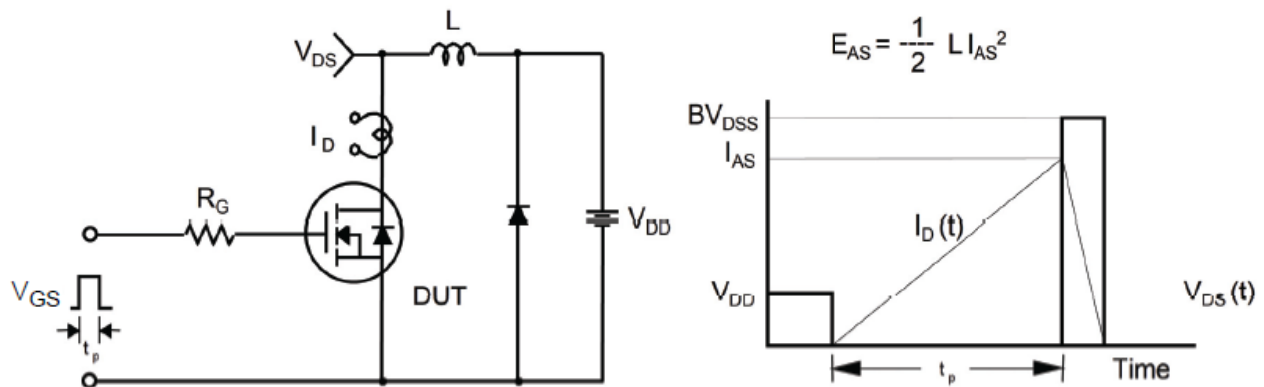
Gate Charge Test Circuit & Waveform



Switching Test Circuit & Waveforms



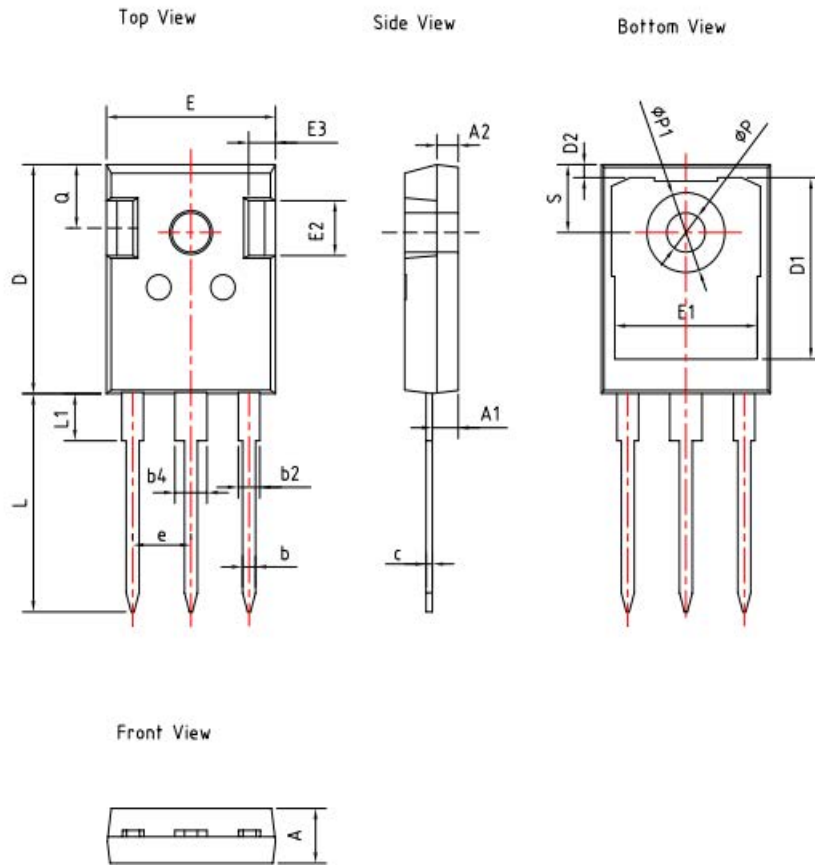
Unclamped Inductive Switching Test Circuit & Waveforms





Package Dimensions

Package TO-247



Dimension unit:[mm]			
SYMBOL	MIN	NOM	MAX
A	4.80	5.00	5.20
A1	2.21	2.41	2.61
A2	1.85	2.00	2.15
b	1.11	1.21	1.36
b2	1.91	2.01	2.21
b4	2.91	3.01	3.21
c	0.51	0.60	0.75
D	20.70	21.00	21.30
D1	16.25	16.55	16.85
D2	1.00	1.20	1.35
E	15.50	15.80	16.10
E1	13.00	13.30	13.60
E2	4.80	5.00	5.20
E3	2.30	2.50	2.70
e	5.44 BSC		
L	19.62	19.92	20.22
L1	-	-	4.30
φP	3.40	3.60	3.80
φP1	-	-	7.30
Q	5.40	5.80	6.20
S	6.20 BSC		



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