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Thank you for your cooperation and understanding,

Ampleon

UHF power LDMOS transistor

BLF647

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on underside eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (HF to 800 MHz)
- Internal input damping for excellent stability over the whole frequency range.

APPLICATIONS

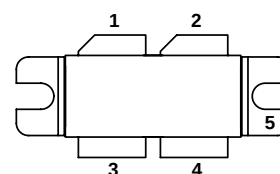
- Communication transmitter applications in the HF to 800 MHz frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS push-pull transistor in a SOT540A package with ceramic cap. The common source is connected to the mounting flange.

PINNING - SOT540A

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source, connected to flange



Top view

MBK777

Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at $T_h = 25^\circ\text{C}$ in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB	600	28	120	>14.5	>55	–
2-tone, class-AB	$f_1 = 600; f_2 = 600.1$	28	120 (PEP)	>14.5	>40	≤ -26

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
V_{GS}	gate-source voltage		–	± 15	V
I_D	drain current (DC)		–	18	A
P_{tot}	total power dissipation	$T_{mb} \leq 25^\circ\text{C}$	–	290	W
T_{stg}	storage temperature		–65	+150	$^\circ\text{C}$
T_j	junction temperature		–	200	$^\circ\text{C}$

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-mb}$	thermal resistance from junction to mounting base	$T_{mb} = 25\text{ }^{\circ}\text{C}$; $P_{tot} = 290\text{ W}$	0.6	K/W
$R_{th\ mb-h}$	thermal resistance from mounting base to heatsink		0.2	K/W

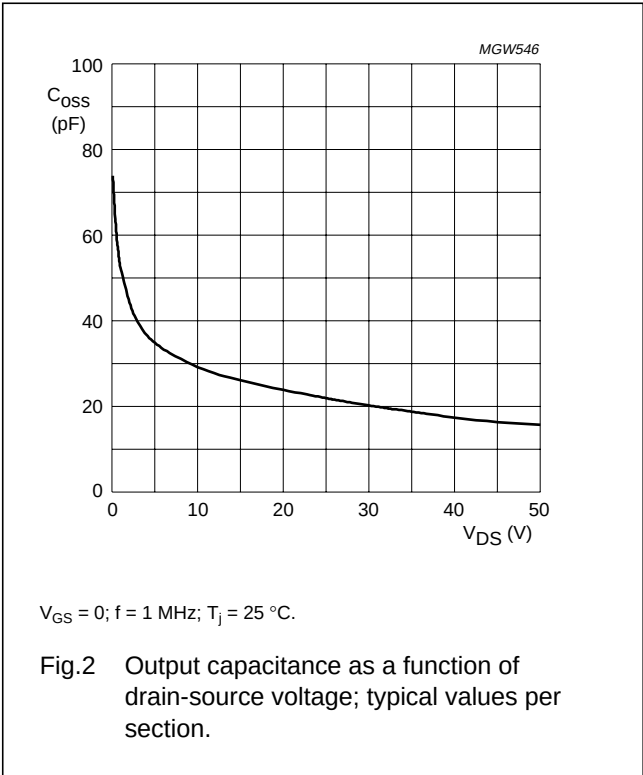
CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ per section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 1.4\text{ mA}$	65	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = 20\text{ V}$; $I_D = 140\text{ mA}$	4	–	5.5	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 28\text{ V}$	–	–	1.2	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GSth} + 9\text{ V}$; $V_{DS} = 10\text{ V}$	18	–	–	A
I_{GSS}	gate leakage current	$V_{GS} = \pm 15\text{ V}$; $V_{DS} = 0$	–	–	25	nA
g_{fs}	forward transconductance	$V_{DS} = 20\text{ V}$; $I_D = 4\text{ A}$	–	4	–	S
R_{DSon}	drain-source on-state resistance	$V_{GS} = V_{GSth} + 9\text{ V}$; $I_D = 4\text{ A}$	–	160	–	$\text{m}\Omega$
C_{iss}	input capacitance	$V_{GS} = 0$; $V_{DS} = 28\text{ V}$; $f = 1\text{ MHz}$; note 1	–	80	–	pF
C_{oss}	output capacitance	$V_{GS} = 0$; $V_{DS} = 28\text{ V}$; $f = 1\text{ MHz}$	–	43	–	pF
C_{rss}	feedback capacitance	$V_{GS} = 0$; $V_{DS} = 28\text{ V}$; $f = 1\text{ MHz}$	–	6	–	pF

Note

1. Capacitance values of the die only.



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APPLICATION INFORMATION

RF performance in a common source class-AB circuit. $T_h = 25\text{ }^{\circ}\text{C}$; $R_{th\text{ mb-h}} = 0.2\text{ K/W}$, unless otherwise specified.

MODE OF OPERATION	f (MHz)	V _{DS} (V)	P _L (W)	G _p (dB)	η_D (%)	d _{im} (dBc)
CW, class-AB	600	28	120	>14.5	>55	–
2-tone, class-AB	$f_1 = 600$; $f_2 = 600.1$	28	120 (PEP)	>14.5	>40	≤ -26
CW, class-AB	800	32	150	typ. 12.5	typ. 60	–
2-tone, class-AB	$f_1 = 800$; $f_2 = 800.1$	32	150 (PEP)	typ. 13	typ. 45	typ. –30

Ruggedness in class-AB operation

The BLF647 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 28\text{ V}$; $f = 100\text{ MHz}$ at rated load power.

The BLF647 is capable of withstanding abrupt source or load mismatch errors under the nominal power conditions.

Impedances (per section)

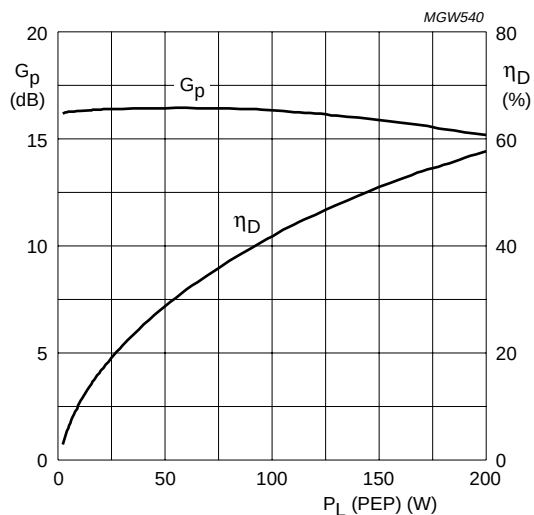
At $f = 600\text{ MHz}$, $P_L = 120\text{ W}$, $V_{DS} = 28\text{ V}$ and $I_{DQ} = 1\text{ A}$: $Z_{in} = 1.0 + j2.0\text{ }\Omega$ and $Z_L = 2.7 + j0.7\text{ }\Omega$.

At $f = 800\text{ MHz}$, $P_L = 150\text{ W}$, $V_{DS} = 32\text{ V}$ and $I_{DQ} = 1\text{ A}$: $Z_{in} = 1.0 + j3.8\text{ }\Omega$ and $Z_L = 1.8 + j0.7\text{ }\Omega$.

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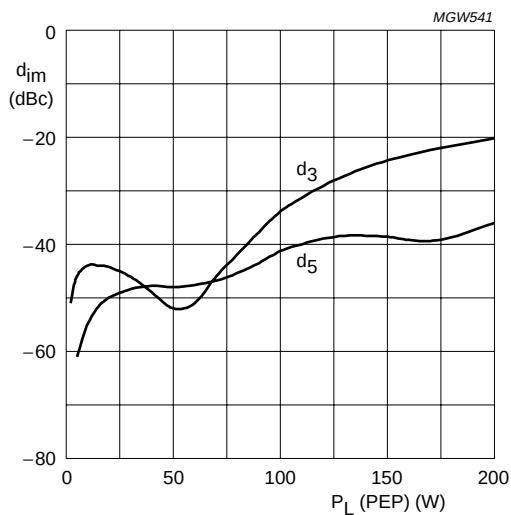
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Application at 600 MHz



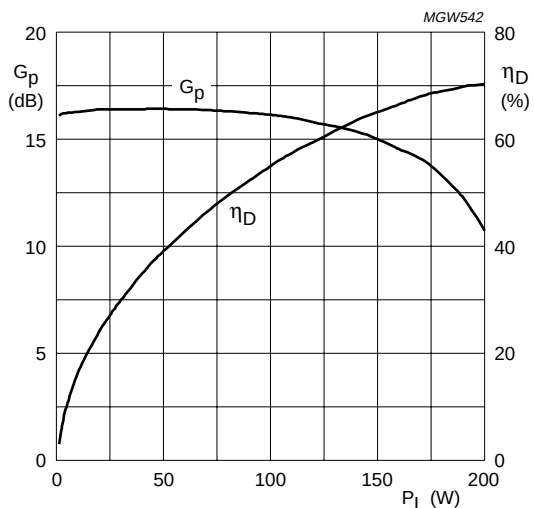
$T_h = 25\text{ }^\circ\text{C}$; $V_{DS} = 28\text{ V}$; $I_{DQ} = 1\text{ A}$.
 2-tone: $f_1 = 600\text{ MHz}$ (−6 dB); $f_2 = 600.1\text{ MHz}$ (−6 dB)
 measured in 600 MHz test circuit.

Fig.3 Power gain and drain efficiency as functions of peak envelope load power; typical values.



$T_h = 25\text{ }^\circ\text{C}$; $V_{DS} = 28\text{ V}$; $I_{DQ} = 1\text{ A}$.
 2-tone: $f_1 = 600\text{ MHz}$ (−6 dB); $f_2 = 600.1\text{ MHz}$ (−6 dB)
 measured in 600 MHz test circuit.

Fig.4 Intermodulation distortion as a function of peak envelope output power; typical values.



$T_h = 25\text{ }^\circ\text{C}$; $V_{DS} = 28\text{ V}$; $I_{DQ} = 1\text{ A}$; CW, class-AB; $f = 600\text{ MHz}$;
 measured in 600 MHz test circuit.

Fig.5 Power gain and drain efficiency as functions of load power; typical values.

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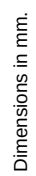


Fig.6 Class-AB common source 600 MHz test circuit.

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List of components class-AB 600 MHz test circuit (see Figs 6 and 7)

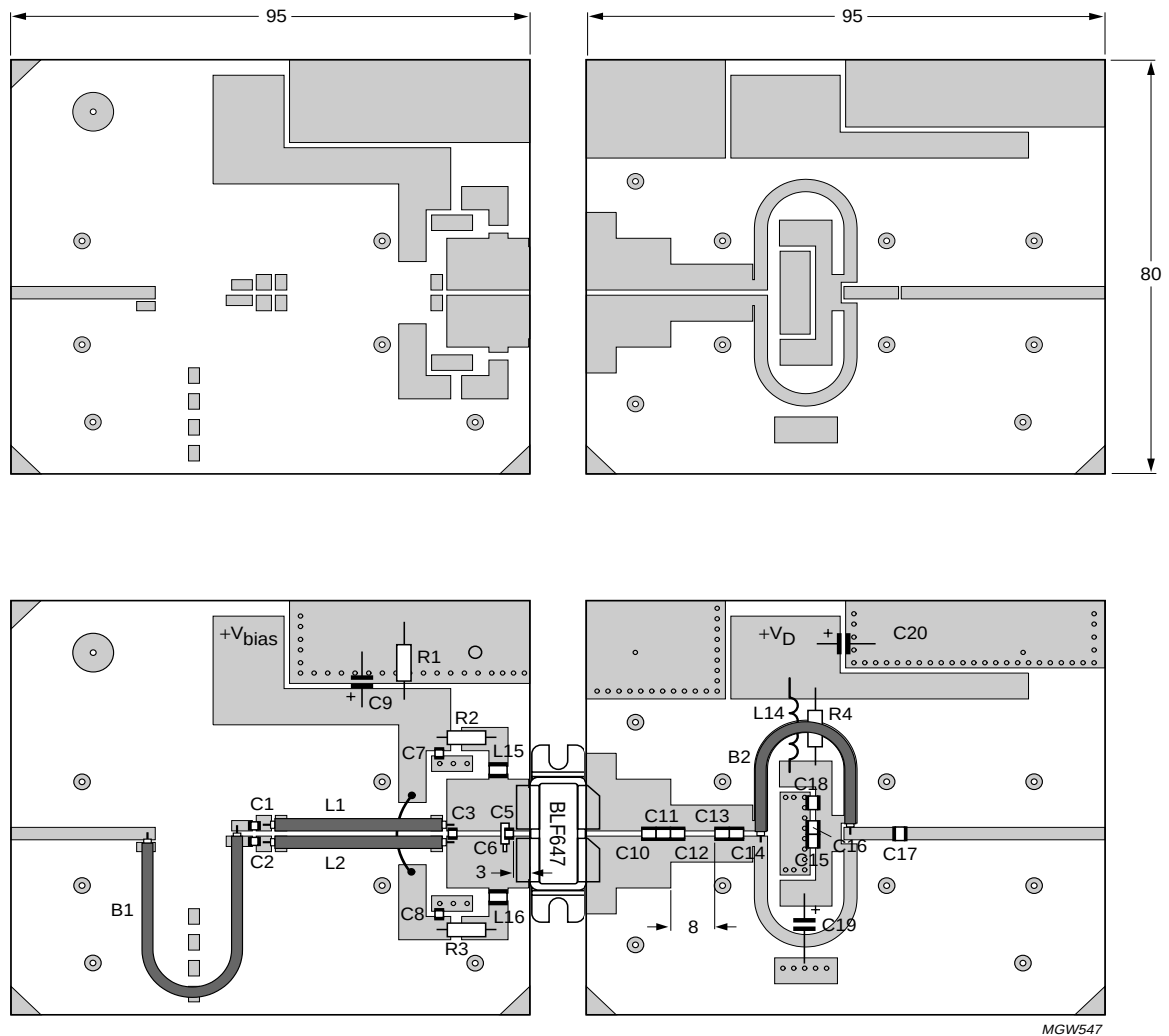
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C2	multilayer ceramic chip capacitor; note 1	30 pF		
C3	multilayer ceramic chip capacitor; note 1	8.2 pF		
C5	multilayer ceramic chip capacitor; note 1	16 pF		
C6	Tekelec trimmer	0.6 to 7.5 pF		
C7, C8	multilayer ceramic chip capacitor; note 1	100 pF		
C9	electrolytic capacitor	10 μ F		
C10	multilayer ceramic chip capacitor; note 2	2 pF		
C11, C12	multilayer ceramic chip capacitor; note 2	10 pF		
C13	multilayer ceramic chip capacitor; note 2	8.2 pF		
C14	multilayer ceramic chip capacitor; note 2	1.5 pF		
C15, C16, C17	multilayer ceramic chip capacitor; note 2	100 pF		
C18	SMD capacitor	1 μ F		2222 595 16754
C19	electrolytic capacitor	470 μ F		
C20	electrolytic capacitor	100 μ F		
L1, L2	semi rigid coax UT70-25	$Z = 25 \Omega \pm 1.5 \Omega$	30.6 mm	
L3, L4	stripline; note 3		15 $\times$ 10 mm	
L5, L6	stripline; note 3		5.5 $\times$ 15 mm	
L7, L8	stripline; note 3		10 $\times$ 10 mm	
L9, L10	stripline; note 3		15 $\times$ 5 mm	
L11, L12	stripline; note 3		48.5 $\times$ 2.4 mm	
L13	stripline; note 3		10 $\times$ 2.4 mm	
L14	ferrite			
L15, L16	Coilcraft SMD coil 1008CS-102XKBC	1 μ H		
B1	semi rigid coax ($\lambda/2$)	$Z = 50 \Omega \pm 1.5 \Omega$	$\lambda/2$	
B2	semi rigid coax balun UT70-25	$Z = 25 \Omega \pm 1.5 \Omega$	48.5 mm	
R1	resistor	1 k Ω		
R2, R3	resistor	100 Ω		
R4	resistor	3,3 Ω		

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 180R or capacitor of same quality.
3. The striplines are on a double copper-clad printed-circuit board: Rogers 5880 ($\epsilon_r = 2.2$); thickness 0.79 mm.

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MGW547

Dimensions in mm.

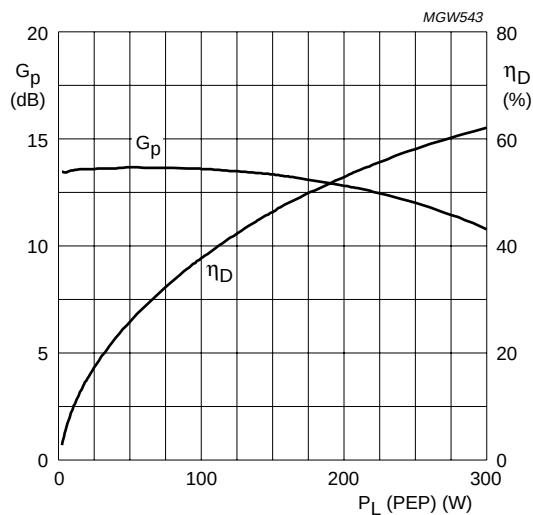
The components are situated on one side of the Rogers 5880 printed-circuit board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

Fig.7 Printed-circuit board and component layout for class-AB 600 MHz test circuit.

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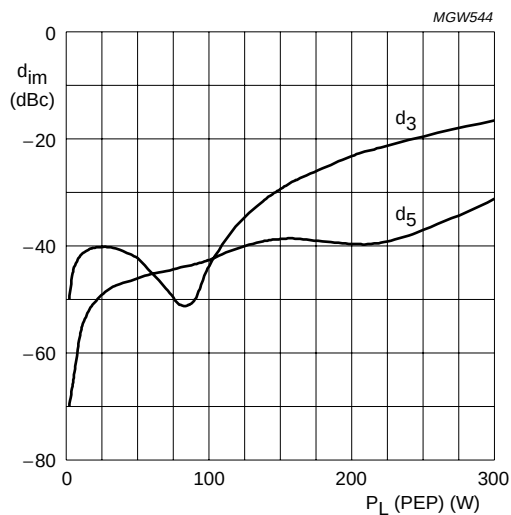
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Application at 800 MHz



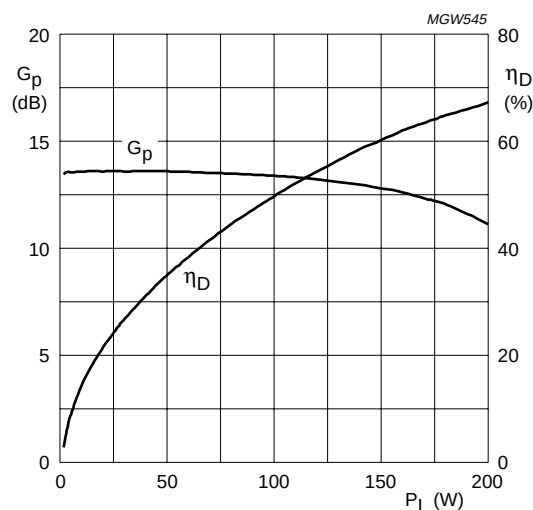
$T_h = 25\text{ }^{\circ}\text{C}$; $V_{DS} = 32\text{ V}$; $I_{DQ} = 1\text{ A}$.
 2-tone: $f_1 = 800\text{ MHz}$ (-6 dB); $f_2 = 800.1\text{ MHz}$ (-6 dB)
 measured in 800 MHz test circuit.

Fig.8 Power gain and drain efficiency as functions of peak envelope load power; typical values.



$T_h = 25\text{ }^{\circ}\text{C}$; $V_{DS} = 32\text{ V}$; $I_{DQ} = 1\text{ A}$.
 2-tone: $f_1 = 800\text{ MHz}$ (-6 dB); $f_2 = 800.1\text{ MHz}$ (-6 dB)
 measured in 800 MHz test circuit.

Fig.9 Intermodulation distortion as a function of peak envelope output power; typical values.



$T_h = 25\text{ }^{\circ}\text{C}$; $V_{DS} = 32\text{ V}$; $I_{DQ} = 1\text{ A}$; CW, class-AB; $f = 800\text{ MHz}$;
 measured in 800 MHz test circuit.

Fig.10 Power gain and drain efficiency as functions of load power; typical values.

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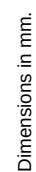


Fig.11 Class-AB common source 800 MHz test circuit.

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List of components class-AB 800 MHz test circuit (see Figs 11 and 12)

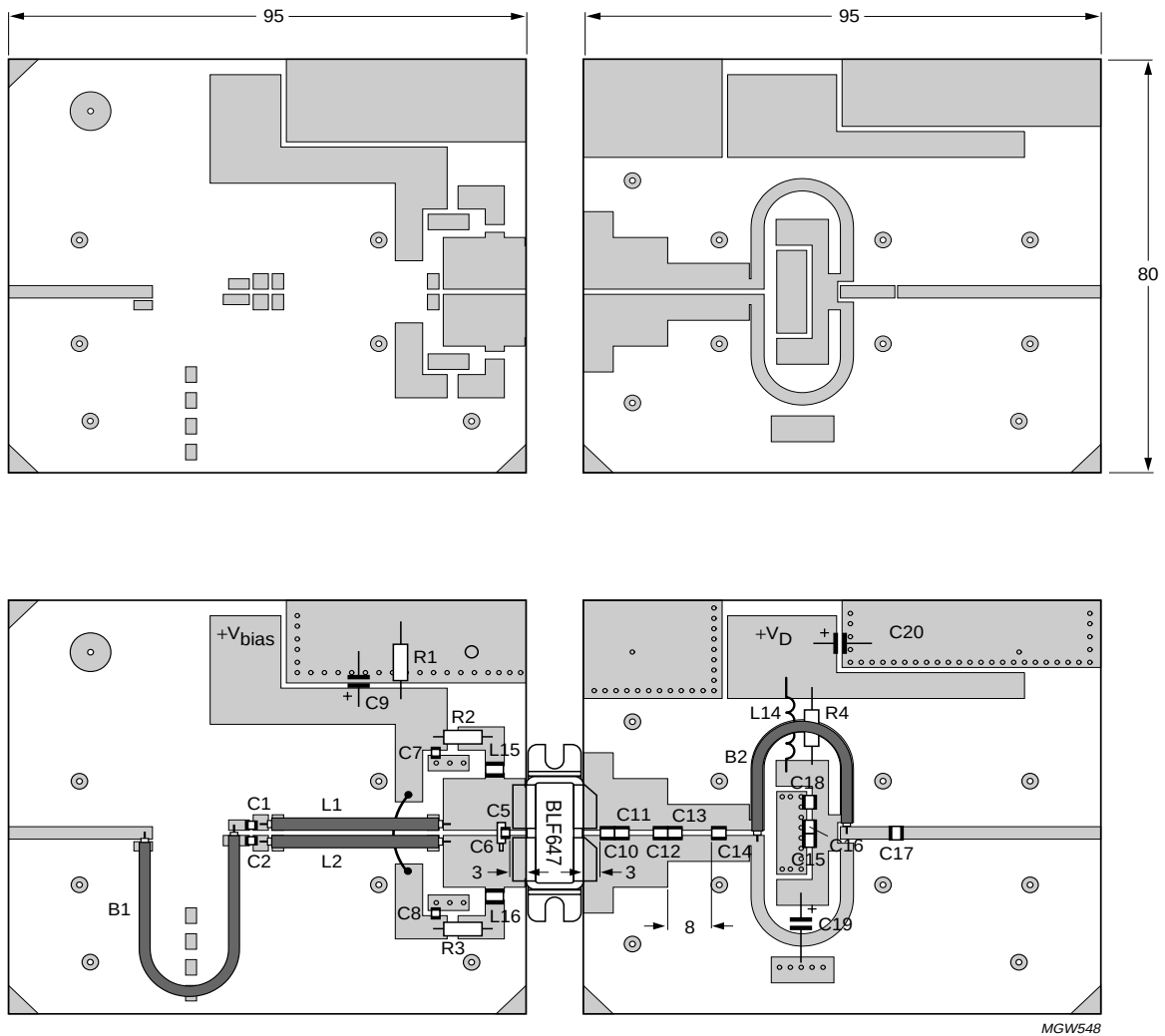
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C2	multilayer ceramic chip capacitor; note 1	30 pF		
C5	multilayer ceramic chip capacitor; note 1	10 pF		
C6	tekelec trimmer	0.6 to 7.5 pF		
C7, C8	multilayer ceramic chip capacitor; note 1	100 pF		
C9	electrolytic capacitor	10 μ F		
C10, C11	multilayer ceramic chip capacitor; note 2	8.2 pF		
C12, C13	multilayer ceramic chip capacitor; note 2	10 pF		
C14	multilayer ceramic chip capacitor; note 2	4.7 pF		
C15, C16	multilayer ceramic chip capacitor; note 2	100 pF		
C17	multilayer ceramic chip capacitor; note 2	20 pF		
C18	SMD capacitor	1 μ F		2222 595 16754
C19	electrolytic capacitor	470 μ F		
C20	electrolytic capacitor	100 μ F		
L1, L2	semi rigid coax UT70-25	$Z = 25 \Omega \pm 1.5 \Omega$	30.6 mm	
L3, L4	stripline; note 3		15 $\times$ 10 mm	
L5, L6	stripline; note 3		5.5 $\times$ 15 mm	
L7, L8	stripline; note 3		10 $\times$ 10 mm	
L9, L10	stripline; note 3		15 $\times$ 5 mm	
L11, L12	stripline; note 3		48.5 $\times$ 2.4 mm	
L13	stripline; note 3		10 $\times$ 2.4 mm	
L14	ferrite			
L15, L16	Coilcraft SMD coil 1008CS-102XKBC	1 μ H		
B1	semi rigid coax ($\lambda/2$)	$Z = 50 \Omega \pm 1.5 \Omega$	$\lambda/2$	
B2	semi rigid coax balun UT70-25	$Z = 25 \Omega \pm 1.5 \Omega$	48.5 mm	
R1	resistor	1 k Ω		
R2, R3	resistor	100 Ω		
R4	resistor	3,3 Ω		

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 180R or capacitor of same quality.
3. The striplines are on a double copper-clad printed-circuit board: Rogers 5880 ($\epsilon_r = 2.2$); thickness 0.79 mm.

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Dimensions in mm.

The components are situated on one side of the Rogers 5880 printed-circuit board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

Fig.12 Printed-circuit board and component layout for class-AB 800 MHz test circuit.

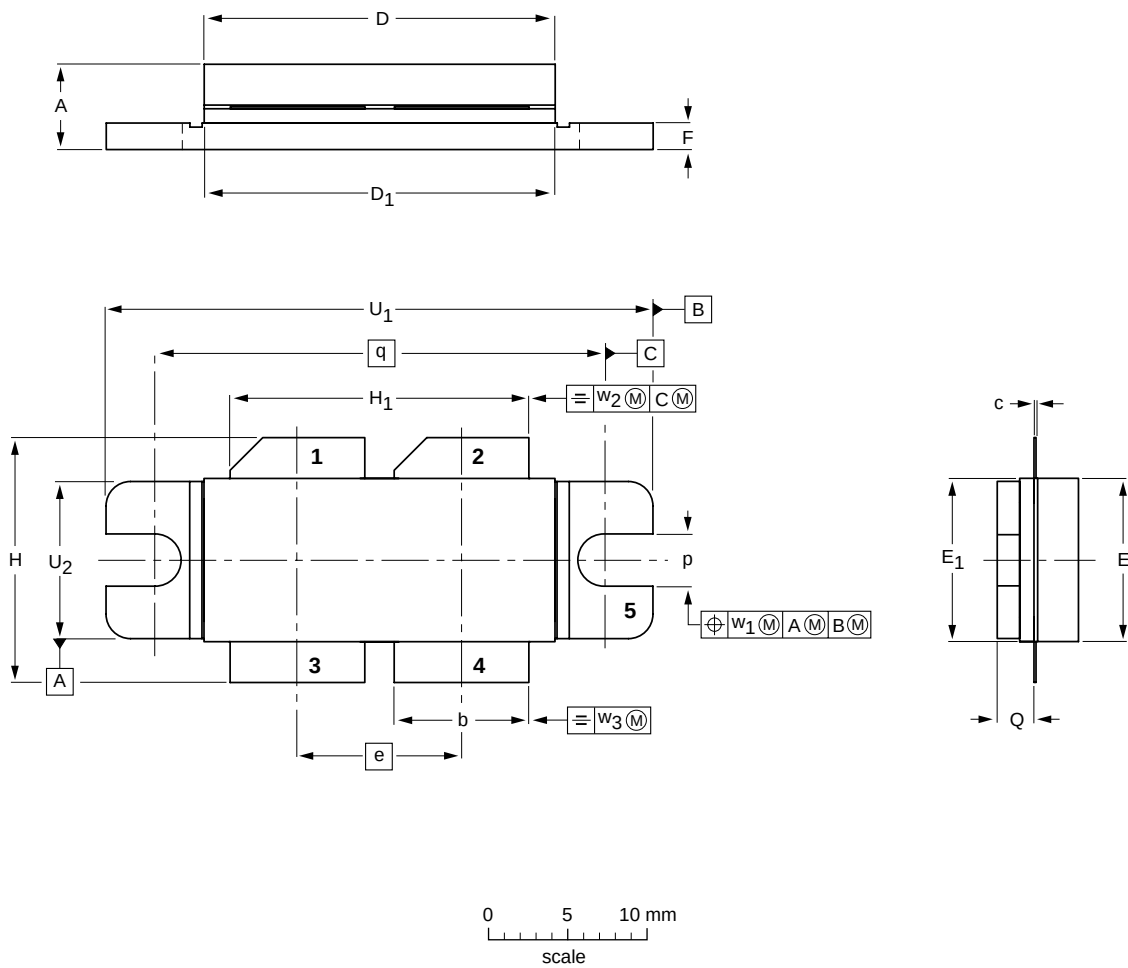
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PACKAGE OUTLINE

Flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads

SOT540A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	p	Q	q	U ₁	U ₂	w ₁	w ₂	w ₃
mm	5.77 5.00	8.51 8.26	0.15 0.10	22.05 21.64	22.05 21.64	10.21	10.26 10.06	10.31 10.01	1.78 1.52	15.75 14.73	18.72 18.47	3.38 3.12	2.72 2.46	27.94	34.16 33.91	9.91 9.65	0.25	0.51	0.25
inches	0.227 0.197	0.335 0.325	0.006 0.004	0.868 0.852	0.868 0.852	0.402	0.404 0.396	0.406 0.394	0.070 0.060	0.620 0.580	0.737 0.727	0.133 0.123	0.107 0.097	1.100	1.345 1.335	0.390 0.380	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT540A						-99-08-27- 99-12-28

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DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contact information

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