

Description

The SX50N06NF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 60V$ $I_D = 50A$

$R_{DS(ON)} < 16m\Omega$ @ $V_{GS}=10V$

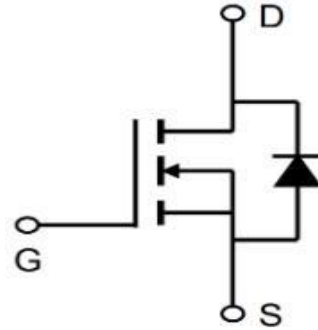
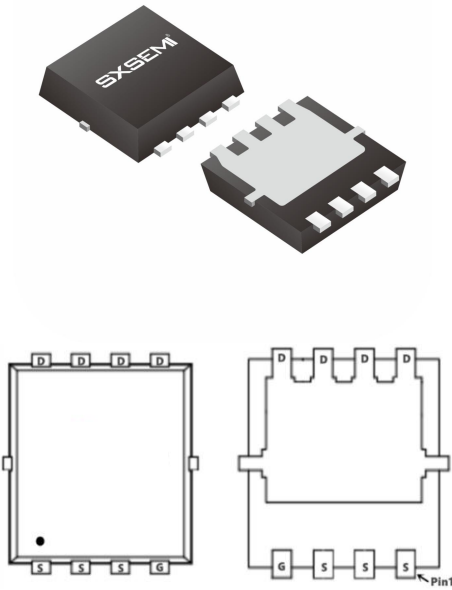
Application

Battery protection

Load switch

Uninterruptible power supply

PDFN5*6-8L



Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_c=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	50	A
$I_D @ T_c=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	25	A
$I_D @ T_A=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	7.4	A
$I_D @ T_A=70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	6	A
I_{DM}	Pulsed Drain Current ²	90	A
E_{AS}	Single Pulse Avalanche Energy ³	39.2	mJ
I_{AS}	Avalanche Current	28	A
$P_D @ T_c=25^\circ\text{C}$	Total Power Dissipation ⁴	45	W
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation ⁴	2	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	62	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	2.8	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250uA	60	65	---	V
ΔBVDSS/ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C , I _D =1mA	---	0.057	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance ²	V _{GS} =10V , I _D =20A	---	11.5	16	mΩ
		V _{GS} =4.5V , I _D =10A	---	16.3	20	
VGS(th)	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.2	1.8	2.5	V
ΔVGS(th)	VGS(th) Temperature Coefficient		---	-5.68	---	mV/°C
IDSS	Drain-Source Leakage Current	V _{DS} =48V , V _{GS} =0V , T _J =25°C	---	---	1	uA
		V _{DS} =48V , V _{GS} =0V , T _J =55°C	---	---	5	
IGSS	Gate-Source Leakage Current	V _{GS} =±20V , V _{DS} =0V	---	---	±100	nA
gfs	Forward Transconductance	V _{DS} =5V , I _D =15A	---	45	---	S
R _g	Gate Resistance	V _{DS} =0V , V _{GS} =0V , f=1MHz	---	1.7	---	Ω
Q _g	Total Gate Charge (4.5V)	V _{DS} =48V , V _{GS} =4.5V , I _D =15A	---	19.3	---	nC
Q _{gs}	Gate-Source Charge		---	7.1	---	
Q _{gd}	Gate-Drain Charge		---	7.6	---	
Td(on)	Turn-On Delay Time	V _{DD} =30V , V _{GS} =10V , R _G =3.3Ω , I _D =15A	---	7.2	---	ns
T _r	Rise Time		---	50	---	
Td(off)	Turn-Off Delay Time		---	36.4	---	
T _f	Fall Time		---	7.6	---	
C _{iss}	Input Capacitance	V _{DS} =15V , V _{GS} =0V , f=1MHz	---	2423	---	pF
C _{oss}	Output Capacitance		---	145	---	
Crss	Reverse Transfer Capacitance		---	97	---	
I _s	Continuous Source Current ^{1,5}	V _G =V _D =0V , Force Current	---	---	35	A
ISM	Pulsed Source Current ^{2,5}		---	---	80	A
VSD	Diode Forward Voltage ²	V _{GS} =0V , I _s =A , T _J =25°C	---	---	1	V
t _{rr}	Reverse Recovery Time	IF=15A, dI/dt=100A/μs , T _J =25°C	---	16.3	---	nS
Q _{rr}	Reverse Recovery Charge		---	11	---	nC

Note :

- 1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、The EAS data shows Max. rating . The test condition is VDD=25V,VGS=10V,L=0.1mH,IAS=28A
- 4、The power dissipation is limited by 150°C junction temperature 5.The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation

Typical Characteristics

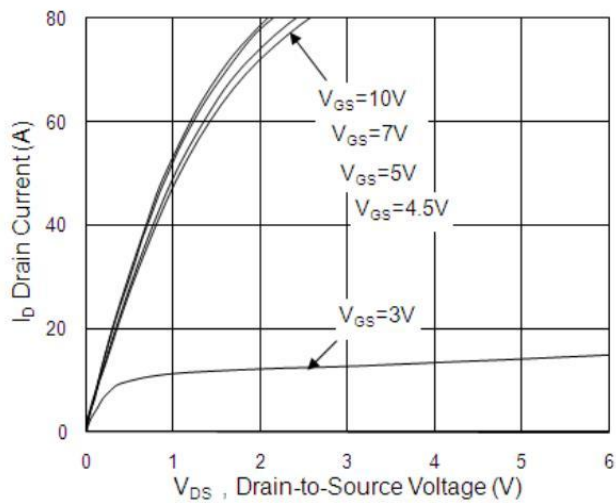


Fig.1 Typical Output Characteristics

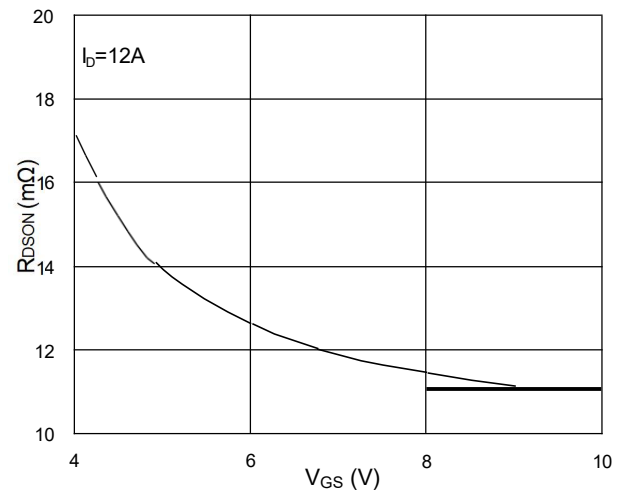


Fig.2 On-Resistance v.s Gate-Source

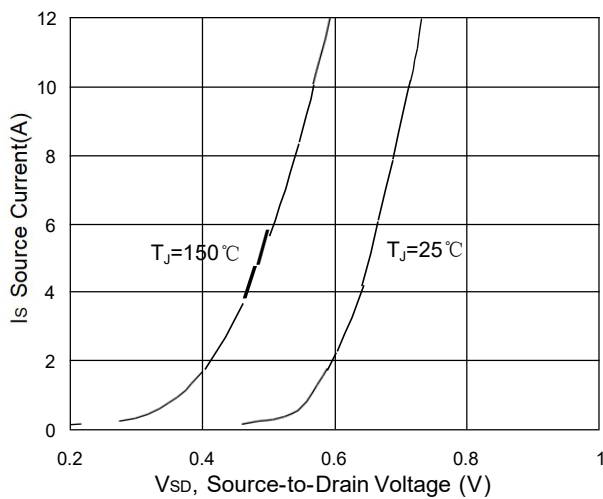


Fig.3 Forward Characteristics of Reverse

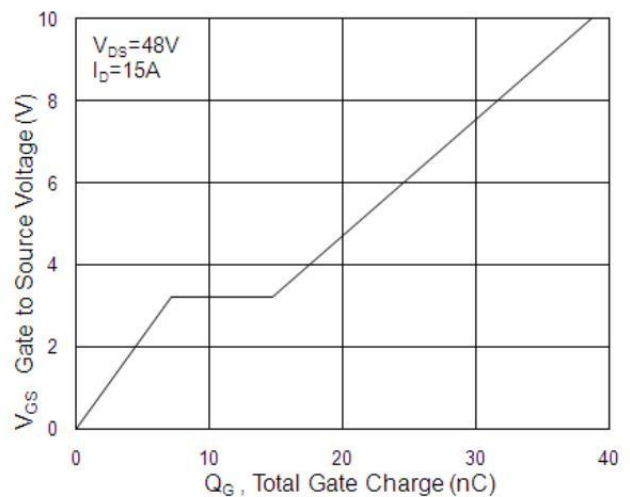


Fig.4 Gate-Charge Characteristics

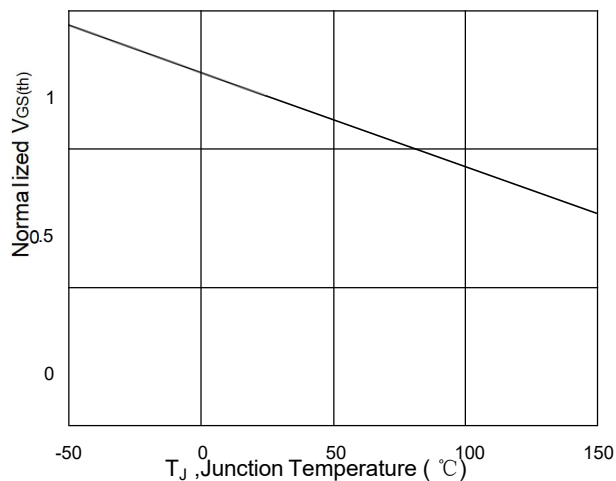


Fig.5 Normalized V_{GS} v.s T_J

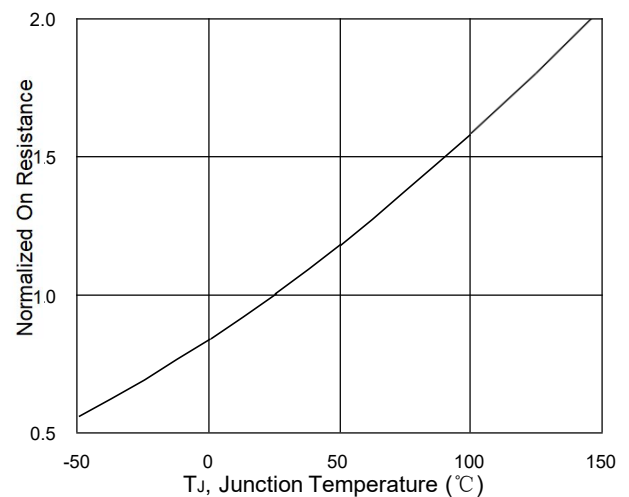


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

Typical Characteristics

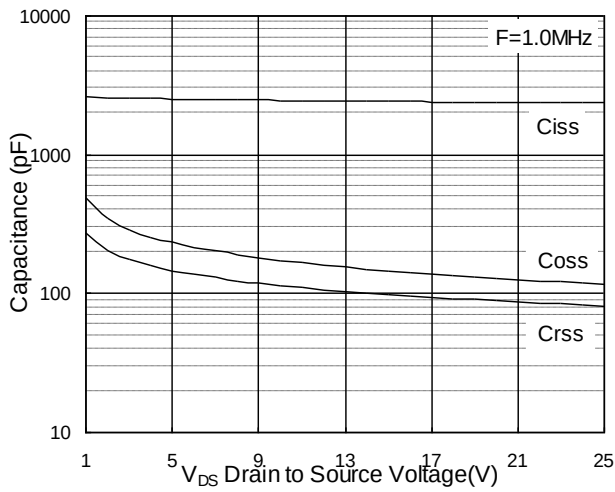


Fig.7 Capacitance

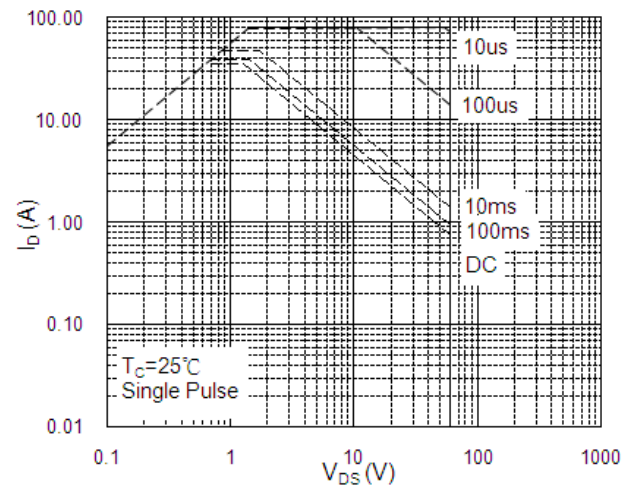


Fig.8 Safe Operating Area

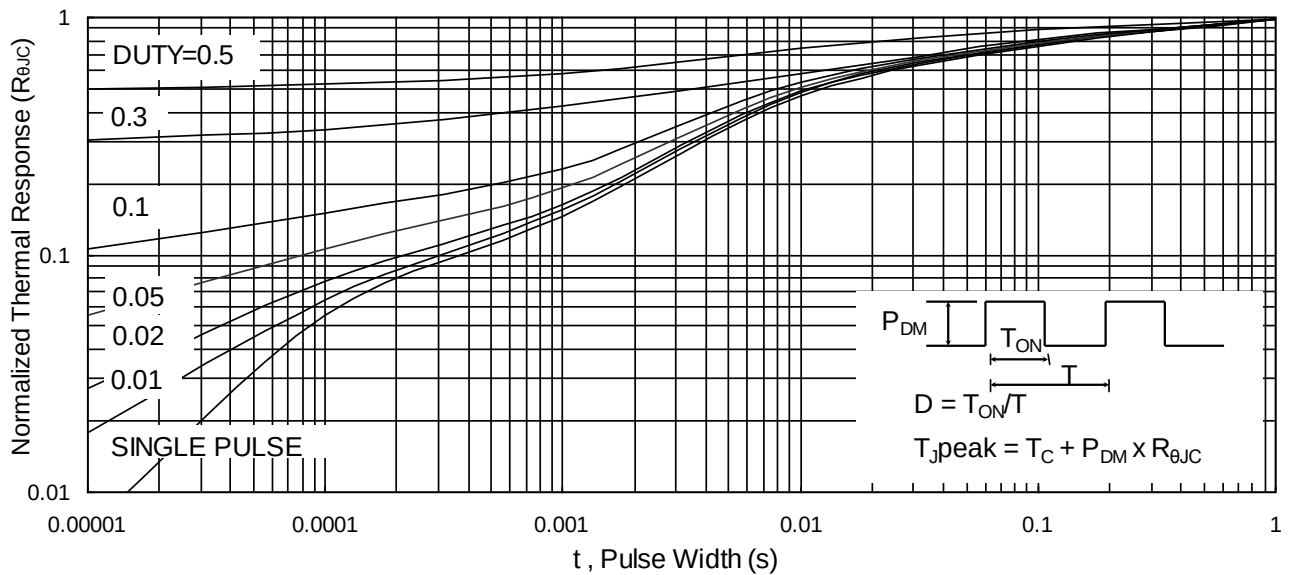


Fig.9 Normalized Maximum Transient Thermal Impedance

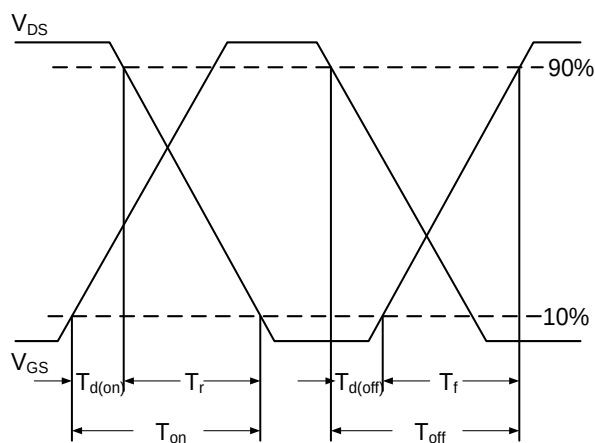


Fig.10 Switching Time Waveform

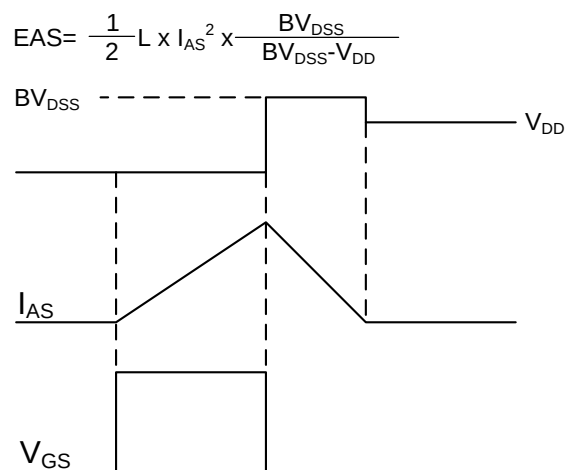
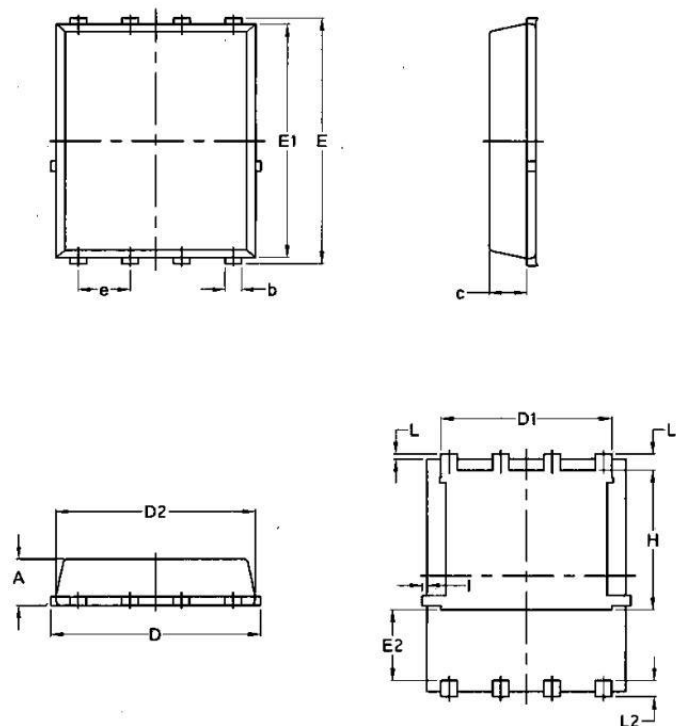


Fig.11 Unclamped Inductive Switching Waveform

MOSFET Package Mechanical Data- PDFN5*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
TAPING	PDFN5*6-8L		5000