

General Description

The AOD603A uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications.

Product Summary

N-Channel

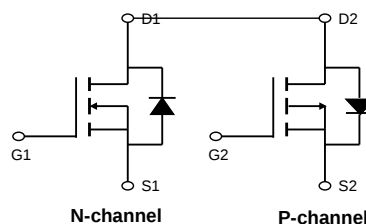
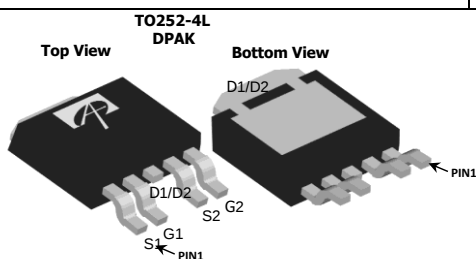
$V_{DS} = 60V$
 $I_D = 13A$ ($V_{GS}=10V$, silicon limit)
 $R_{DS(ON)}$
 $< 60m\Omega$ ($V_{GS}=10V$)
 $< 85m\Omega$ ($V_{GS}=4.5V$)

100% UIS Tested
 100% R_g Tested

P-Channel

$-60V$
 $-13A$ ($V_{GS}=-10V$, silicon limit)
 $R_{DS(ON)}$
 $< 115m\Omega$ ($V_{GS}=-10V$)
 $< 150m\Omega$ ($V_{GS}=-4.5V$)

100% UIS Tested
 100% R_g Tested



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Max N-channel	Max P-channel	Units
Drain-Source Voltage	V_{DS}	60	-60	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current	$T_C=25^\circ C$ (silicon limit)	13.6	-13.4	A
	$T_C=25^\circ C^G$	12	-12	
	$T_C=100^\circ C$	9.5	-9.5	
Pulsed Drain Current ^C	I_{DM}	30	-30	
Continuous Drain Current	$T_A=25^\circ C$	3.5	-3	A
	$T_A=70^\circ C$	3	-2.5	
Avalanche Current ^C	I_{AS}, I_{AR}	19	25	A
Avalanche energy $L=0.1mH$ ^C	E_{AS}, E_{AR}	18	31	mJ
Power Dissipation ^B	$T_C=25^\circ C$	27	42.5	W
	$T_C=100^\circ C$	13.5	21.5	
Power Dissipation ^A	$T_A=25^\circ C$	2	2	W
	$T_A=70^\circ C$	1.3	1.3	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	-55 to 175	$^\circ C$

Thermal Characteristics

Parameter N-channel		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$t \leq 10s$	$R_{\theta JA}$	19	23	$^\circ C/W$
Maximum Junction-to-Ambient ^{A,D}	Steady-State		50	60	$^\circ C/W$
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	4	5.5	$^\circ C/W$
Parameter P-channel		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$t \leq 10s$	$R_{\theta JA}$	19	23	$^\circ C/W$
Maximum Junction-to-Ambient ^{A,D}	Steady-State		50	60	$^\circ C/W$
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	2.5	3.5	$^\circ C/W$

N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	60			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=60\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1	2.4	3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=12\text{A}$ $T_J=125^\circ\text{C}$		47 90	60 110	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=8\text{A}$		67	85	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=12\text{A}$		22		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.74	1	V
I_S	Maximum Body-Diode Continuous Current ^G				12	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=30\text{V}$, $f=1\text{MHz}$		450		pF
C_{oss}	Output Capacitance			61		pF
C_{rss}	Reverse Transfer Capacitance			27		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$	0.6	1.35	2	Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=30\text{V}$, $I_D=12\text{A}$		7.5	12	nC
$Q_g(4.5\text{V})$	Total Gate Charge			3.8	7	nC
Q_{gs}	Gate Source Charge			1.2		nC
Q_{gd}	Gate Drain Charge			1.9		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$, $V_{DS}=30\text{V}$, $R_L=2.5\Omega$, $R_{GEN}=3\Omega$		4.2		ns
t_r	Turn-On Rise Time			3.4		ns
$t_{D(off)}$	Turn-Off DelayTime			16		ns
t_f	Turn-Off Fall Time			2		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=12\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		27		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=12\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		30		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}=175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=175^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}=175^\circ\text{C}$. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$.

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N-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

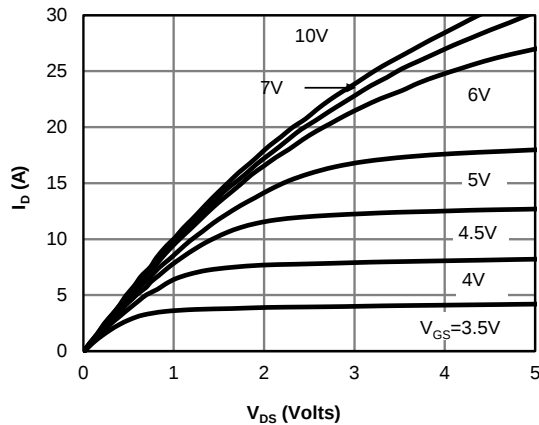


Fig 1: On-Region Characteristics (Note E)

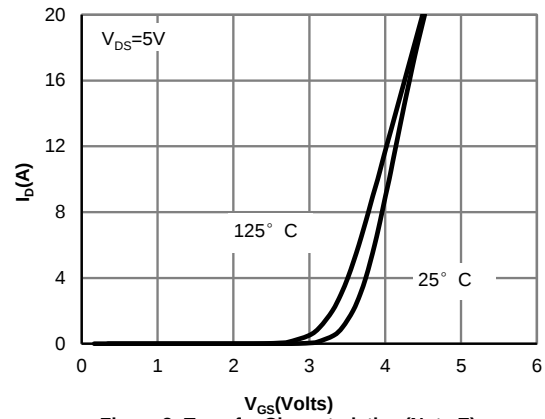


Figure 2: Transfer Characteristics (Note E)

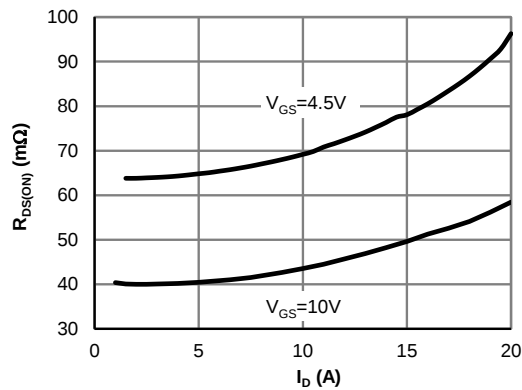


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

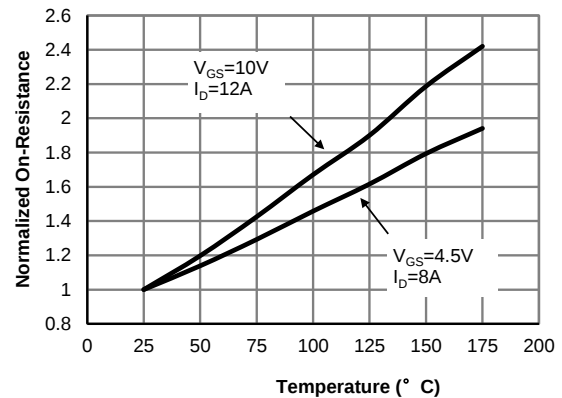


Figure 4: On-Resistance vs. Junction Temperature (Note E)

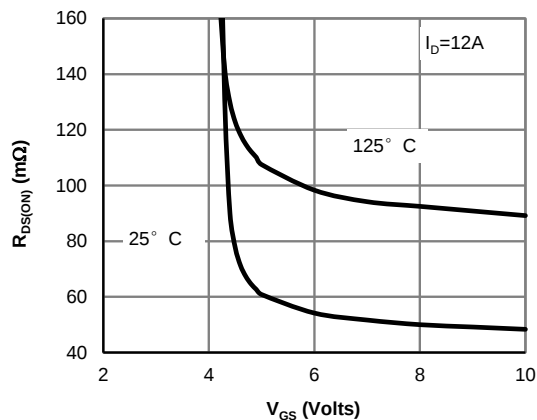


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

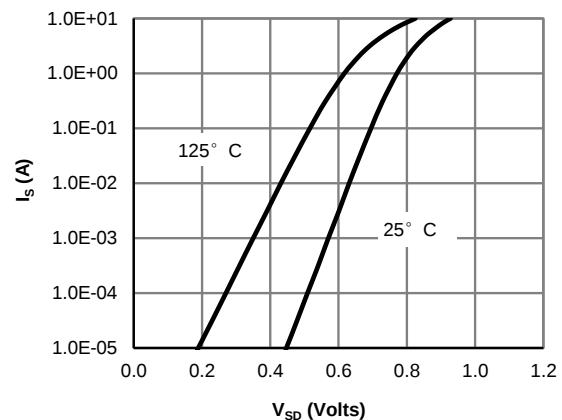


Figure 6: Body-Diode Characteristics (Note E)

N-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

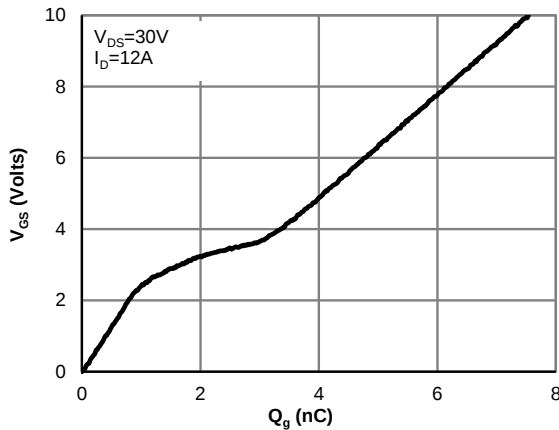


Figure 7: Gate-Charge Characteristics

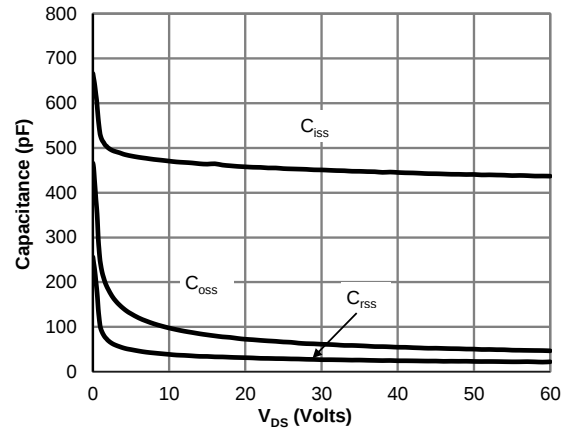


Figure 8: Capacitance Characteristics

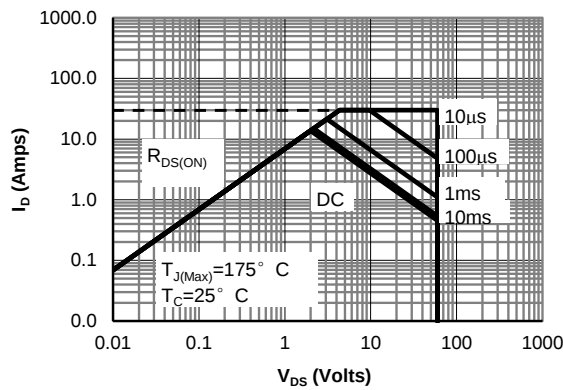


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

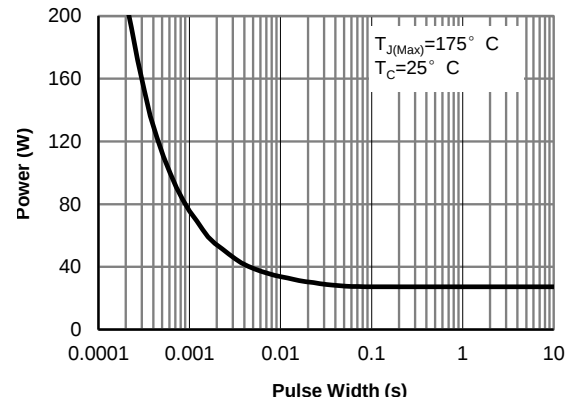


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

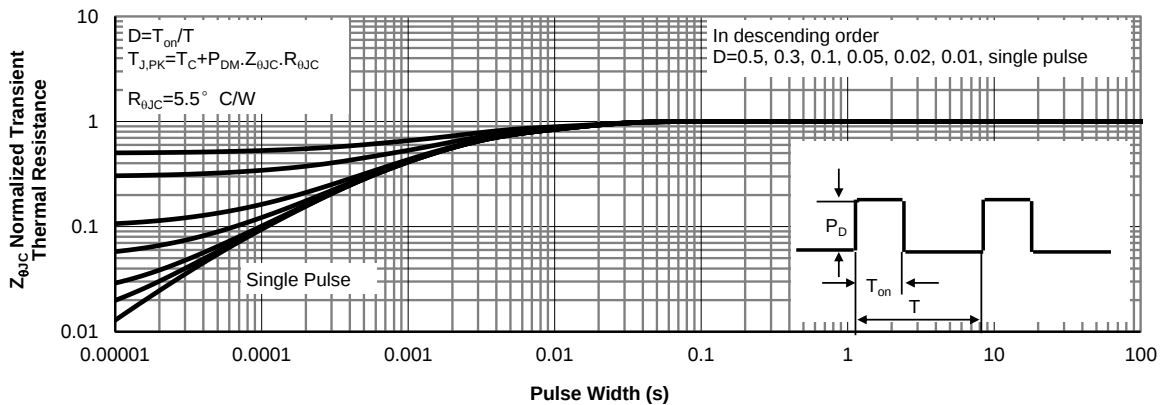


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

N-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

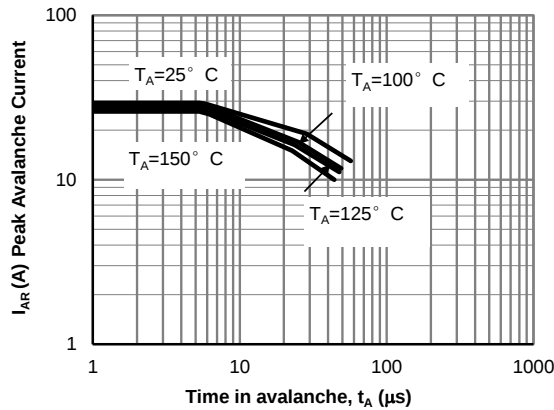


Figure 12: Single Pulse Avalanche capability (Note C)

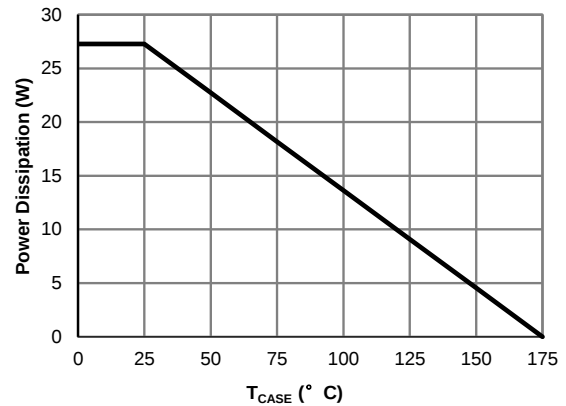


Figure 13: Power De-rating (Note F)

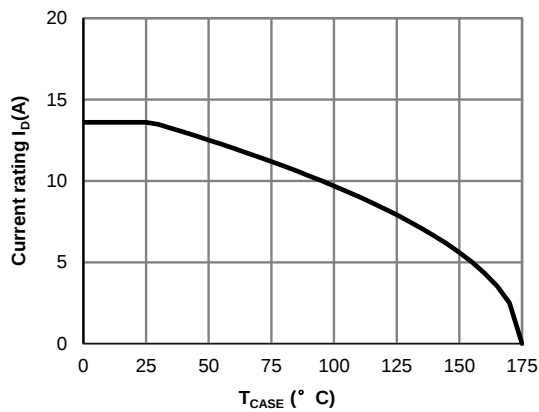


Figure 14: Current De-rating (Note F)

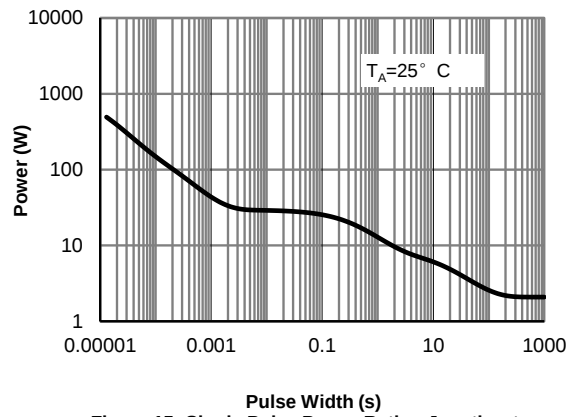


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

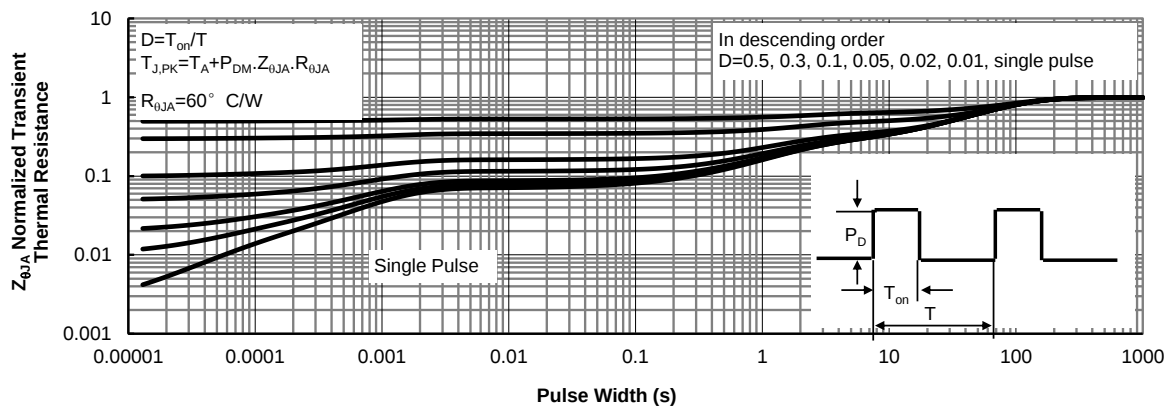
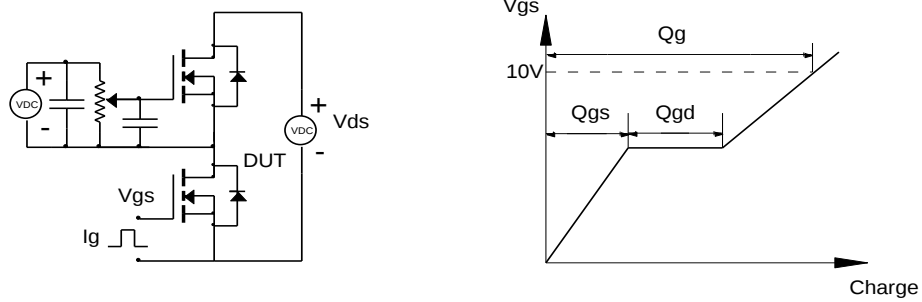
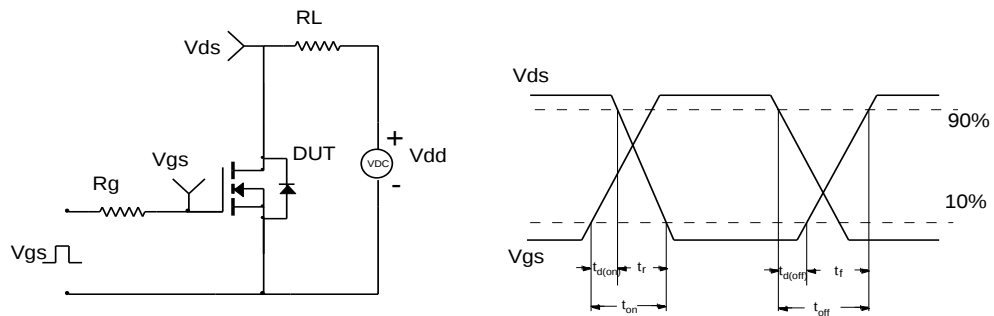


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

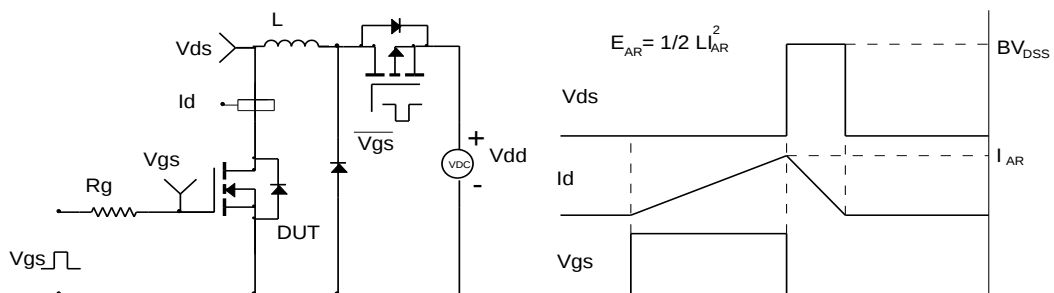
Gate Charge Test Circuit & Waveform



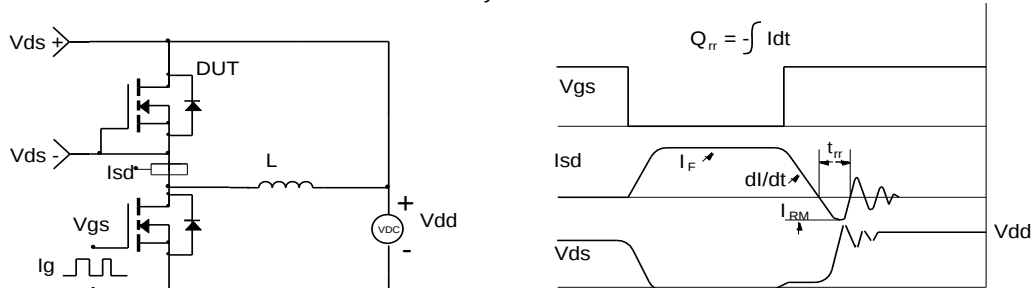
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



P-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-60			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-60V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.5	-2.1	-3	V
I _{D(ON)}	On state drain current	V _{GS} =-10V, V _{DS} =-5V	-30			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-12A T _J =125°C		91	115	mΩ
		V _{GS} =-4.5V, I _D =-8A		150	180	mΩ
				114	150	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-12A		12		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.76	-1	V
I _S	Maximum Body-Diode Continuous Current ^G				-12	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-30V, f=1MHz		960		pF
C _{oss}	Output Capacitance			86		pF
C _{rss}	Reverse Transfer Capacitance			38		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		9.5	15	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =-10V, V _{DS} =-30V, I _D =-12A		15.8	22	nC
Q _{g(4.5V)}	Total Gate Charge			7.4	12	nC
Q _{gs}	Gate Source Charge			3		nC
Q _{gd}	Gate Drain Charge			3.5		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-30V, R _L =2.5Ω, R _{GEN} =3Ω		9		ns
t _r	Turn-On Rise Time			10		ns
t _{D(off)}	Turn-Off DelayTime			25		ns
t _f	Turn-Off Fall Time			11		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-12A, dI/dt=100A/μs		27.5		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-12A, dI/dt=100A/μs		30		nC

A. The value of R_{DS(on)} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{DS(on)} and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation P_D is based on T_{J(MAX)}=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{DS(on)} is the sum of the thermal impedance from junction to case R_{DSJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

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P-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

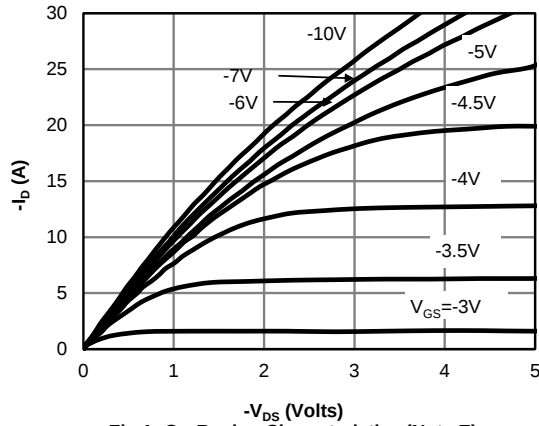


Fig 1: On-Region Characteristics (Note E)

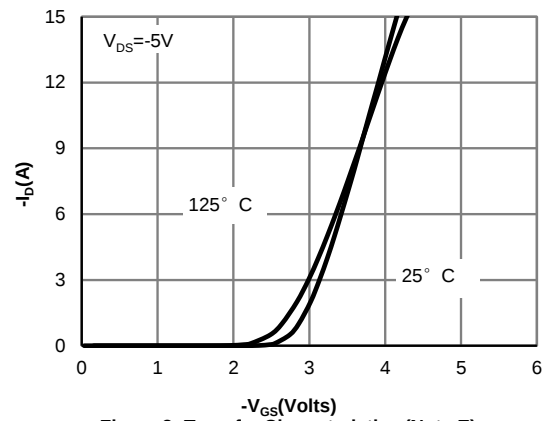


Figure 2: Transfer Characteristics (Note E)

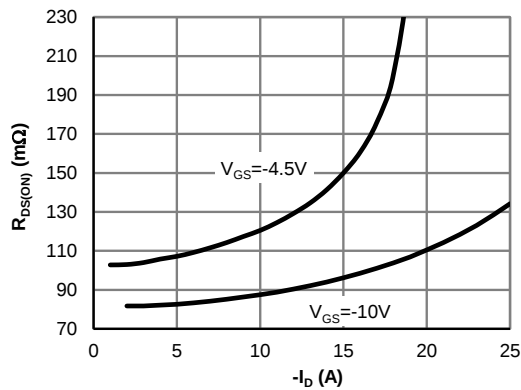


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

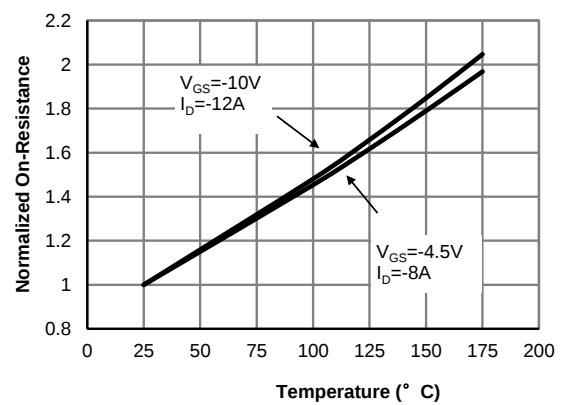


Figure 4: On-Resistance vs. Junction Temperature (Note E)

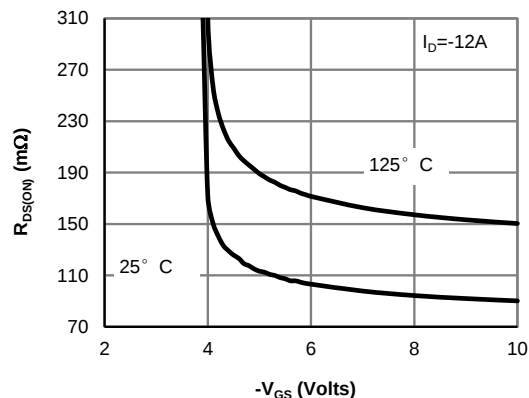


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

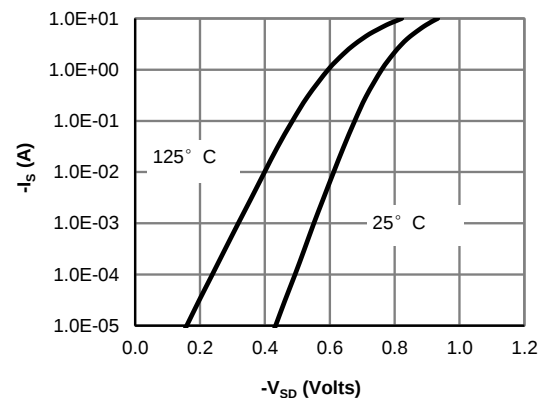


Figure 6: Body-Diode Characteristics (Note E)

P-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

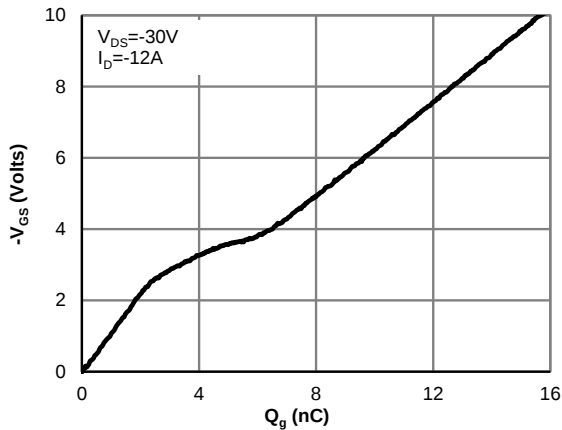


Figure 7: Gate-Charge Characteristics

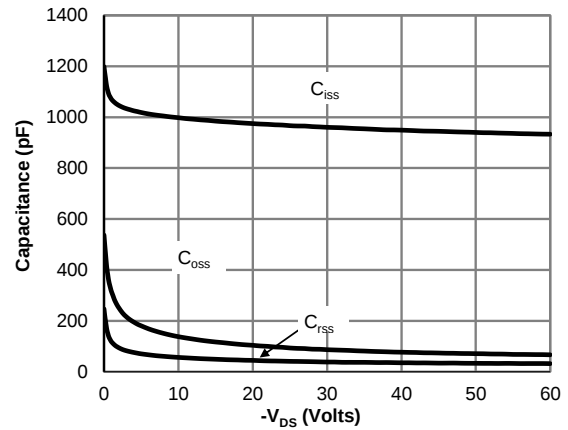


Figure 8: Capacitance Characteristics

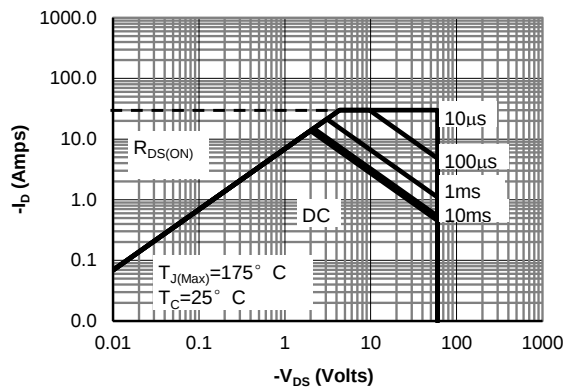


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

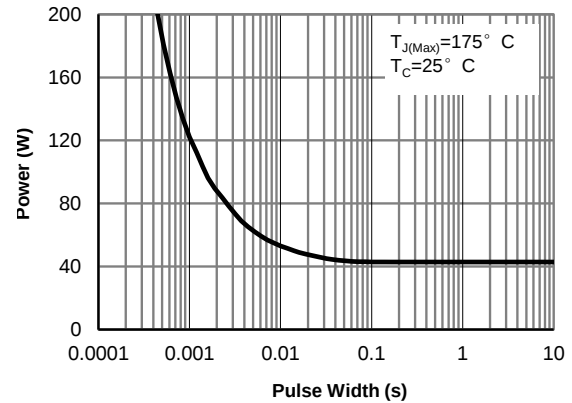


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

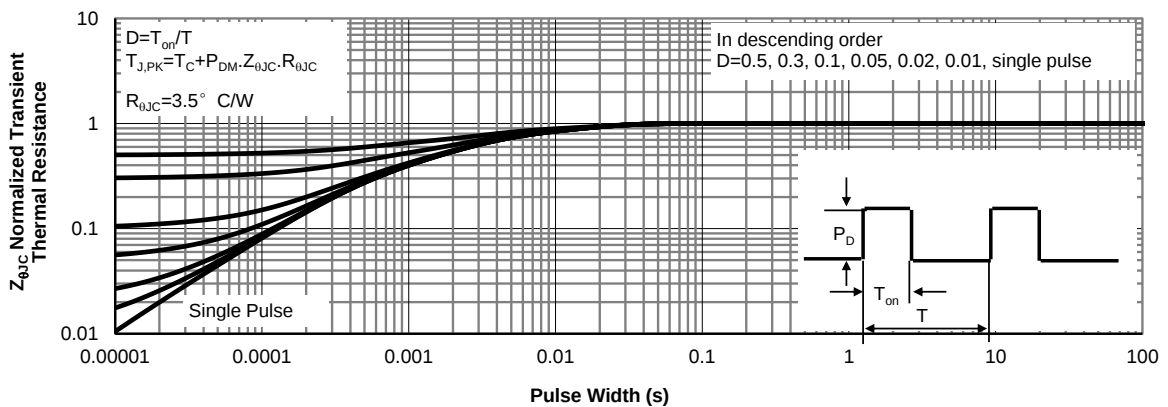


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

P-Channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

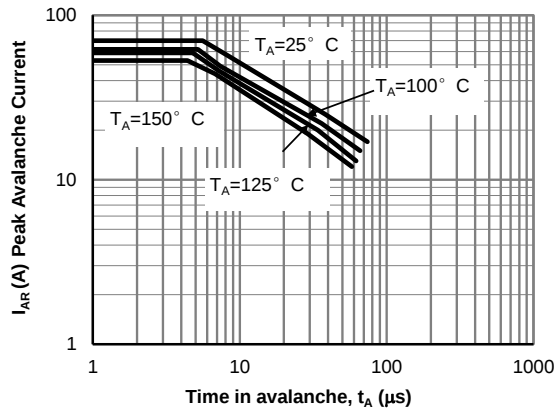


Figure 12: Single Pulse Avalanche capability (Note C)

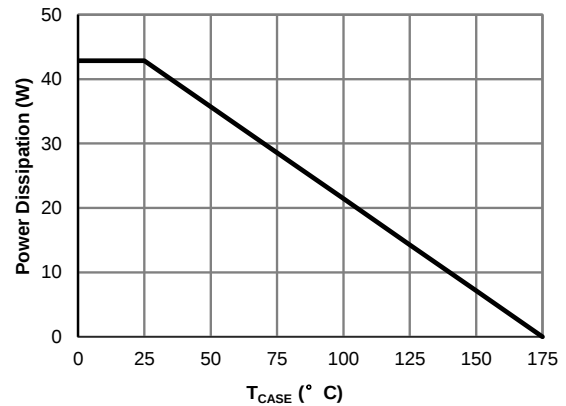


Figure 13: Power De-rating (Note F)

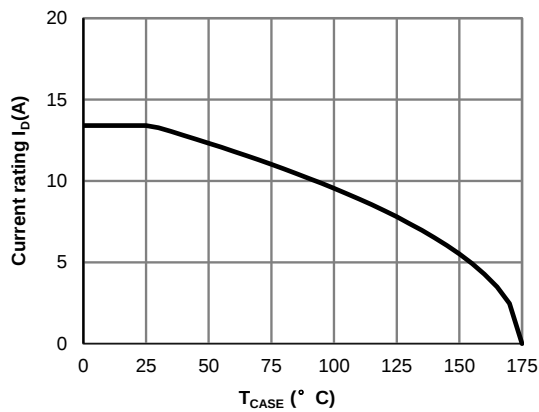


Figure 14: Current De-rating (Note F)

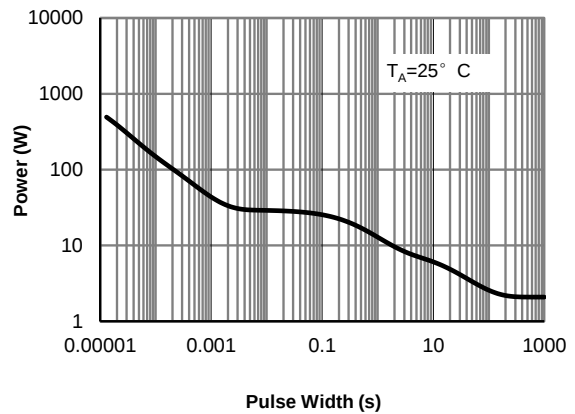


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

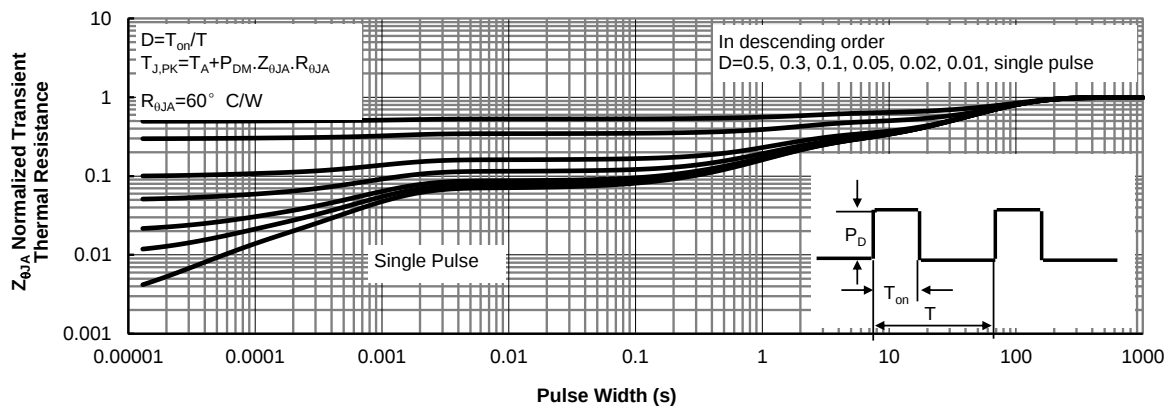
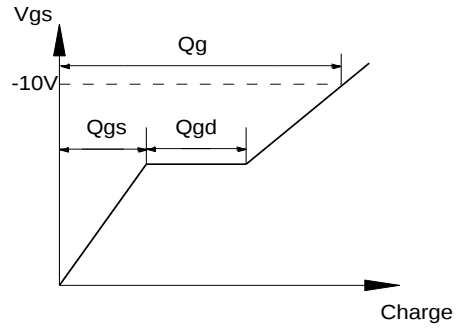
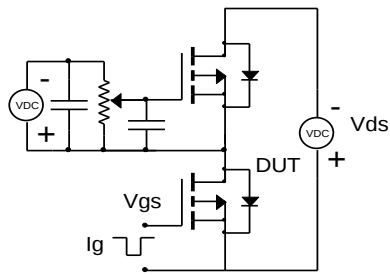
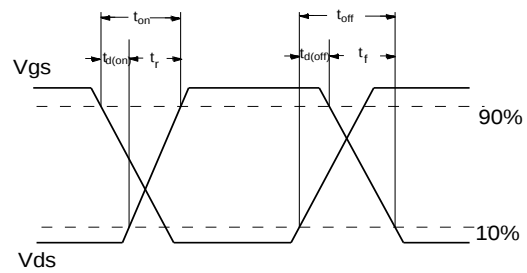
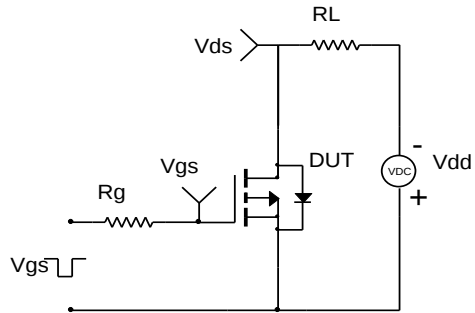


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

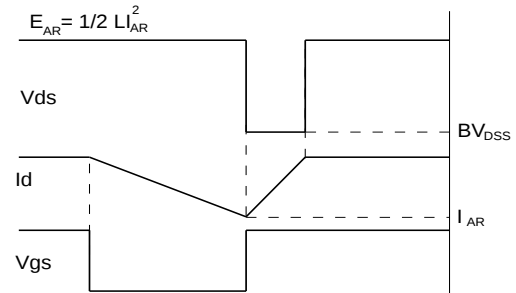
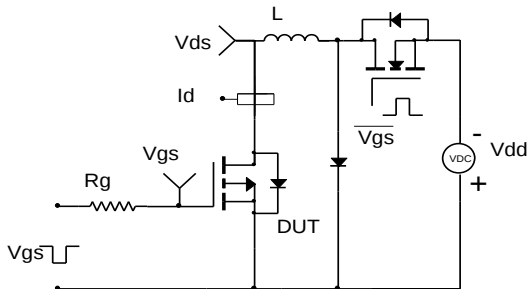
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

