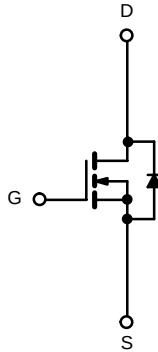
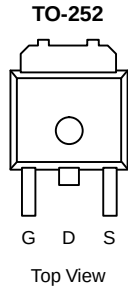


D4110-VB Datasheet

N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^{a, e}	Q_g (Typ)
30	0.005 at $V_{GS} = 10$ V	80	31 nC
	0.006 at $V_{GS} = 4.5$ V	68	



N-Channel MOSFET

FEATURES

- Trench Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2011/65/EU



RoHS
COMPLIANT

APPLICATIONS

- OR-ing
- Server
- DC/DC

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 175$ °C)	$T_C = 25$ °C	I_D	80	A
	$T_C = 70$ °C		60	
	$T_A = 25$ °C		25.8 ^{b, c}	
	$T_A = 70$ °C		22 ^{b, c}	
Pulsed Drain Current		I_{DM}	250	
Avalanche Current Pulse		I_{AS}	39	
Single Pulse Avalanche Energy		E_{AS}	94.8	mJ
Continuous Source-Drain Diode Current	$T_C = 25$ °C	I_S	90 ^{a, e}	A
	$T_A = 25$ °C		3.13 ^{b, c}	
Maximum Power Dissipation	$T_C = 25$ °C	P_D	205 ^a	W
	$T_C = 70$ °C		135	
	$T_A = 25$ °C		3.75 ^{b, c}	
	$T_A = 70$ °C		2.63 ^{b, c}	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typ.	Max.	Unit
Maximum Junction-to-Ambient ^{b, d}	$t \leq 10$ sec	R_{thJA}	32	40	°C/W
Maximum Junction-to-Case	Steady State	R_{thJC}	0.5	0.6	

Notes:

a. Based on $T_C = 25$ °C.

b. Surface mounted on 1" x 1" FR4 board.

c. $t = 10$ sec.

d. Maximum under steady state conditions is 90 °C/W.

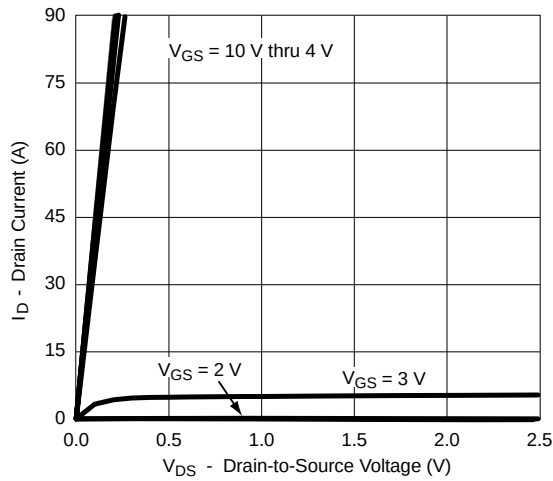
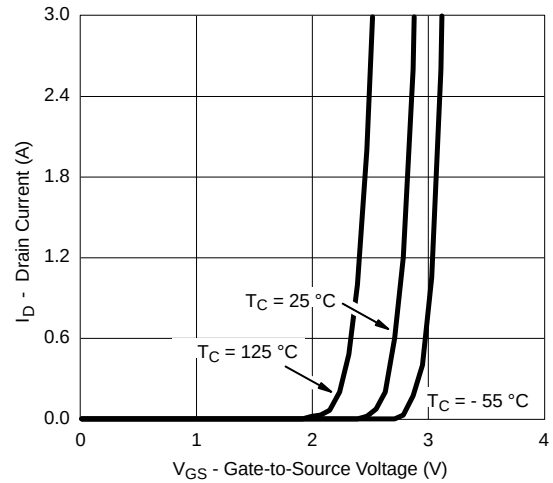
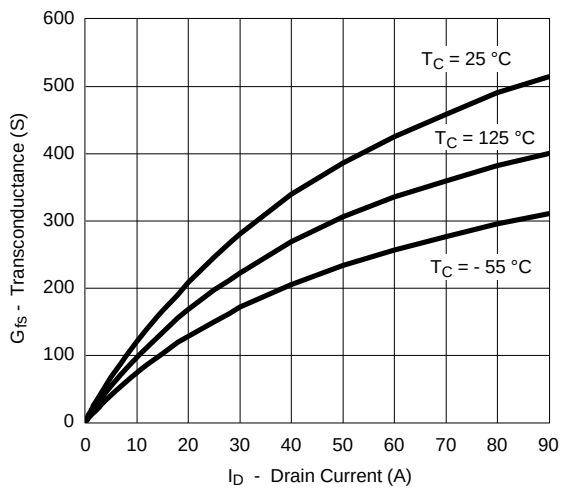
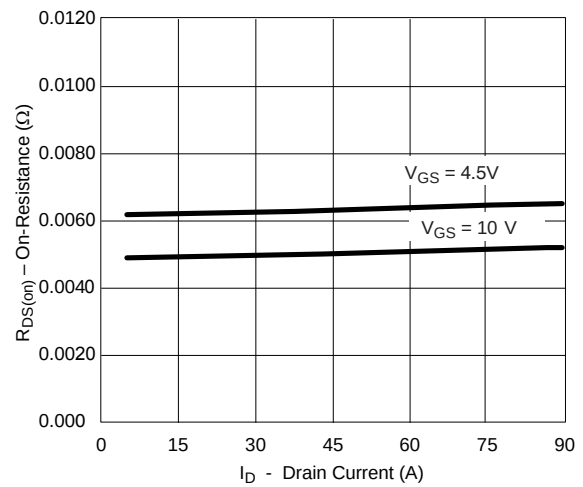
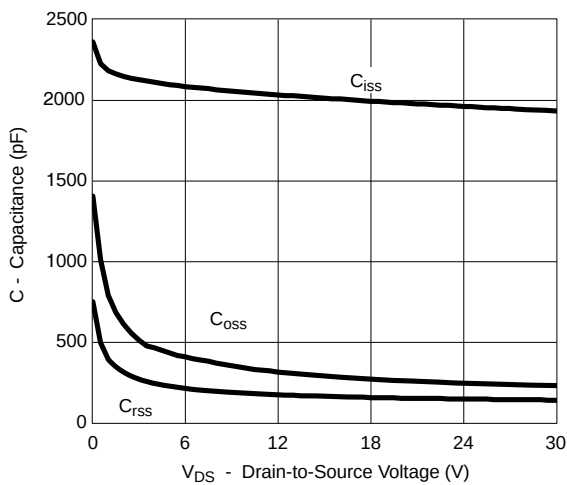
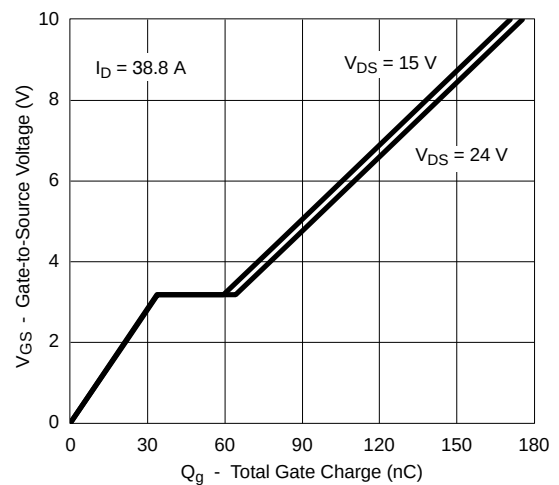
e. Calculated based on maximum junction temperature. Package limitation current is 90 A.

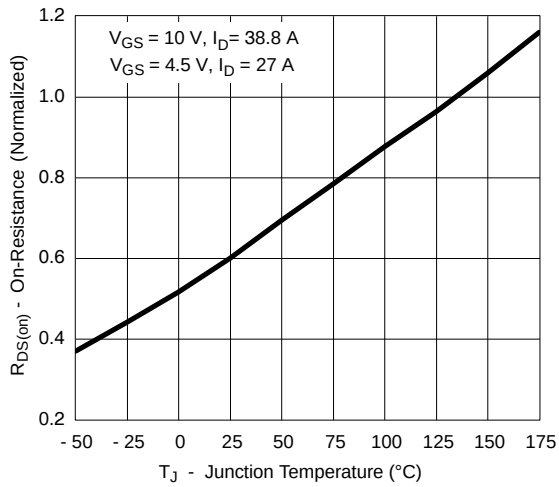
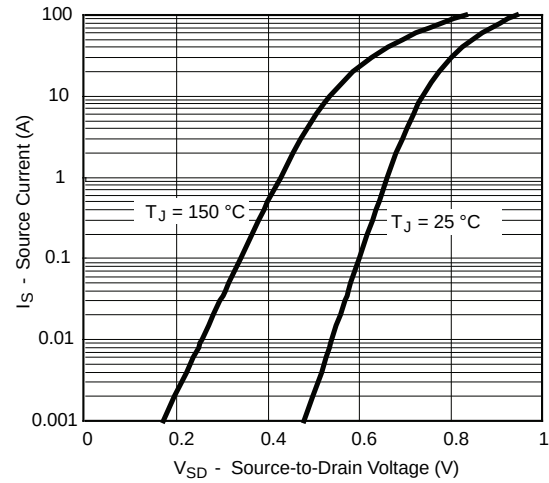
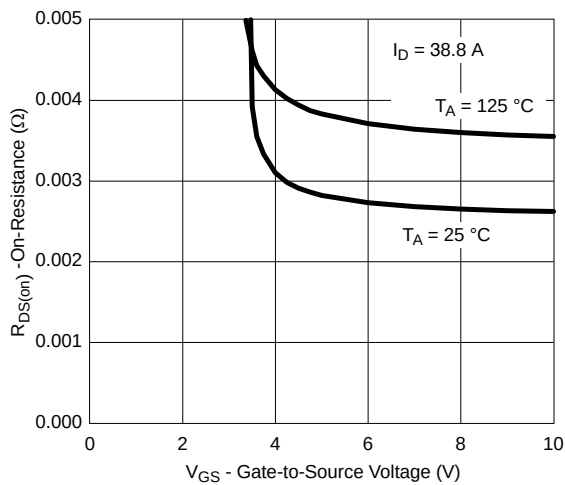
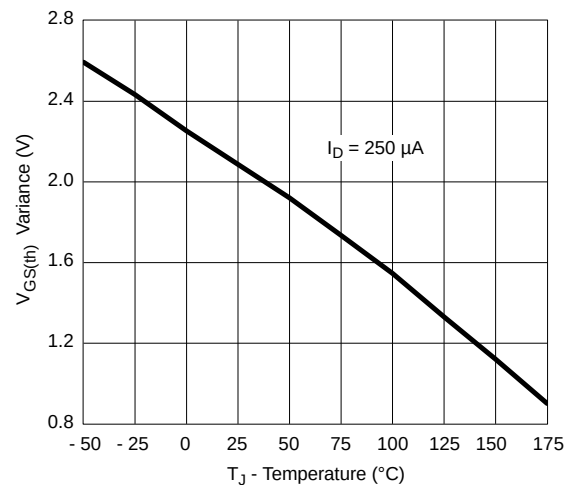
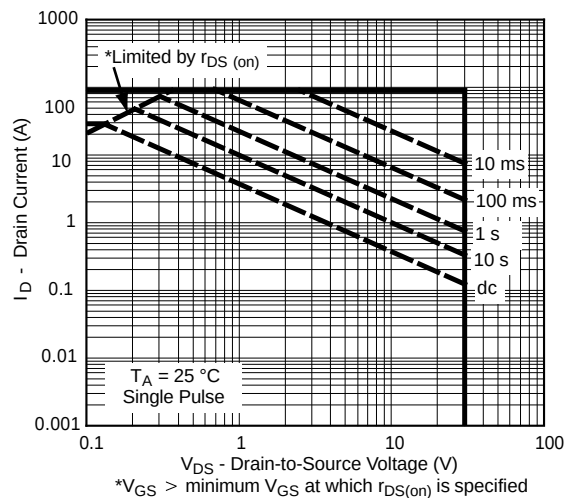
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		35		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 7.5		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.0		2.5	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	90			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 38.8 A		0.005		Ω
		V _{GS} = 4.5 V, I _D = 37 A		0.006		
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 38.8 A		160		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		2201		pF
Output Capacitance	C _{oss}			525		
Reverse Transfer Capacitance	C _{rss}			270		
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 38.8 A		61	107	nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 28.8 A		31.5	50	
Gate-Source Charge	Q _{gs}			10		
Gate-Drain Charge	Q _{gd}			6		
Gate Resistance	R _g	f = 1 MHz		1.4	2.1	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 0.625 Ω I _D ≅ 24 A, V _{GEN} = 10 V, R _g = 1 Ω		18	27	ns
Rise Time	t _r			11	17	
Turn-Off Delay Time	t _{d(off)}			70	105	
Fall Time	t _f			10	15	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 0.67 Ω I _D ≅ 22.5 A, V _{GEN} = 4.5 V, R _g = 1 Ω		55	83	
Rise Time	t _r			180	270	
Turn-Off Delay Time	t _{d(off)}			55	83	
Fall Time	t _f			12	18	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			120	A
Pulse Diode Forward Current ^a	I _{SM}				120	
Body Diode Voltage	V _{SD}	I _S = 22 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 20 A, di/dt = 100 A/μs, T _J = 25 °C		52	78	ns
Body Diode Reverse Recovery Charge	Q _{rr}			70.2	105	nC
Reverse Recovery Fall Time	t _a			27		ns
Reverse Recovery Rise Time	t _b			25		

Notes:

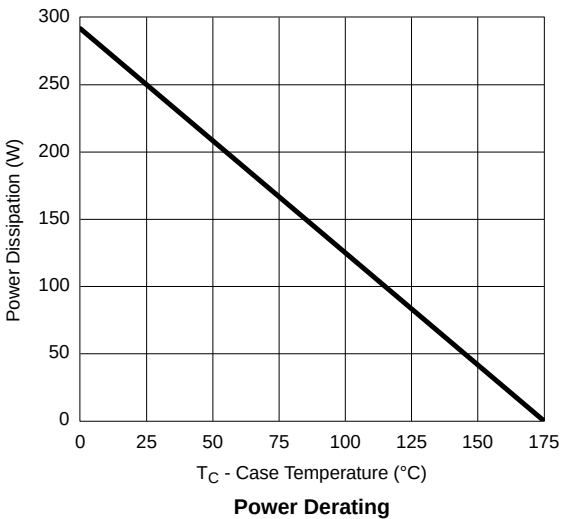
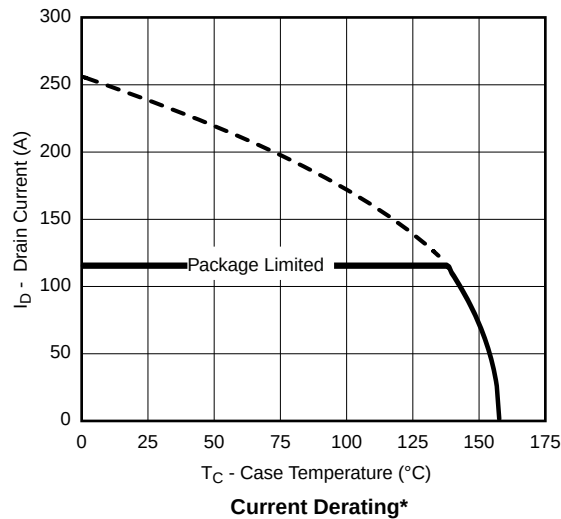
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

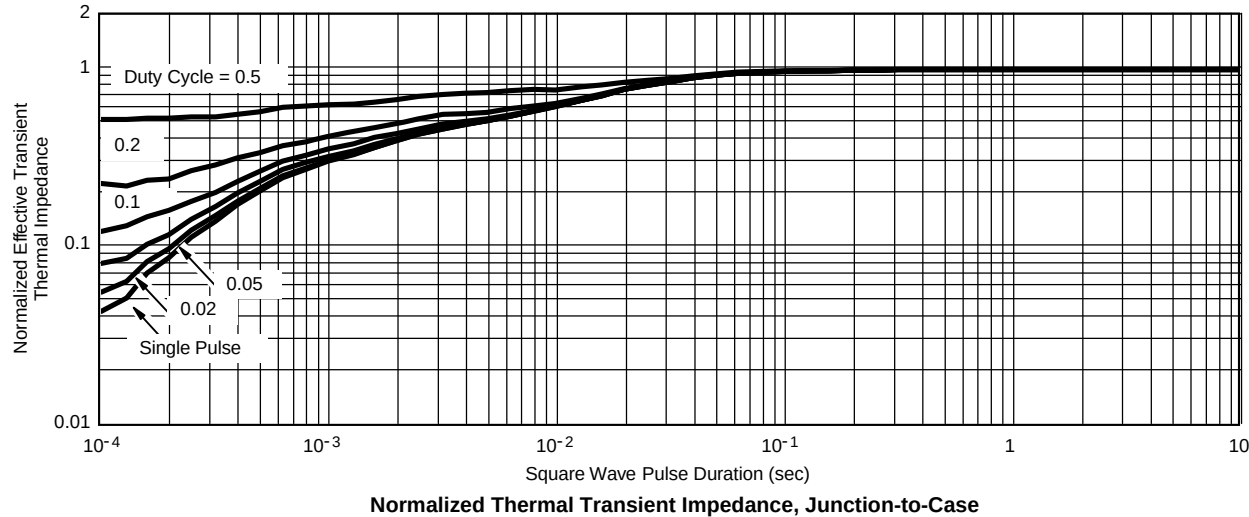
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transconductance

 $R_{DS(on)}$ vs. Drain Current

Capacitance

Gate Charge

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

On-Resistance vs. Junction Temperature

Forward Diode Voltage vs. Temperature

 $R_{DS(on)}$ vs. V_{GS} vs. Temperature

Threshold Voltage

Safe Operating Area, Junction-to-Ambient

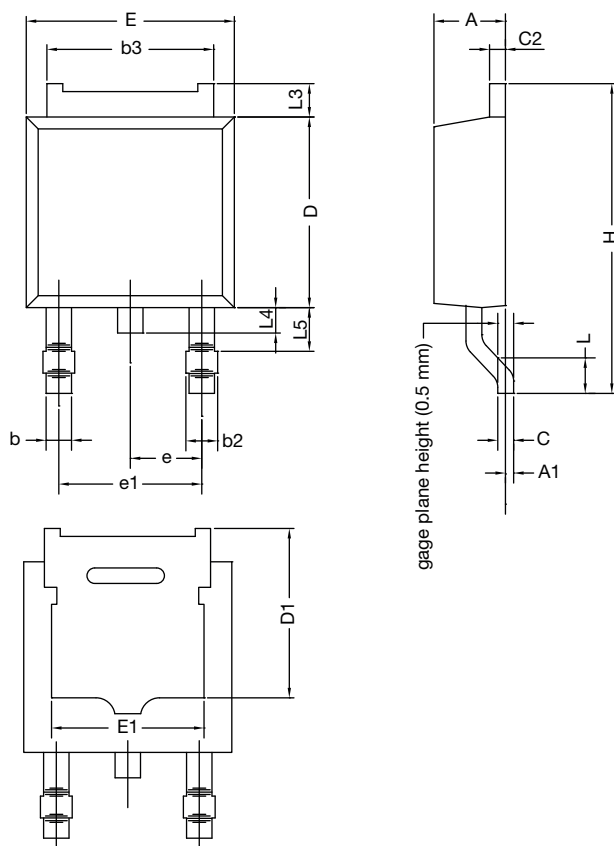
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



*The power dissipation P_D is based on $T_{J(max)} = 175\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TO-252AA CASE OUTLINE

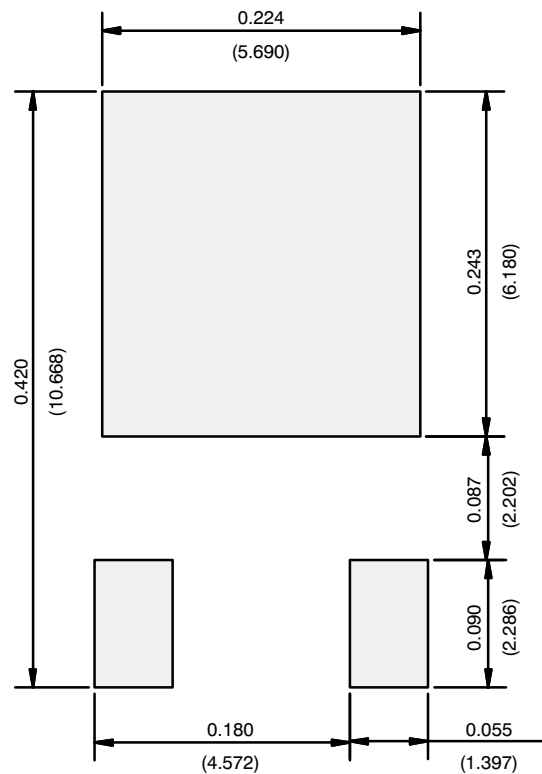


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.14	1.52	0.045	0.060
ECN: X12-0247-Rev. M, 24-Dec-12				
DWG: 5347				

Note

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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