National Semiconductor

T-43-21

MM54HCU04/MM74HCU04 Hex Inverter

General Description

These inverters utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits.

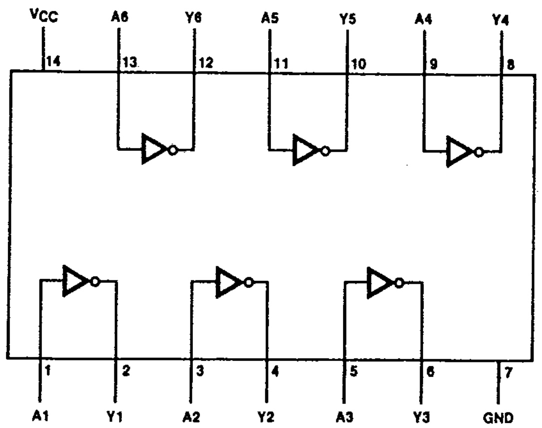
The MM54HCU04/MM74HCU04 is an unbuffered inverter. It has high noise immunity and the ability to drive 15 LS-TTL loads. The 54HCU/74HCU logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 7 ns
- Fanout of 15 LS-TTL loads
- Quiescent power consumption: 10 μA maximum at room temperature
- Low input current: 1 μA maximum

Connection and Schematic Diagrams

Dual-In-Line Package



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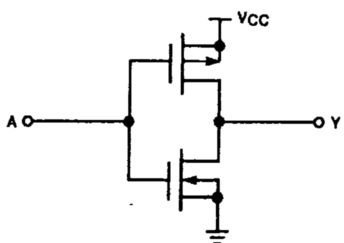
Top View

Order Number MM54HCU04* or MM74HCU04*

*Please look into Section 8, Appendix D for availability of various package types.



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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCU	−40	+85	°C
MM54HCU	−55	+125	°C

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C	74HCU T_A=−40 to 85°C	54HCU T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.7	1.7	1.7	V
			4.5V		3.6	3.6	3.6	V
			6.0V		4.8	4.8	4.8	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.8	0.8	0.8	V
			6.0V		1.1	1.1	1.1	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IL}$ $\|I_{OUT}\|\leq20\ \mu A$	2.0V	2.0	1.8	1.8	1.8	V
			4.5V	4.5	4.0	4.0	4.0	V
			6.0V	6.0	5.5	5.5	5.5	V
		V_{IN}=GND $\|I_{OUT}\|\leq4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ $\|I_{OUT}\|\leq20\ \mu A$	2.0V	0	0.2	0.2	0.2	V
			4.5V	0	0.5	0.5	0.5	V
			6.0V	0	0.5	0.5	0.5	V
		$V_{IN}=V_{CC}$ $\|I_{OUT}\|\leq6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

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Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		7	13	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HCU $T_A=-40$ to 85°C	54HCU $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	49	82	103	120	ns
			4.5V	9.9	16	21	24	ns
			6.0V	8.4	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		90				pF
C_{IN}	Maximum Input Capacitance			8	15	15	15	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Typical Applications

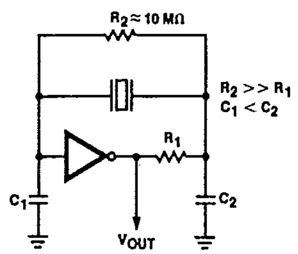

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FIGURE 1. Crystal Oscillator

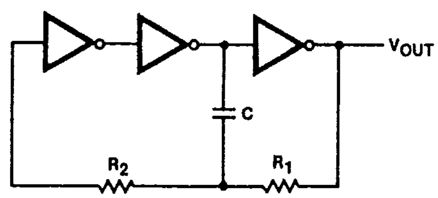

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FIGURE 2. Stable RC Oscillator

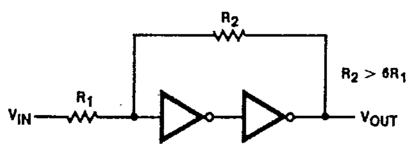

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FIGURE 3. Schmitt Trigger