

# MMDF2P02E

## Power MOSFET 2 Amps, 25 Volts P-Channel SO-8, Dual

These miniature surface mount MOSFETs feature ultra low  $R_{DS(on)}$  and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain-to-source diode has a low reverse recovery time. These devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc-dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

### Features

- Ultra Low  $R_{DS(on)}$  Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO-8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, with Soft Recovery
- $I_{DSS}$  Specified at Elevated Temperatures
- Avalanche Energy Specified
- Mounting Information for SO-8 Package Provided
- This is a Pb-Free Device

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (Note 1)

| Rating                                                                                                                                                                                                                     | Symbol                     | Value            | Unit                      |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|------------------|---------------------------|
| Drain-to-Source Voltage                                                                                                                                                                                                    | $V_{DS}$                   | 25               | Vdc                       |
| Gate-to-Source Voltage – Continuous                                                                                                                                                                                        | $V_{GS}$                   | $\pm 20$         | Vdc                       |
| Drain Current – Continuous @ $T_A = 25^\circ\text{C}$<br>– Continuous @ $T_A = 100^\circ\text{C}$<br>– Single Pulse ( $t_p \leq 10 \mu\text{s}$ )                                                                          | $I_D$<br>$I_D$<br>$I_{DM}$ | 2.5<br>1.7<br>13 | Adc<br>Adc<br>Apk         |
| Total Power Dissipation @ $T_A = 25^\circ\text{C}$<br>(Note 2)<br>Derate above $25^\circ\text{C}$                                                                                                                          | $P_D$                      | 2.0<br>16        | W<br>mW/ $^\circ\text{C}$ |
| Operating and Storage Temperature Range                                                                                                                                                                                    | $T_J, T_{stg}$             | -55 to 150       | $^\circ\text{C}$          |
| Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$<br>( $V_{DD} = 20 \text{ Vdc}$ , $V_{GS} = 10 \text{ Vdc}$ , Peak<br>$I_L = 7.0 \text{ Apk}$ , $L = 10 \text{ mH}$ , $R_G = 25 \Omega$ ) | $E_{AS}$                   | 245              | mJ                        |
| Thermal Resistance, Junction-to-Ambient<br>(Note 2)                                                                                                                                                                        | $R_{\theta JA}$            | 62.5             | $^\circ\text{C/W}$        |
| Maximum Lead Temperature for Soldering<br>Purposes, 0.0625" from case for 10 sec.                                                                                                                                          | $T_L$                      | 260              | $^\circ\text{C}$          |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Negative sign for P-Channel device omitted for clarity.
2. Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided) with one die operating, 10 sec. max.

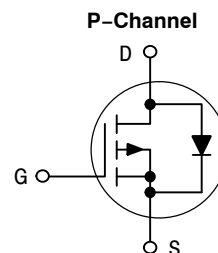


**ON Semiconductor®**

<http://onsemi.com>

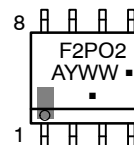
**2 AMPERES, 25 VOLTS**

**$R_{DS(on)} = 250 \text{ m}\Omega$**



**SO-8, Dual  
CASE 751  
STYLE 11**

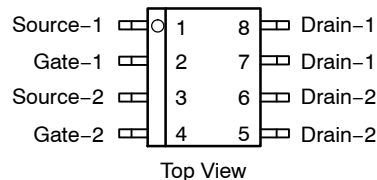
### MARKING DIAGRAM



F2P02 = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### PIN ASSIGNMENT



Top View

### ORDERING INFORMATION

| Device       | Package           | Shipping†        |
|--------------|-------------------|------------------|
| MMDF2P02ER2G | SO-8<br>(Pb-Free) | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MMDF2P02E

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted) (Note 3)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

### OFF CHARACTERISTICS

|                                                                                                                                                                                 |               |         |          |           |                             |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|----------|-----------|-----------------------------|
| Drain-to-Source Breakdown Voltage<br>( $V_{GS} = 0\text{ Vdc}$ , $I_D = 250\text{ }\mu\text{Adc}$ )<br>Temperature Coefficient (Positive)                                       | $V_{(BR)DSS}$ | 25<br>– | –<br>2.2 | –<br>–    | Vdc<br>mV/ $^\circ\text{C}$ |
| Zero Gate Voltage Drain Current<br>( $V_{DS} = 20\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )<br>( $V_{DS} = 20\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $T_J = 125^\circ\text{C}$ ) | $I_{DSS}$     | –<br>–  | –<br>–   | 1.0<br>10 | $\mu\text{Adc}$             |
| Gate-Body Leakage Current ( $V_{GS} = \pm 20\text{ Vdc}$ , $V_{DS} = 0$ )                                                                                                       | $I_{GSS}$     | –       | –        | 100       | nAdc                        |

### ON CHARACTERISTICS (Note 4)

|                                                                                                                                                         |              |          |             |             |          |
|---------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|----------|-------------|-------------|----------|
| Gate Threshold Voltage<br>( $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{Adc}$ )<br>Temperature Coefficient (Negative)                                | $V_{GS(th)}$ | 1.0<br>– | 2.0<br>3.8  | 3.0<br>–    | Vdc      |
| Static Drain-to-Source On-Resistance<br>( $V_{GS} = 10\text{ Vdc}$ , $I_D = 2.0\text{ Adc}$ )<br>( $V_{GS} = 4.5\text{ Vdc}$ , $I_D = 1.0\text{ Adc}$ ) | $R_{DS(on)}$ | –<br>–   | 0.19<br>0.3 | 0.25<br>0.4 | $\Omega$ |
| Forward Transconductance ( $V_{DS} = 3.0\text{ Vdc}$ , $I_D = 1.0\text{ Adc}$ )                                                                         | $g_{FS}$     | 1.0      | 2.8         | –           | Mhos     |

### DYNAMIC CHARACTERISTICS

|                      |                                                                                 |           |   |     |     |    |
|----------------------|---------------------------------------------------------------------------------|-----------|---|-----|-----|----|
| Input Capacitance    | $(V_{DS} = 16\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ ,<br>$f = 1.0\text{ MHz}$ ) | $C_{iss}$ | – | 340 | 475 | pF |
| Output Capacitance   |                                                                                 | $C_{oss}$ | – | 220 | 300 |    |
| Transfer Capacitance |                                                                                 | $C_{rss}$ | – | 75  | 150 |    |

### SWITCHING CHARACTERISTICS (Note 5)

|                     |                                                                                                                 |              |   |     |     |    |
|---------------------|-----------------------------------------------------------------------------------------------------------------|--------------|---|-----|-----|----|
| Turn-On Delay Time  | $(V_{DD} = 10\text{ Vdc}$ , $I_D = 2.0\text{ Adc}$ ,<br>$V_{GS} = 5.0\text{ Vdc}$ , $R_G = 6.0\text{ }\Omega$ ) | $t_{d(on)}$  | – | 20  | 40  | ns |
| Rise Time           |                                                                                                                 | $t_r$        | – | 40  | 80  |    |
| Turn-Off Delay Time |                                                                                                                 | $t_{d(off)}$ | – | 53  | 106 |    |
| Fall Time           |                                                                                                                 | $t_f$        | – | 41  | 82  |    |
| Turn-On Delay Time  | $(V_{DD} = 10\text{ Vdc}$ , $I_D = 2.0\text{ Adc}$ ,<br>$V_{GS} = 10\text{ Vdc}$ , $R_G = 6.0\text{ }\Omega$ )  | $t_{d(on)}$  | – | 13  | 26  |    |
| Rise Time           |                                                                                                                 | $t_r$        | – | 29  | 58  |    |
| Turn-Off Delay Time |                                                                                                                 | $t_{d(off)}$ | – | 30  | 60  |    |
| Fall Time           |                                                                                                                 | $t_f$        | – | 28  | 56  |    |
| Gate Charge         | $(V_{DS} = 16\text{ Vdc}$ , $I_D = 2.0\text{ Adc}$ ,<br>$V_{GS} = 10\text{ Vdc}$ )                              | $Q_T$        | – | 10  | 15  | nC |
|                     |                                                                                                                 | $Q_1$        | – | 1.0 | –   |    |
|                     |                                                                                                                 | $Q_2$        | – | 3.5 | –   |    |
|                     |                                                                                                                 | $Q_3$        | – | 3.0 | –   |    |

### SOURCE-DrAIN DIODE CHARACTERISTICS

|                                        |                                                                                               |          |   |       |     |               |
|----------------------------------------|-----------------------------------------------------------------------------------------------|----------|---|-------|-----|---------------|
| Forward On-Voltage (Note 4)            | $(I_S = 2.0\text{ Adc}$ , $V_{GS} = 0\text{ Vdc}$ )                                           | $V_{SD}$ | – | 1.5   | 2.0 | Vdc           |
| Reverse Recovery Time<br>See Figure 11 | $(I_S = 2.0\text{ Adc}$ , $V_{GS} = 0\text{ Vdc}$ ,<br>$dI_S/dt = 100\text{ A}/\mu\text{s}$ ) | $t_{rr}$ | – | 32    | 64  | ns            |
|                                        |                                                                                               | $t_a$    | – | 19    | –   |               |
|                                        |                                                                                               | $t_b$    | – | 12    | –   |               |
| Reverse Recovery Storage Charge        |                                                                                               | $Q_{RR}$ | – | 0.035 | –   | $\mu\text{C}$ |

- Negative sign for P-Channel device omitted for clarity.
- Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

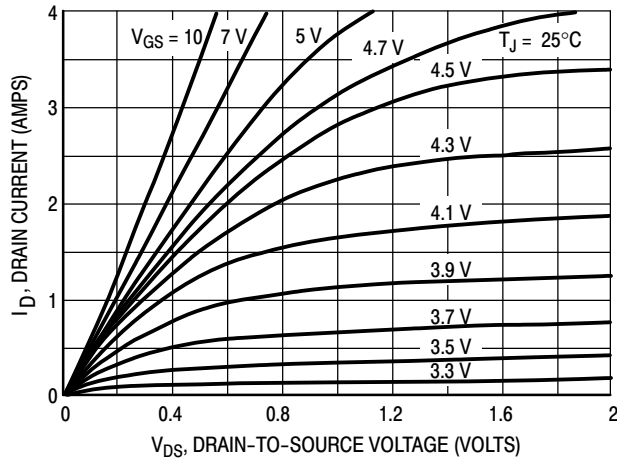


Figure 1. On-Region Characteristics

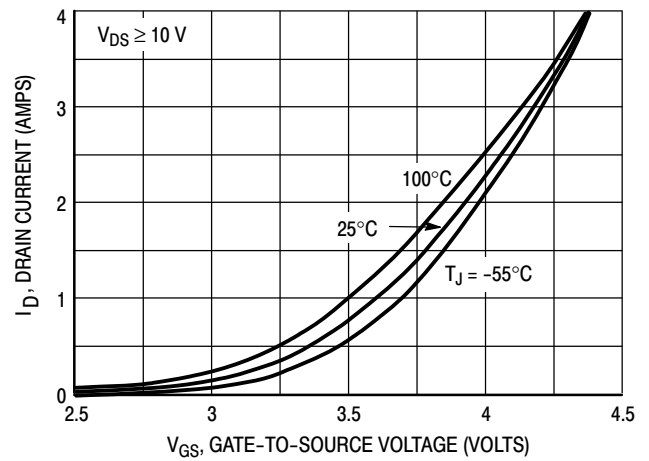


Figure 2. Transfer Characteristics

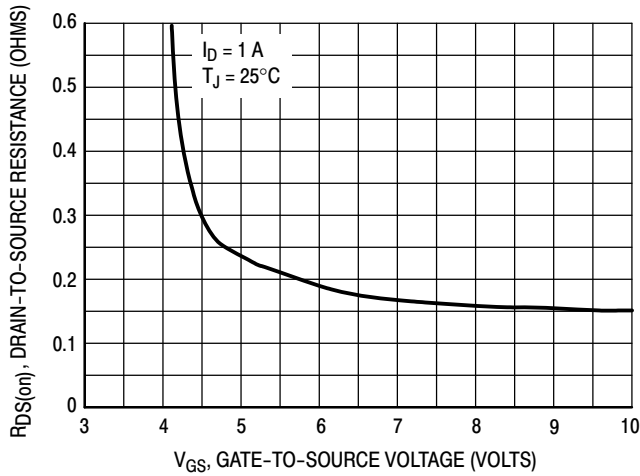


Figure 3. On-Resistance versus Gate-to-Source Voltage

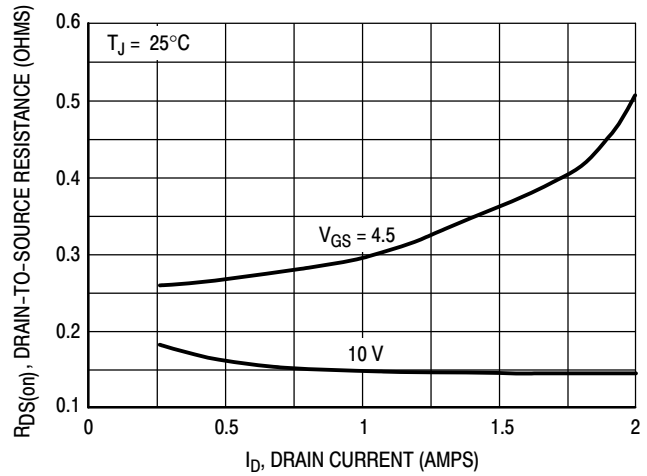


Figure 4. On-Resistance versus Drain Current and Gate Voltage

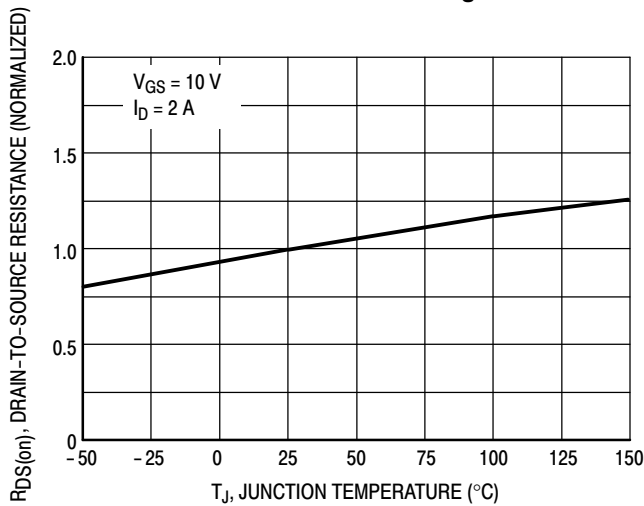


Figure 5. On-Resistance Variation with Temperature

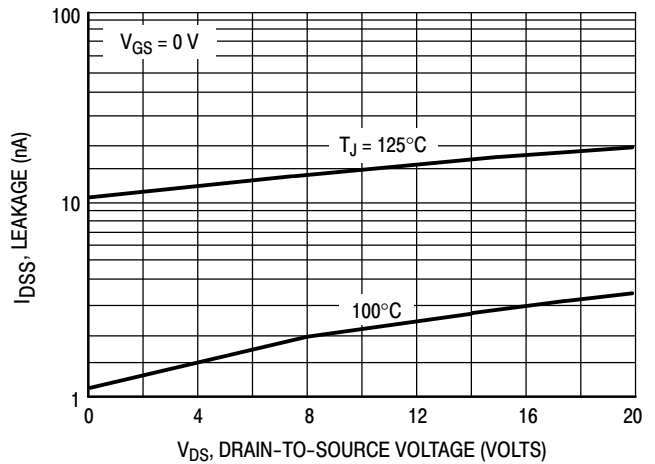


Figure 6. Drain-to-Source Leakage Current versus Voltage

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ( $\Delta t$ ) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ( $I_{G(AV)}$ ) can be made from a rudimentary analysis of the drive circuit so that

$$t = Q/I_{G(AV)}$$

During the rise and fall time interval when switching a resistive load,  $V_{GS}$  remains virtually constant at a level known as the plateau voltage,  $V_{SGP}$ . Therefore, rise and fall times may be approximated by the following:

$$t_r = Q_2 \times R_G / (V_{GG} - V_{SGP})$$

$$t_f = Q_2 \times R_G / V_{SGP}$$

where

$V_{GG}$  = the gate drive voltage, which varies from zero to  $V_{GG}$

$R_G$  = the gate drive resistance

and  $Q_2$  and  $V_{SGP}$  are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{SGP})]$$

$$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{SGP})$$

The capacitance ( $C_{iss}$ ) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating  $t_{d(on)}$  and is read at a voltage corresponding to the on–state when calculating  $t_{d(off)}$ .

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by  $L di/dt$ , but since  $di/dt$  is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

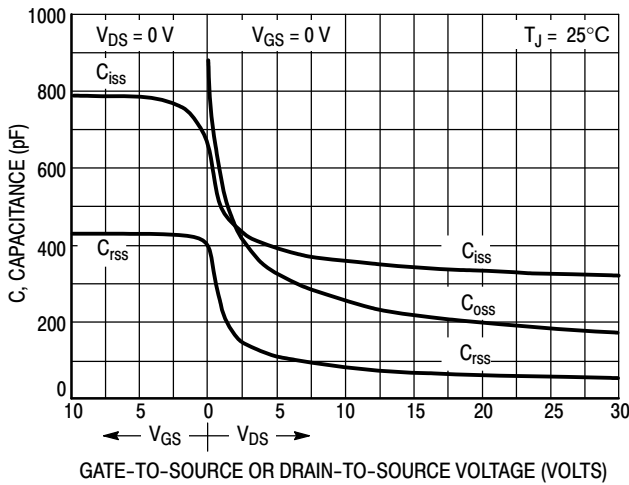


Figure 7. Capacitance Variation

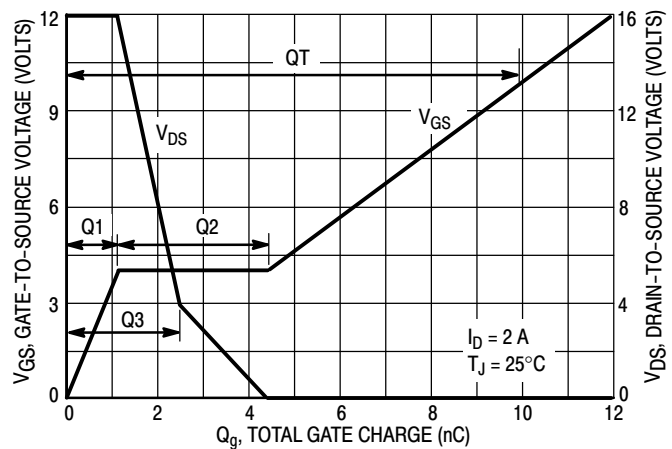


Figure 8. Gate–to–Source and Drain–to–Source Voltage versus Total Charge

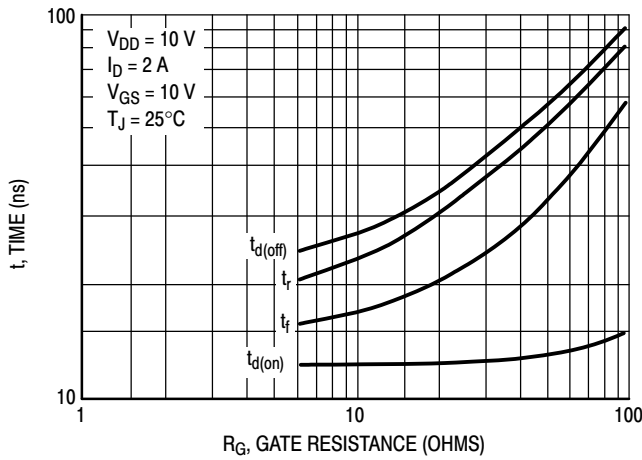


Figure 9. Resistive Switching Time Variation versus Gate Resistance

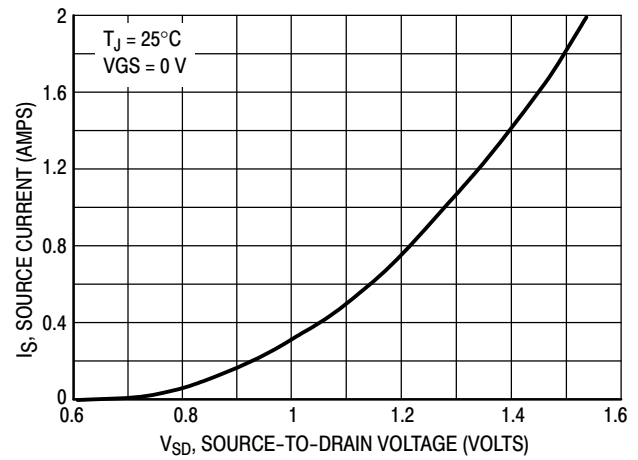


Figure 10. Diode Forward Voltage versus Current

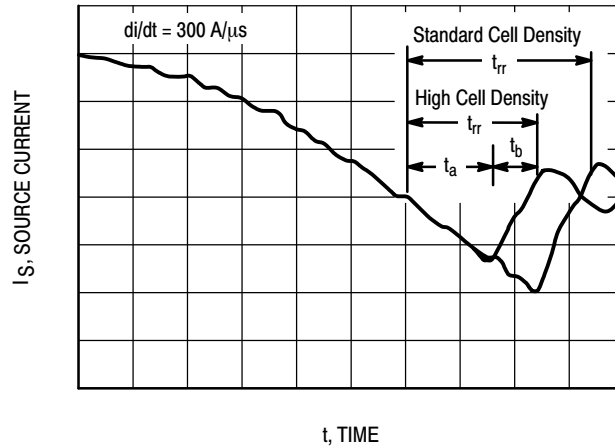


Figure 11. Reverse Recovery Time ( $t_{rr}$ )

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain-to-source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ( $T_C$ ) of  $25^\circ\text{C}$ . Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off-state and the on-state may traverse any load line provided neither rated peak current ( $I_{DM}$ ) nor rated voltage ( $V_{DSS}$ ) is exceeded, and that the transition time ( $t_r$ ,  $t_f$ ) does not exceed  $10\text{ }\mu\text{s}$ . In addition the total power averaged over a complete switching cycle must not exceed  $(T_{J(MAX)} - T_C)/(R_{\theta JC})$ .

This MOSFET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non-linearly with an increase of peak current in avalanche and peak junction temperature.

Although many MOSFETs can withstand the stress of drain-to-source avalanche at currents up to rated pulsed current ( $I_{DM}$ ), the energy rating is specified at rated continuous current ( $I_D$ ), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous  $I_D$  can safely be assumed to equal the values indicated.

# MMDF2P02E

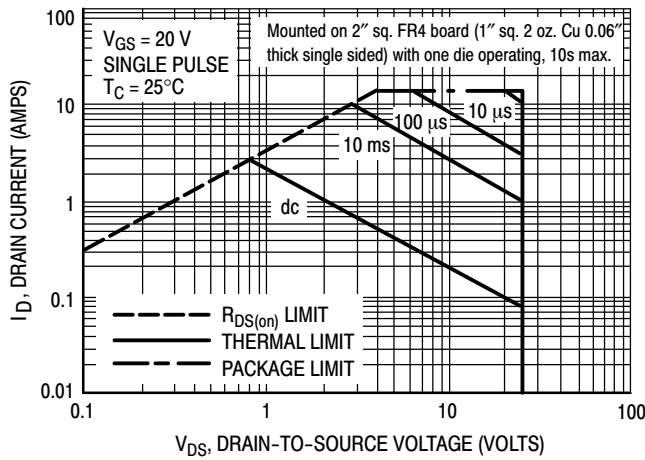


Figure 12. Maximum Rated Forward Biased Safe Operating Area

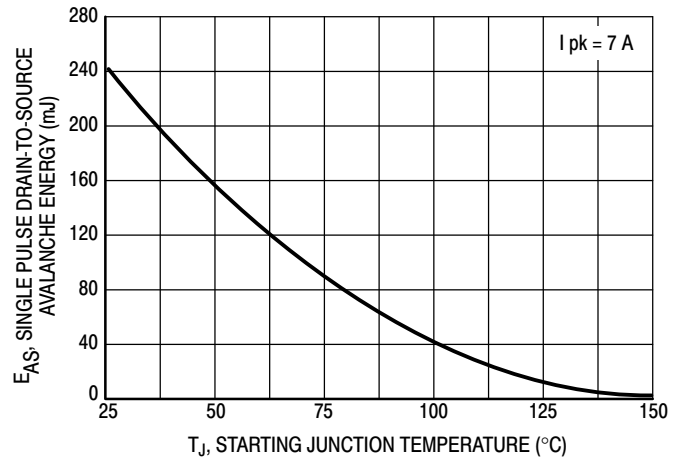


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

## TYPICAL ELECTRICAL CHARACTERISTICS

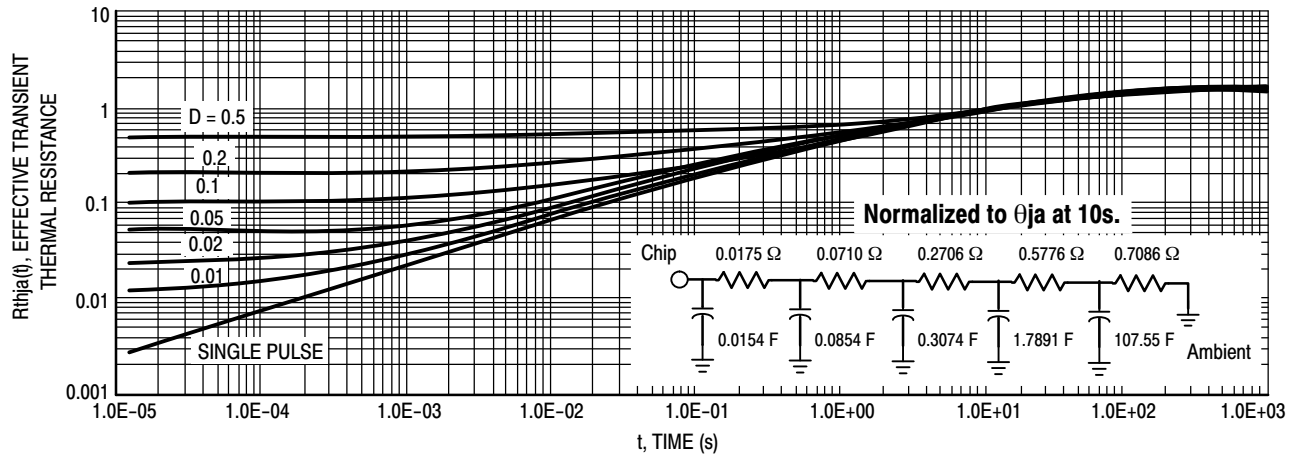


Figure 14. Thermal Response

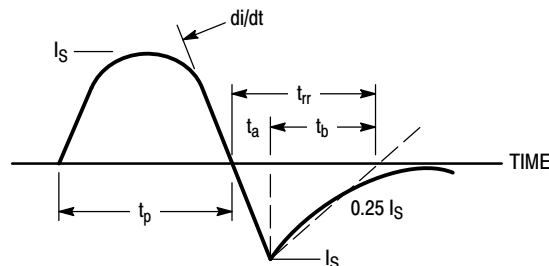
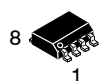


Figure 15. Diode Reverse Recovery Waveform

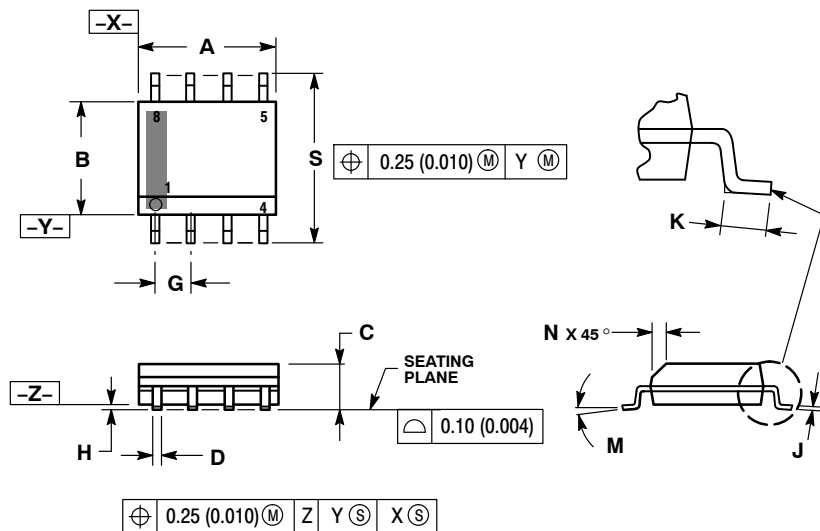
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011

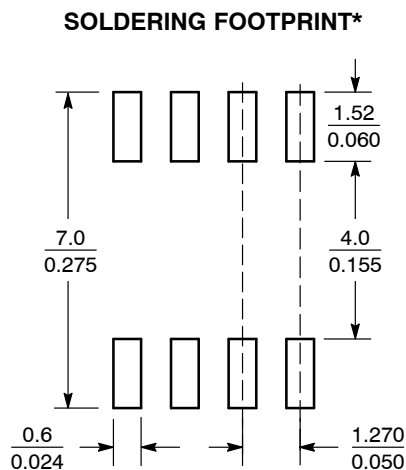


## NOTES:

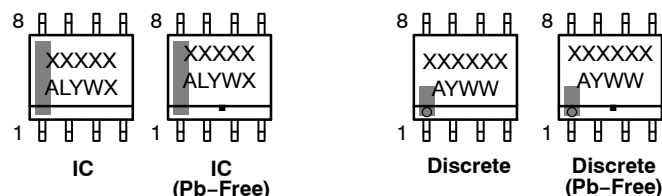
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

## GENERIC MARKING DIAGRAM\*



SCALE 6:1 (mm/inches)



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## STYLES ON PAGE 2

|                  |             |                                                                                                                                                                                  |
|------------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98ASB42564B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | SOIC-8 NB   | PAGE 1 OF 2                                                                                                                                                                      |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

|                                                                                                                                                                                                   |                                                                                                                                                                                          |                                                                                                                                                                                    |                                                                                                                                                                                                        |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>STYLE 1:</b><br>PIN 1. EMITTER<br>2. COLLECTOR<br>3. COLLECTOR<br>4. EMITTER<br>5. EMITTER<br>6. BASE<br>7. BASE<br>8. EMITTER                                                                 | <b>STYLE 2:</b><br>PIN 1. COLLECTOR, DIE, #1<br>2. COLLECTOR, #1<br>3. COLLECTOR, #2<br>4. COLLECTOR, #2<br>5. BASE, #2<br>6. EMITTER, #2<br>7. BASE, #1<br>8. EMITTER, #1               | <b>STYLE 3:</b><br>PIN 1. DRAIN, DIE #1<br>2. DRAIN, #1<br>3. DRAIN, #2<br>4. DRAIN, #2<br>5. GATE, #2<br>6. SOURCE, #2<br>7. GATE, #1<br>8. SOURCE, #1                            | <b>STYLE 4:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. ANODE<br>4. ANODE<br>5. ANODE<br>6. ANODE<br>7. ANODE<br>8. COMMON CATHODE                                                                           |
| <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. DRAIN<br>3. DRAIN<br>4. DRAIN<br>5. GATE<br>6. GATE<br>7. SOURCE<br>8. SOURCE                                                                               | <b>STYLE 6:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. DRAIN<br>4. SOURCE<br>5. SOURCE<br>6. GATE<br>7. GATE<br>8. SOURCE                                                                    | <b>STYLE 7:</b><br>PIN 1. INPUT<br>2. EXTERNAL BYPASS<br>3. THIRD STAGE SOURCE<br>4. GROUND<br>5. DRAIN<br>6. GATE 3<br>7. SECOND STAGE Vd<br>8. FIRST STAGE Vd                    | <b>STYLE 8:</b><br>PIN 1. COLLECTOR, DIE #1<br>2. BASE, #1<br>3. BASE, #2<br>4. COLLECTOR, #2<br>5. COLLECTOR, #2<br>6. EMITTER, #2<br>7. EMITTER, #1<br>8. COLLECTOR, #1                              |
| <b>STYLE 9:</b><br>PIN 1. EMITTER, COMMON<br>2. COLLECTOR, DIE #1<br>3. COLLECTOR, DIE #2<br>4. EMITTER, COMMON<br>5. EMITTER, COMMON<br>6. BASE, DIE #2<br>7. BASE, DIE #1<br>8. EMITTER, COMMON | <b>STYLE 10:</b><br>PIN 1. GROUND<br>2. BIAS 1<br>3. OUTPUT<br>4. GROUND<br>5. GROUND<br>6. BIAS 2<br>7. INPUT<br>8. GROUND                                                              | <b>STYLE 11:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. DRAIN 2<br>7. DRAIN 1<br>8. DRAIN 1                                               | <b>STYLE 12:</b><br>PIN 1. SOURCE<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                                 |
| <b>STYLE 13:</b><br>PIN 1. N.C.<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                              | <b>STYLE 14:</b><br>PIN 1. N-SOURCE<br>2. N-GATE<br>3. P-SOURCE<br>4. P-GATE<br>5. P-DRAIN<br>6. P-DRAIN<br>7. N-DRAIN<br>8. N-DRAIN                                                     | <b>STYLE 15:</b><br>PIN 1. ANODE 1<br>2. ANODE 1<br>3. ANODE 1<br>4. ANODE 1<br>5. CATHODE, COMMON<br>6. CATHODE, COMMON<br>7. CATHODE, COMMON<br>8. CATHODE, COMMON               | <b>STYLE 16:</b><br>PIN 1. EMITTER, DIE #1<br>2. BASE, DIE #1<br>3. EMITTER, DIE #2<br>4. BASE, DIE #2<br>5. COLLECTOR, DIE #2<br>6. COLLECTOR, DIE #2<br>7. COLLECTOR, DIE #1<br>8. COLLECTOR, DIE #1 |
| <b>STYLE 17:</b><br>PIN 1. VCC<br>2. V2OUT<br>3. V1OUT<br>4. TXE<br>5. RXE<br>6. VEE<br>7. GND<br>8. ACC                                                                                          | <b>STYLE 18:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. CATHODE<br>8. CATHODE                                                                 | <b>STYLE 19:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. MIRROR 2<br>7. DRAIN 1<br>8. MIRROR 1                                             | <b>STYLE 20:</b><br>PIN 1. SOURCE (N)<br>2. GATE (N)<br>3. SOURCE (P)<br>4. GATE (P)<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                   |
| <b>STYLE 21:</b><br>PIN 1. CATHODE 1<br>2. CATHODE 2<br>3. CATHODE 3<br>4. CATHODE 4<br>5. CATHODE 5<br>6. COMMON ANODE<br>7. COMMON ANODE<br>8. CATHODE 6                                        | <b>STYLE 22:</b><br>PIN 1. I/O LINE 1<br>2. COMMON CATHODE/VCC<br>3. COMMON CATHODE/VCC<br>4. I/O LINE 3<br>5. COMMON ANODE/GND<br>6. I/O LINE 4<br>7. I/O LINE 5<br>8. COMMON ANODE/GND | <b>STYLE 23:</b><br>PIN 1. LINE 1 IN<br>2. COMMON ANODE/GND<br>3. COMMON ANODE/GND<br>4. LINE 2 IN<br>5. LINE 2 OUT<br>6. COMMON ANODE/GND<br>7. COMMON ANODE/GND<br>8. LINE 1 OUT | <b>STYLE 24:</b><br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR/ANODE<br>4. COLLECTOR/ANODE<br>5. CATHODE<br>6. CATHODE<br>7. COLLECTOR/ANODE<br>8. COLLECTOR/ANODE                                      |
| <b>STYLE 25:</b><br>PIN 1. VIN<br>2. N/C<br>3. REXT<br>4. GND<br>5. IOUT<br>6. IOUT<br>7. IOUT<br>8. IOUT                                                                                         | <b>STYLE 26:</b><br>PIN 1. GND<br>2. dv/dt<br>3. ENABLE<br>4. ILIMIT<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. VCC                                                                    | <b>STYLE 27:</b><br>PIN 1. ILIMIT<br>2. OVLO<br>3. UVLO<br>4. INPUT+<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. DRAIN                                                            | <b>STYLE 28:</b><br>PIN 1. SW_TO_GND<br>2. DASIC_OFF<br>3. DASIC_SW_DET<br>4. GND<br>5. V_MON<br>6. VBULK<br>7. VBULK<br>8. VIN                                                                        |
| <b>STYLE 29:</b><br>PIN 1. BASE, DIE #1<br>2. EMITTER, #1<br>3. BASE, #2<br>4. EMITTER, #2<br>5. COLLECTOR, #2<br>6. COLLECTOR, #2<br>7. COLLECTOR, #1<br>8. COLLECTOR, #1                        | <b>STYLE 30:</b><br>PIN 1. DRAIN 1<br>2. DRAIN 1<br>3. GATE 2<br>4. SOURCE 2<br>5. SOURCE 1/DRAIN 2<br>6. SOURCE 1/DRAIN 2<br>7. SOURCE 1/DRAIN 2<br>8. GATE 1                           |                                                                                                                                                                                    |                                                                                                                                                                                                        |

|                         |                    |                                                                                                                                                                                     |
|-------------------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DOCUMENT NUMBER:</b> | <b>98ASB42564B</b> | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| <b>DESCRIPTION:</b>     | <b>SOIC-8 NB</b>   | <b>PAGE 2 OF 2</b>                                                                                                                                                                  |

**onsemi** and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)