CY7C1339G

4-Mbit (128K × 32) Pipelined Sync SRAM

Features

- Registered inputs and outputs for pipelined operation
- 128K × 32 common I/O architecture
- 3.3 V core power supply (V_{DD})
- 2.5 V/3.3 V I/O power supply (V_{DDQ})
- Fast clock-to-output times
  - 4.0 ns (for 133-MHz device)
- Provide high-performance 3-1-1-1 access rate
- User-selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed writes
- Asynchronous output enable
- Available in Pb-free 100-pin TQFP package
- "ZZ" sleep mode option

Functional Description

The CY7C1339G SRAM integrates 128K × 32 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable ($\overline{CE_1}$), depth-expansion chip enables (CE_2 and $\overline{CE_3}$), burst control inputs (ADSC, ADSP, and ADV), write enables ($\overline{BW}_{[A:D]}$, and $\overline{BWE}$), and global write ($\overline{GW}$). Asynchronous inputs include the output enable ($\overline{OE}$) and the ZZ pin.

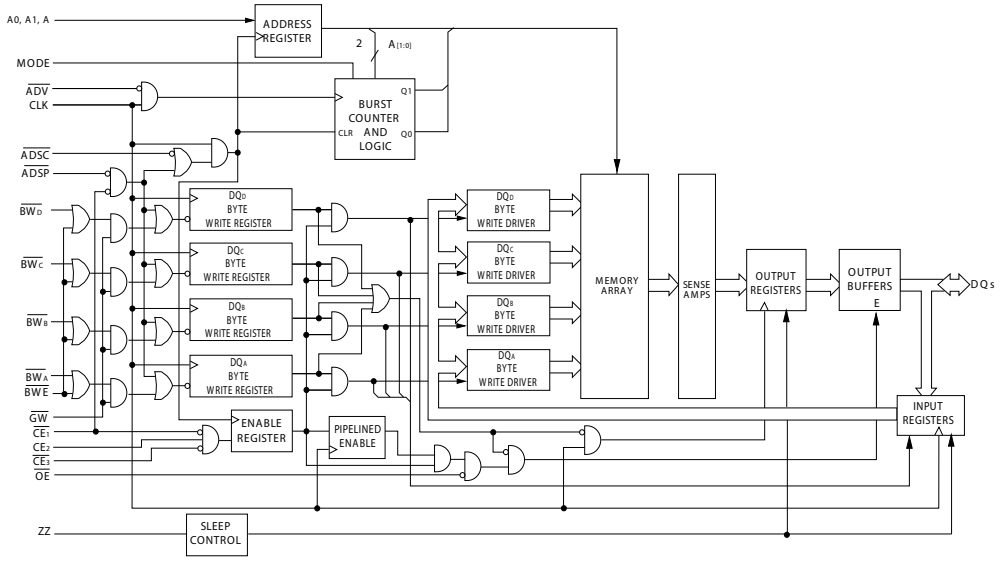
Addresses and chip enables are registered at rising edge of clock when either address strobe processor (ADSP) or address strobe controller (ADSC) are active. Subsequent burst addresses can be internally generated as controlled by the advance pin (ADV).

Address, data inputs, and write controls are registered on-chip to initiate a self-timed write cycle.This part supports byte write operations (see Pin Descriptions and Truth Table for further details). Write cycles can be one to four bytes wide as controlled by the byte write control inputs. GW when active LOW causes all bytes to be written.

The CY7C1339G operates from a +3.3 V core power supply while all outputs may operate with either a +2.5 or +3.3 V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

For a complete list of related documentation, click here.

Logic Block Diagram



Errata: For information on silicon errata, see "Errata" on page 20. Details include trigger conditions, devices affected, and proposed workaround.

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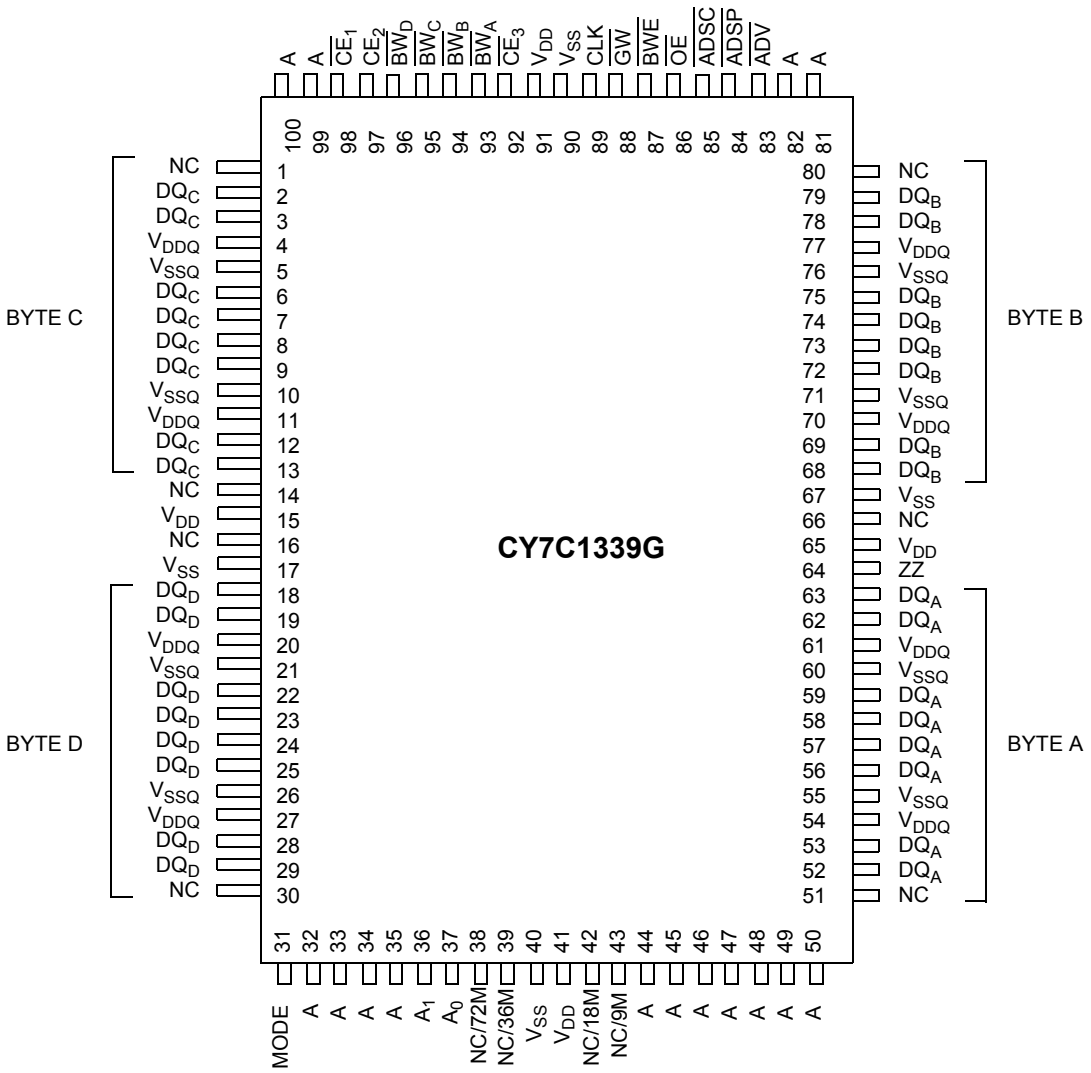
Selection Guide

Description	133 MHz	Unit
Maximum access time	4.0	ns
Maximum operating current	225	mA
Maximum CMOS standby current	40	mA

Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout [1]



Note
1. Errata: The ZZ pin (Pin 64) needs to be externally connected to ground. For more information, see "Errata" on page 20.

Pin Definitions

Name	I/O	Description
A_0, A_1, A	Input-synchronous	**Address inputs used to select one of the 128K address locations**. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are sampled active. A1:A0 are fed to the two-bit counter.
$\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$	Input-synchronous	**Byte write select inputs, active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-synchronous	**Global write enable input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (all bytes are written, regardless of the values on $\overline{BW}_{[A:D]}$ and $\overline{BWE}$).
$\overline{BWE}$	Input-synchronous	**Byte write enable input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-clock	**Clock input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
$\overline{CE}_1$	Input-synchronous	**Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
CE_2	Input-synchronous	**Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE}_3$	Input-synchronous	**Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-asynchronous	**Output enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	Input-synchronous	**Advance input signal, sampled on the rising edge of CLK, active LOW**. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input-synchronous	**Address strobe from processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1:A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. ASDP is ignored when $\overline{CE}_1$ is deasserted HIGH.
$\overline{ADSC}$	Input-synchronous	**Address strobe from controller, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. A1:A0 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
ZZ[2]	Input-asynchronous	**ZZ "sleep" input, active HIGH**. When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.

Note
2. Errata: The ZZ pin (Pin 64) needs to be externally connected to ground. For more information, see "Errata" on page 20.

Pin Definitions *(continued)*

Name	I/O	Description
DQs	I/O-synchronous	**Bidirectional data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs are placed in a tri-state condition.
V_{DD}	Power supply	**Power supply inputs to the core of the device**.
V_{SS}	Ground	**Ground for the core of the device**.
V_{DDQ}	I/O power supply	**Power supply for the I/O circuitry**.
V_{SSQ}	I/O ground	**Ground for the I/O circuitry**.
MODE	Input-static	**Selects burst order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode pin has an internal pull-up.
NC, NC/9M, NC/18M, NC/72M, NC/144M, NC/288M, NC/576M, NC/1G	–	**No Connects**. Not internally connected to the die. NC/9M, NC/18M, NC/72M, NC/144M, NC/288M, NC/576M and NC/1G are address expansion pins are not internally connected to the die.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 4.0 ns (133-MHz device).

The CY7C1339G supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the processor address strobe ($\overline{ADSP}$) or the controller address strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the byte write enable ($\overline{BWE}$) and byte write select ($\overline{BW}_{[A:D]}$) inputs. A global write enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous chip selects ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output tri-state control. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW, (2) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active, and (3) the write signals ($\overline{GW}$, $\overline{BWE}$) are all deserted HIGH. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH. The address presented to the address inputs (A) is stored into the address advancement logic and the address register while being presented to the memory array. The corresponding data is allowed to propagate to the input of the output registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within 2.6 ns (250-MHz device) if $\overline{OE}$ is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always tri-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the $\overline{OE}$ signal. Consecutive single read cycles are supported. Once the SRAM is deselected at clock rise by the chip select and either $\overline{ADSP}$ or $\overline{ADSC}$ signals, its output will tri-state immediately.

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when both of the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ is asserted LOW, and (2) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The Write signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}_{[A:D]}$) and $\overline{ADV}$ inputs are ignored during this first cycle.

$\overline{ADSP}$-triggered write accesses require two clock cycles to complete. If $\overline{GW}$ is asserted LOW on the second clock rise, the data presented to the DQs inputs is written into the corresponding address location in the memory array. If $\overline{GW}$ is HIGH, then the write operation is controlled by $\overline{BWE}$ and $\overline{BW}_{[A:D]}$ signals. The CY7C1339G provides byte write capability that is described in the Write Cycle Descriptions table. Asserting the byte write enable input ($\overline{BWE}$) with the selected byte write ($\overline{BW}_{[A:D]}$) input, will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed Write mechanism has been provided to simplify the Write operations.

Because the CY7C1339G is a common I/O device, the output enable ($\overline{OE}$) must be deserted HIGH before presenting data to the DQs inputs. Doing so will tri-state the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by $\overline{ADSC}$

$\overline{ADSC}$ Write accesses are initiated when the following conditions are satisfied: (1) $\overline{ADSC}$ is asserted LOW, (2) $\overline{ADSP}$ is deserted HIGH, (3) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active, and (4) the appropriate combination of the write inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}_{[A:D]}$) are asserted active to conduct a write to the desired byte(s). $\overline{ADSC}$-triggered write accesses require a single clock cycle to complete. The address presented to A is loaded into the address register and the address advancement logic while being delivered to the memory array. The $\overline{ADV}$ input is ignored during this cycle. If a global write is conducted, the data presented to the DQs is written into the corresponding address location in the memory core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY7C1339G is a common I/O device, the output enable ($\overline{OE}$) must be deserted HIGH before presenting data to the DQs inputs. Doing so will tri-state the output drivers. As a safety precaution, DQs are automatically tri-stated whenever a Write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY7C1339G provides a two-bit wraparound counter, fed by A1:A0, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting $\overline{ADV}$ LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both Read and Write burst operations are supported.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE}_1$, CE_2, $\overline{CE}_3$, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Snooze mode standby current	ZZ $\geq$ V_{DD} – 0.2 V	–	40	mA
t_{ZZS}	Device operation to ZZ	ZZ $\geq$ V_{DD} – 0.2 V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ $\leq$ 0.2 V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to snooze current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit snooze current	This parameter is sampled	0	–	ns

Truth Table

The truth table for CY7C1339G follows. [3, 4, 5, 6, 7, 8]

Operation	Add. Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect cycle, power-down	None	H	X	X	L	X	L	X	X	X	L–H	Tri-state
Deselect cycle, power-down	None	L	L	X	L	L	X	X	X	X	L–H	Tri-state
Deselect cycle, power-down	None	L	X	H	L	L	X	X	X	X	L–H	Tri-state
Deselect cycle, power-down	None	L	L	X	L	H	L	X	X	X	L–H	Tri-state
Deselect cycle, power-down	None	L	X	H	L	H	L	X	X	X	L–H	Tri-state
Snooze mode, power-down	None	X	X	X	H	X	X	X	X	X	X	Tri-state
READ cycle, begin burst	External	L	H	L	L	L	X	X	X	L	L–H	Q
READ cycle, begin burst	External	L	H	L	L	L	X	X	X	H	L–H	Tri-state
WRITE cycle, begin burst	External	L	H	L	L	H	L	X	L	X	L–H	D
READ cycle, begin burst	External	L	H	L	L	H	L	X	H	L	L–H	Q
READ cycle, begin burst	External	L	H	L	L	H	L	X	H	H	L–H	Tri-state
READ cycle, continue burst	Next	X	X	X	L	H	H	L	H	L	L–H	Q
READ cycle, continue burst	Next	X	X	X	L	H	H	L	H	H	L–H	Tri-state
READ cycle, continue burst	Next	H	X	X	L	X	H	L	H	L	L–H	Q
READ cycle, continue burst	Next	H	X	X	L	X	H	L	H	H	L–H	Tri-state
WRITE cycle, continue burst	Next	X	X	X	L	H	H	L	L	X	L–H	D
WRITE cycle, continue burst	Next	H	X	X	L	X	H	L	L	X	L–H	D
READ cycle, suspend burst	Current	X	X	X	L	H	H	H	H	L	L–H	Q
READ cycle, suspend burst	Current	X	X	X	L	H	H	H	H	H	L–H	Tri-state
READ cycle, suspend burst	Current	H	X	X	L	X	H	H	H	L	L–H	Q
READ cycle, suspend burst	Current	H	X	X	L	X	H	H	H	H	L–H	Tri-state
WRITE cycle, suspend burst	Current	X	X	X	L	H	H	H	L	X	L–H	D
WRITE cycle, suspend burst	Current	H	X	X	L	X	H	H	L	X	L–H	D

Notes

3. X = "Don't Care." H = Logic HIGH, L = Logic LOW.
4. $\overline{WRITE}$ = L when any one or more byte write enable signals ($\overline{BW_A}$, $\overline{BW_B}$, $\overline{BW_C}$, $\overline{BW_D}$) and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all byte write enable signals ($\overline{BW_A}$, $\overline{BW_B}$, $\overline{BW_C}$, $\overline{BW_D}$), $\overline{BWE}$, GW = H.
5. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
6. $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are available only in the TQFP package.
7. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_{[A:D]}}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state. $\overline{OE}$ is a don't care for the remainder of the write cycle.
8. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tri-state when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Partial Truth Table for Read/Write

The partial truth table for Read/Write for CY7C1339G follows. [9, 10]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_D}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write byte A – DQ_A	H	L	H	H	H	L
Write byte B – DQ_B	H	L	H	H	L	H
Write bytes B, A	H	L	H	H	L	L
Write byte C– DQ_C	H	L	H	L	H	H
Write bytes C, A	H	L	H	L	H	L
Write bytes C, B	H	L	H	L	L	H
Write bytes C, B, A	H	L	H	L	L	L
Write byte D– DQ_D	H	L	L	H	H	H
Write bytes D, A	H	L	L	H	H	L
Write bytes D, B	H	L	L	H	L	H
Write bytes D, B, A	H	L	L	H	L	L
Write bytes D, C	H	L	L	L	H	H
Write bytes D, C, A	H	L	L	L	H	L
Write bytes D, C, B	H	L	L	L	L	H
Write all bytes	H	L	L	L	L	L
Write all bytes	L	X	X	X	X	X

Notes
9. X = “Don't Care.” H = Logic HIGH, L = Logic LOW.
10. Table only lists a partial listing of the byte write combinations. Any combination of $\overline{BW}_X$ is valid. Appropriate write will be done based on which byte write is active.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{DD} relative to GND .....–0.5 V to +4.6 V

Supply voltage on V_{DDQ} relative to GND ..... –0.5 V to +V_{DD}

DC voltage applied to outputs in tri-state .....–0.5 V to V_{DDQ} + 0.5 V

DC input voltage .....–0.5 V to V_{DD} + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}

Electrical Characteristics

Over the Operating Range

Parameter [11, 12]	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power supply voltage			3.135	3.6	V
V_{DDQ}	I/O supply voltage			2.375	V_{DD}	V
V_{OH}	Output HIGH voltage	for 3.3 V I/O, I_{OH} = –4.0 mA		2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA		2.0	–	V
V_{OL}	Output LOW voltage	for 3.3 V I/O, I_{OL} = 8.0 mA		–	0.4	V
		for 2.5 V I/O, I_{OL} = 1.0 mA		–	0.4	V
V_{IH}	Input HIGH voltage [11.]	for 3.3 V I/O		2.0	V_{DD} + 0.3 V	V
		for 2.5 V I/O		1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW voltage [11.]	for 3.3 V I/O		–0.3	0.8	V
		for 2.5 V I/O		–0.3	0.7	V
I_X	Input leakage current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input current of MODE	Input = V_{SS}		–30	–	µA
		Input = V_{DD}		–	5	µA
	Input current of ZZ	Input = V_{SS}		–5	–	µA
		Input = V_{DD}		–	30	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{DDQ}, output disabled		–5	5	µA
I_{DD}	V_{DD} operating supply current	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	7.5-ns cycle, 133 MHz	–	225	mA
I_{SB1}	Automatic CE power-down current – TTL inputs	V_{DD} = Max, device deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX} = 1/t_{CYC}	7.5-ns cycle, 133 MHz	–	90	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs	V_{DD} = Max, device deselected, V_{IN} ≤ 0.3 V or V_{IN} ≥ V_{DDQ} – 0.3 V, f = 0	7.5-ns cycle, 133 MHz	–	40	mA
I_{SB3}	Automatic CE power-down current – CMOS inputs	V_{DD} = Max, device deselected, V_{IN} ≤ 0.3 V or V_{IN} ≥ V_{DDQ} – 0.3 V, f = f_{MAX} = 1/t_{CYC}	7.5-ns cycle, 133 MHz	–	75	mA
I_{SB4}	Automatic CE power-down current – TTL inputs	V_{DD} = Max, device deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = 0	7.5-ns cycle, 133 MHz	–	45	mA

Notes

11. Overshoot: $V_{IH(AC)}$ < V_{DD} + 1.5 V (Pulse width less than t_{CYC}/2), undershoot: $V_{IL(AC)}$ > –2 V (Pulse width less than t_{CYC}/2).
12. TPower-up: Assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

Capacitance

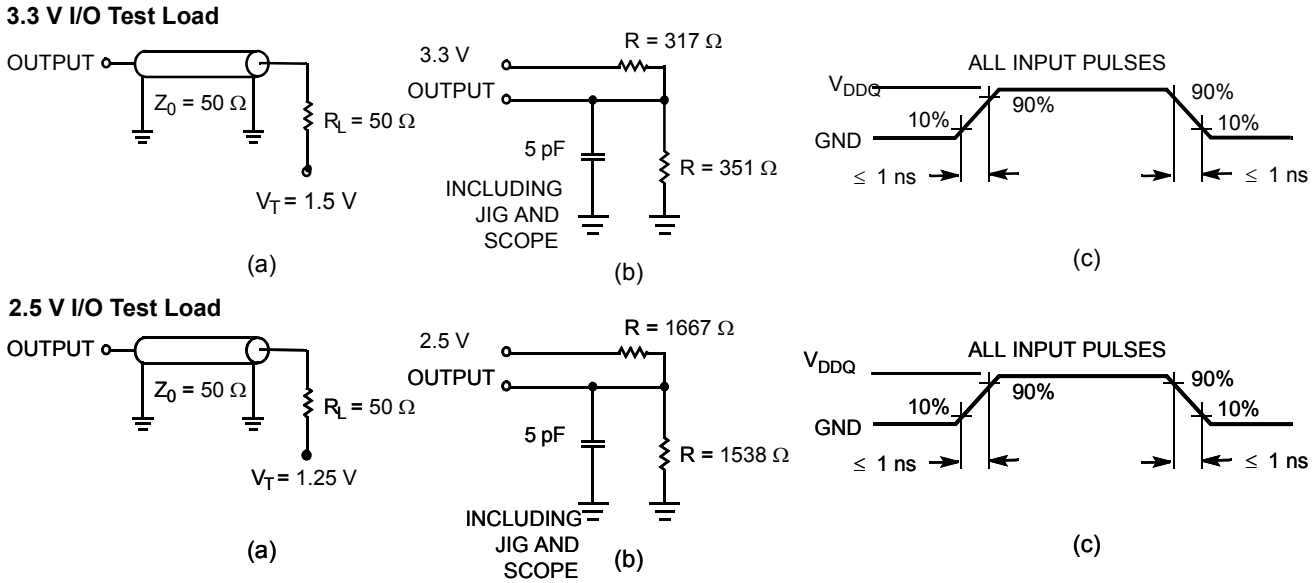
Parameter [13]	Description	Test Conditions	100-pin TQFP Package	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 3.3 V	5	pF
C_{CLK}	Clock input capacitance		5	pF
$C_{I/O}$	Input/output capacitance		5	pF

Thermal Resistance

Parameter [13]	Description	Test Conditions	100-pin TQFP Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	30.32	°C/W
Θ_{JC}	Thermal resistance (junction to case)		6.85	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Note
13. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

Over the Operating Range

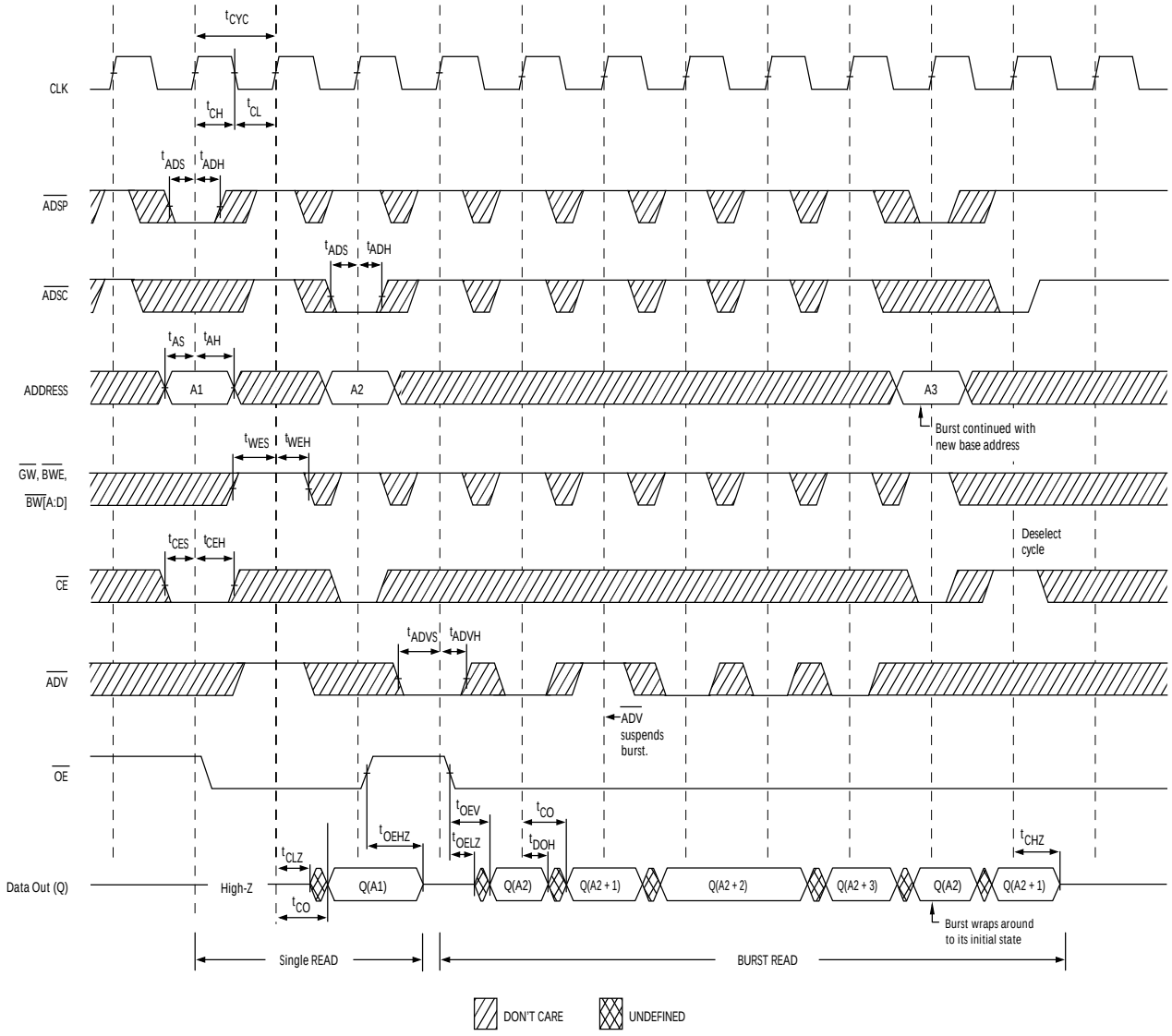
Parameter [14, 15]	Description	-133		Unit
		Min	Max	
t_{POWER}	V_{DD}(typical) to the first access [16]	1	–	ms
Clock				
t_{CYC}	Clock cycle time	7.5	–	ns
t_{CH}	Clock HIGH	3.0	–	ns
t_{CL}	Clock LOW	3.0	–	ns
Output Times				
t_{CO}	Data output valid after CLK rise	–	4.0	ns
t_{DOH}	Data output hold after CLK rise	1.5	–	ns
t_{CLZ}	Clock to low Z [17, 18, 19]	0	–	ns
t_{CHZ}	Clock to high Z [17, 18, 19]	–	4.0	ns
t_{OEV}	$\overline{OE}$ LOW to output valid	–	4.0	ns
t_{OELZ}	$\overline{OE}$ LOW to output low Z [17, 18, 19]	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to output high Z [17, 18, 19]	–	4.0	ns
Set-up Times				
t_{AS}	Address set-up before CLK rise	1.5	–	ns
t_{ADS}	$\overline{ADSC}$, $\overline{ADSP}$ set-up before CLK rise	1.5	–	ns
t_{ADVS}	$\overline{ADV}$ set-up before CLK rise	1.5	–	ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ set-up before CLK rise	1.5	–	ns
t_{DS}	Data input set-up before CLK rise	1.5	–	ns
t_{CES}	Chip enable set-up before CLK rise	1.5	–	ns
Hold Times				
t_{AH}	Address hold after CLK rise	0.5	–	ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ hold after CLK rise	0.5	–	ns
t_{ADVH}	$\overline{ADV}$ hold after CLK rise	0.5	–	ns
t_{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW_X}$ hold after CLK rise	0.5	–	ns
t_{DH}	Data input hold after CLK rise	0.5	–	ns
t_{CEH}	Chip enable hold after CLK rise	0.5	–	ns

Notes

14. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
15. Test conditions shown in (a) of Figure 2 on page 11 unless otherwise noted.
16. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above $V_{DD(minimum)}$ initially before a read or write operation can be initiated.
17. t_{CHZ}, t_{CLZ},t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 2 on page 11. Transition is measured ± 200 mV from steady-state voltage.
18. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.
19. This parameter is sampled and not 100% tested.

Switching Waveforms

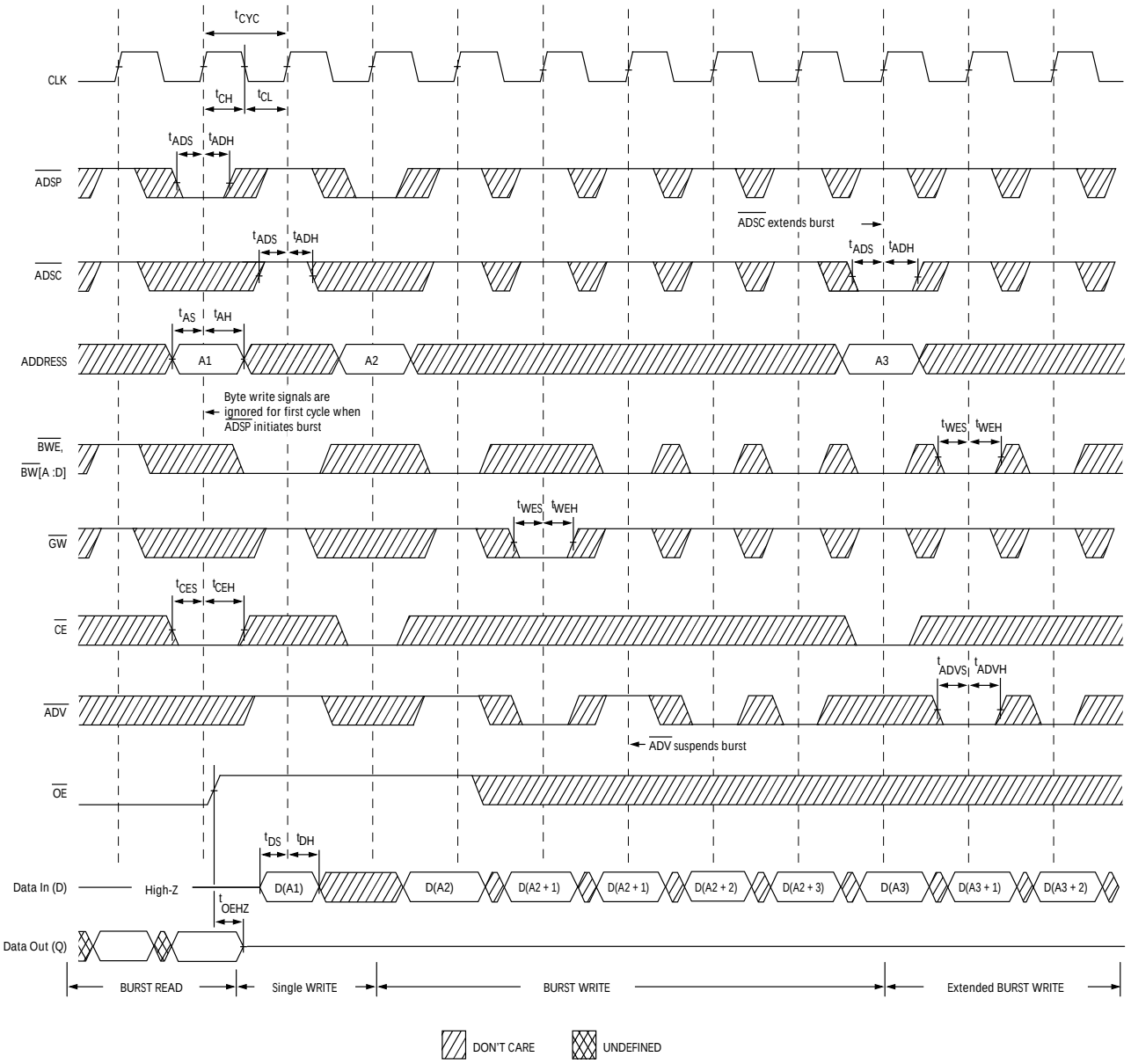
Figure 3. Read Cycle Timing [20]



Note
20. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

Switching Waveforms *(continued)*

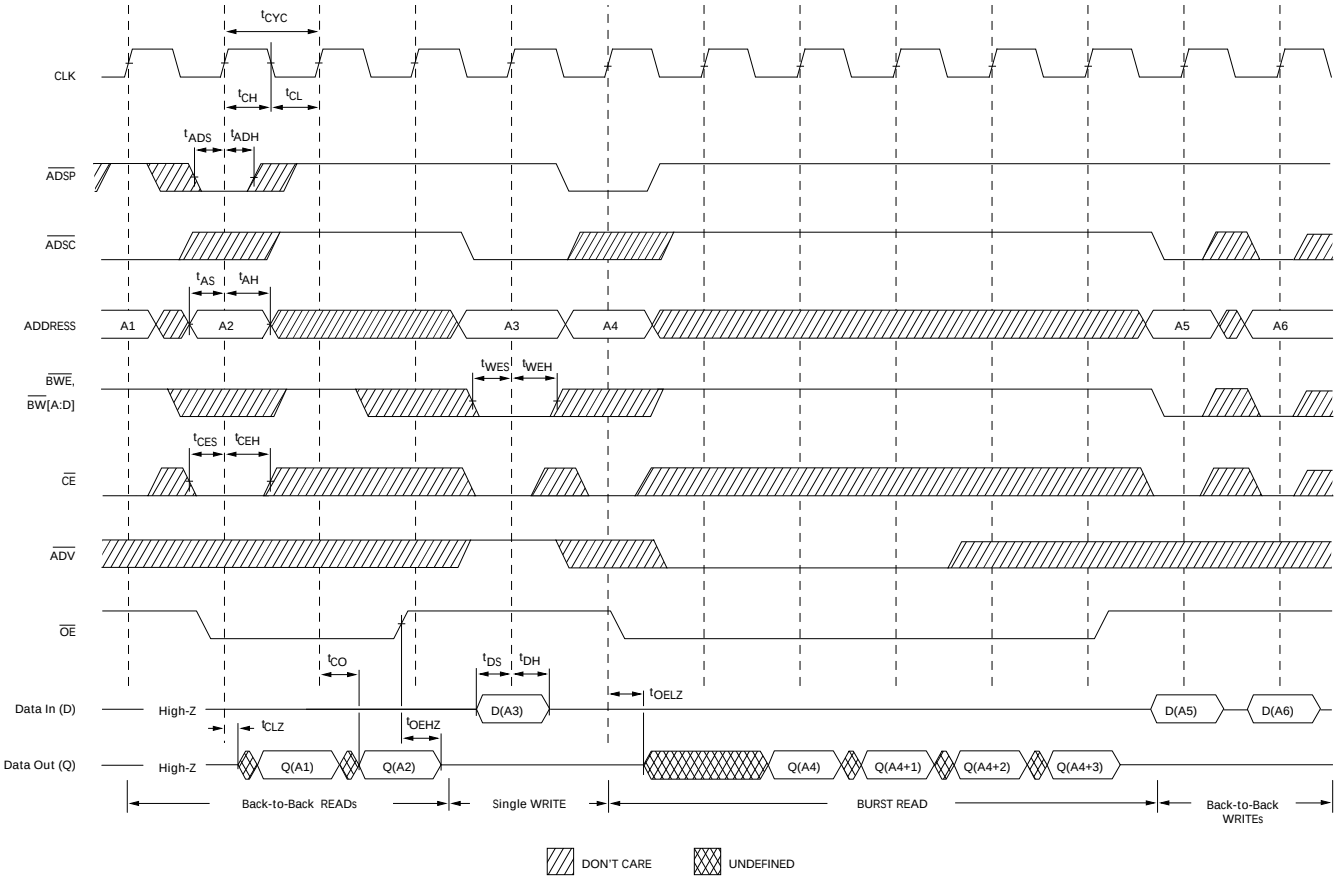
Figure 4. Write Cycle Timing [21, 22]



Notes
21. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
22. Full width write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}_{[A:D]}$ LOW.

Switching Waveforms *(continued)*

Figure 5. Read/Write Cycle Timing [23, 24, 25]

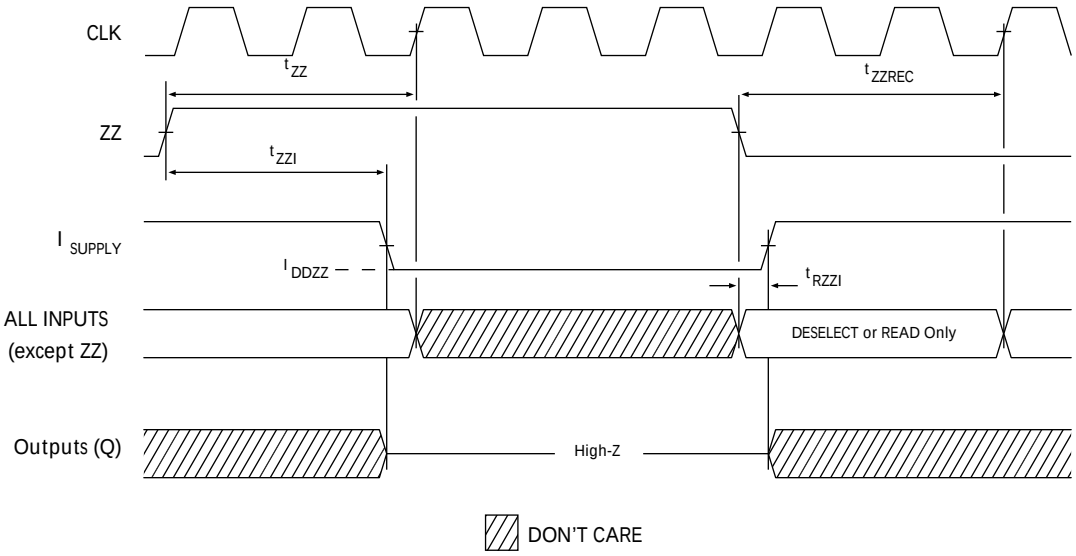


Notes

23. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
24. The data bus (Q) remains in high Z following a WRITE cycle, unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
25. $\overline{GW}$ is HIGH.

Switching Waveforms *(continued)*

Figure 6. ZZ Mode Timing [26, 27]



Notes
26. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
27. DQs are in high Z when exiting ZZ sleep mode.

Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available.
For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative.
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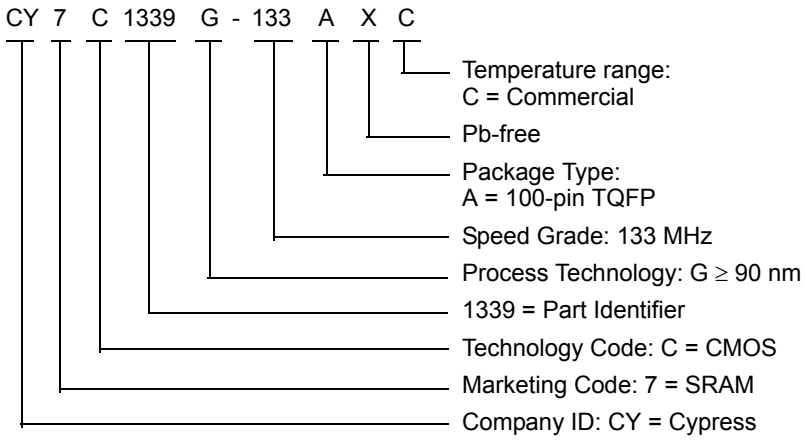
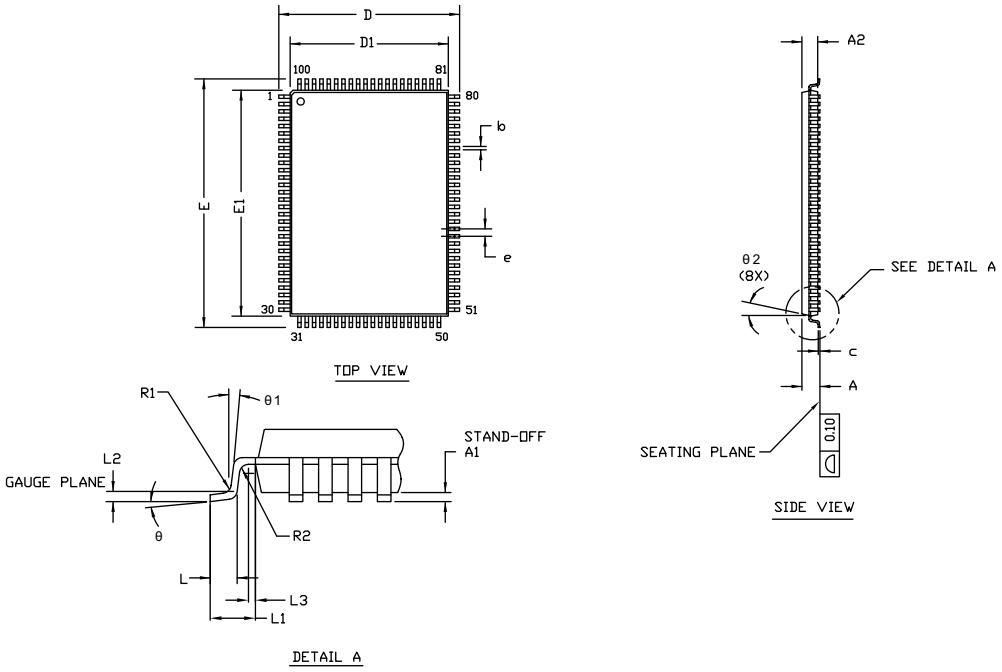
Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
133	CY7C1339G-133AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial

Ordering Code Definitions



Package Diagrams

Figure 7. 100-pin TQFP (16 × 22 × 1.6 mm) A100RA Package Outline, 51-85050



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
R1	0.08	—	0.20
R2	0.08	—	0.20
θ	0°	—	7°
θ1	0°	—	—
θ2	11°	12°	13°
c	—	—	0.20
b	0.22	0.30	0.38
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
L3	0.20	—	—
e	0.65 TYP		

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH. MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE. BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
3. JEDEC SPECIFICATION NO. REF: MS-026.

51-85050 *F

Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
EIA	Electronic Industries Alliance
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Errata

This section describes the Ram9 Sync ZZ pin issue. Details include trigger conditions, the devices affected, proposed workaround and silicon revision applicability. Please contact your local Cypress sales representative if you have further questions.

Part Numbers Affected

Density & Revision	Package Type	Operating Range
4Mb-Ram9 Synchronous SRAMs: CY7C133*G	100-pin TQFP	Commercial

Product Status

All of the devices in the Ram9 4Mb Sync family are qualified and available in production quantities.

Ram9 Sync ZZ Pin Issues Errata Summary

The following table defines the errata applicable to available Ram9 4Mb Sync family devices.

Item	Issues	Description	Device	Fix Status
1.	ZZ Pin	When asserted HIGH, the ZZ pin places device in a “sleep” condition with data integrity preserved.The ZZ pin currently does not have an internal pull-down resistor and hence cannot be left floating externally by the user during normal mode of operation.	4M-Ram9 (90 nm)	For the 4M Ram9 (90 nm) devices, there is no plan to fix this issue.

1. ZZ Pin Issue

- PROBLEM DEFINITION
  The problem occurs only when the device is operated in the normal mode with ZZ pin left floating. The ZZ pin on the SRAM device does not have an internal pull-down resistor. Switching noise in the system may cause the SRAM to recognize a HIGH on the ZZ input, which may cause the SRAM to enter sleep mode. This could result in incorrect or undesirable operation of the SRAM.

- TRIGGER CONDITIONS
  Device operated with ZZ pin left floating.

- SCOPE OF IMPACT
  When the ZZ pin is left floating, the device delivers incorrect data.

- WORKAROUND
  Tie the ZZ pin externally to ground.

- FIX STATUS
  For the 4M Ram9 (90 nm) devices, there is no plan to fix this issue.

Document History Page

Document Title: CY7C1339G, 4-Mbit (128K × 32) Pipelined Sync SRAM Document Number: 38-05520				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	224368	See ECN	RKF	New data sheet.
*A	288909	See ECN	VBL	Updated Ordering Information (Updated part numbers (Added Pb-free BGA package), changed TQFP package to Pb-free TQFP package).
*B	332895	See ECN	SYT	Updated Pin Configurations (Modified Address Expansion balls in the pinouts for 100-pin TQFP and 119-ball BGA Packages as per JEDEC standards). Updated Pin Definitions. Updated Electrical Characteristics (Updated test conditions for V_{OL} and V_{OH} parameters). Updated Thermal Resistance (Replaced TBDs for Θ_{JA} and Θ_{JC} to their respective values). Updated Ordering Information (By shading and unshading MPNs as per availability).
*C	351194	See ECN	PCI	Updated Ordering Information (Updated part numbers).
*D	366728	See ECN	PCI	Updated Electrical Characteristics (Updated test conditions for V_{DD} and V_{DDQ} parameters, updated Note 12 (Changed test condition from $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$).
*E	420883	See ECN	RXU	Changed status from Preliminary to Final. Changed address of Cypress Semiconductor Corporation from “3901 North First Street” to “198 Champion Court”. Updated Operating Range (Added Automotive Range). Updated Electrical Characteristics (Changed “Input Load Current except ZZ and MODE” to “Input Leakage Current except ZZ and MODE”). Updated Ordering Information (Updated part numbers, replaced Package Name column with Package Diagram in the Ordering Information table). Replaced Package Diagram of 51-85050 from *A to *B
*F	480368	See ECN	VKN	Updated Maximum Ratings (Added the Maximum Rating for Supply Voltage on V_{DDQ} Relative to GND). Updated Ordering Information (Updated part numbers).
*G	2896584	03/19/2010	NJY	Updated Ordering Information (Removed obsolete part numbers). Updated Package Diagrams.
*H	3045943	10/03/2010	NJY	Added Ordering Code Definitions. Added Acronyms and Units of Measure. Minor edits. Updated to new template.
*I	3052769	10/08/2010	NJY	Updated Ordering Information (Removed pruned part CY7C1339G-133AXI).
*J	3365114	09/07/2011	PRIT	Updated Package Diagrams. Updated to new template.

Document History Page *(continued)*

Document Title: CY7C1339G, 4-Mbit (128K × 32) Pipelined Sync SRAM Document Number: 38-05520				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
*K	3587066	05/10/2012	NJY / PRIT	Updated Features (Removed 250 MHz, 200 MHz, and 166 MHz frequencies related information, removed 119-ball BGA package related information). Updated Functional Description (Removed the Note “For best-practices recommendations, please refer to the Cypress application note *System Design Guidelines* on www.cypress.com.” and its reference). Updated Selection Guide (Removed 250 MHz, 200 MHz, and 166 MHz frequencies related information). Updated Pin Configurations (Removed 119-ball BGA package related information). Updated Pin Definitions (Removed 119-ball BGA package related information). Updated Functional Overview (Removed 250 MHz, 200 MHz, and 166 MHz frequencies related information). Updated Truth Table (Updated Note 6 (Removed 119-ball BGA package related information)). Updated Operating Range (Removed Industrial and Automotive Temperature Ranges). Updated Electrical Characteristics (Removed 250 MHz, 200 MHz, and 166 MHz frequencies related information, removed Industrial and Automotive Temperature Ranges). Updated Capacitance (Removed 119-ball BGA package related information). Updated Thermal Resistance (Removed 119-ball BGA package related information). Updated Switching Characteristics (Removed 250 MHz, 200 MHz, and 166 MHz frequencies related information). Updated Package Diagrams (Removed 119-ball BGA package related information).
*L	3766472	10/04/2012	PRIT	No technical updates. Completing Sunset Review.
*M	3984870	05/02/2013	PRIT	Added Errata.
*N	4039556	06/25/2013	PRIT	Added Errata Footnotes. Updated to new template.
*O	4150660	10/08/2013	PRIT	Updated Errata.
*P	4540469	10/16/2014	PRIT	Updated Package Diagrams: spec 51-85050 – Changed revision from *D to *E. Completing Sunset Review.
*Q	4575272	11/20/2014	PRIT	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*R	5514112	11/08/2016	PRIT	Updated Package Diagrams: spec 51-85050 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review.

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