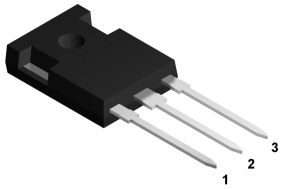
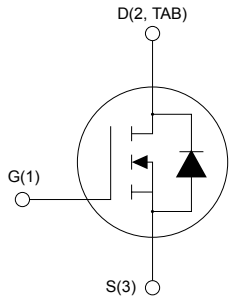
STWA60N043DM9

Datasheet

N-channel 600 V, 38 mΩ typ., 55 A MDmesh DM9 Power MOSFET in a TO-247 long leads package



TO-247 long leads



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Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STWA60N043DM9	600 V	43 mΩ	55 A

- Fast-recovery body diode
- Worldwide best $R_{DS(on)}$ per area among silicon-based fast recovery devices
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness

Applications

- Power supplies and converters
- LLC resonant converter

Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh DM9 technology, suitable for medium/high voltage MOSFETs featuring very low $R_{DS(on)}$ per area coupled with a fast-recovery diode. The silicon-based DM9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The fast-recovery diode featuring very low recovery charge (Q_{rr}), time (t_{rr}) and $R_{DS(on)}$ makes this fast-switching super-junction Power MOSFET tailored for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

Product status link
STWA60N043DM9

Product summary	
Order code	STWA60N043DM9
Marking	60N043DM9
Package	TO-247 long leads
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	55	A
	Drain current (continuous) at T_C = 100 °C	35	
I_{DM}(1)	Drain current (pulsed)	175	A
P_{TOT}	Total power dissipation at T_C = 25 °C	312	W
dv/dt(2)	Peak diode recovery voltage slope	120	V/ns
di/dt(2)	Peak diode recovery current slope	1300	A/µs
dv/dt(3)	MOSFET dv/dt ruggedness	120	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 28 A, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*
3. *V_{DS} ≤ 400 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.4	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	50	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	6	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 100 V)	839	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			5	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C (1)			200	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.5	4.0	4.5	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS} = 10 V, I_D = 28 A		38	43	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 400 V, f = 1 MHz, V_{GS} = 0 V	-	4675	-	pF
C_{oss}	Output capacitance		-	82	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 400 V, V_{GS} = 0 V	-	729	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, open drain	-	0.78	-	Ω
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 28 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	78.6	-	nC
Q_{gs}	Gate-source charge		-	29	-	nC
Q_{gd}	Gate-drain charge		-	20	-	nC

1. *$C_{oss\ eq}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to stated value.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 28 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	28	-	ns
t_r	Rise time		-	27	-	ns
$t_{d(off)}$	Turn-off delay time		-	77	-	ns
t_f	Fall time		-	5	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		55	A
I_{SDM}(1)	Source-drain current (pulsed)		-		175	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 56 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 56 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	165		ns
Q_{rr}	Reverse recovery charge		-	1.06		µC
I_{RRM}	Reverse recovery current		-	11		A
t_{rr}	Reverse recovery time	I_{SD} = 56 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	215		ns
Q_{rr}	Reverse recovery charge		-	2.2		µC
I_{RRM}	Reverse recovery current		-	18		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

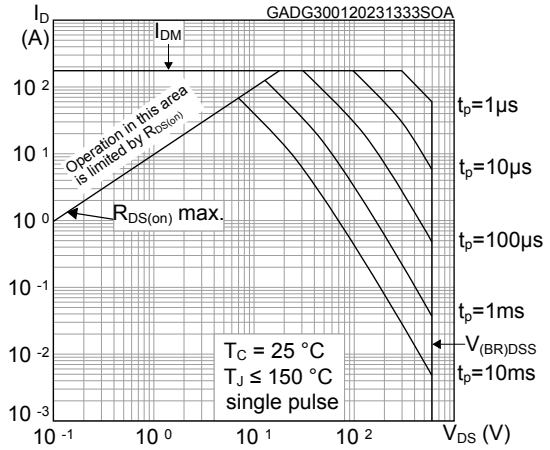


Figure 2. Maximum transient thermal impedance

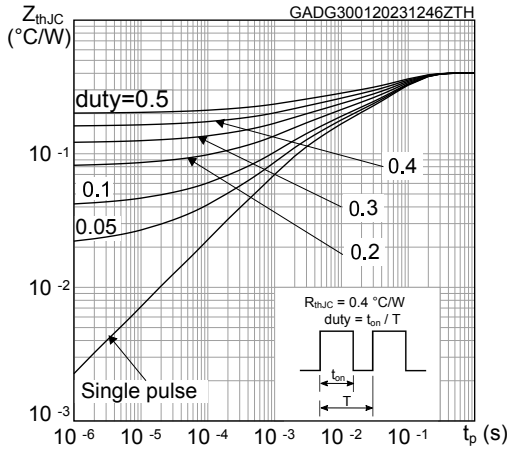


Figure 3. Typical output characteristics

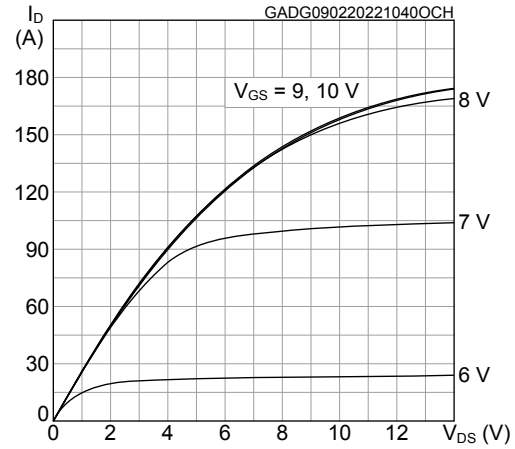


Figure 4. Typical transfer characteristics

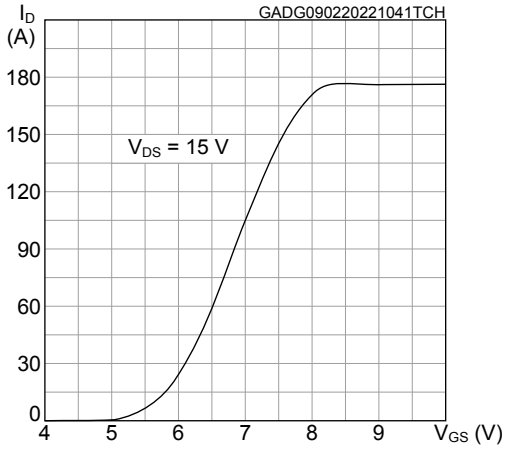


Figure 5. Typical gate charge characteristics

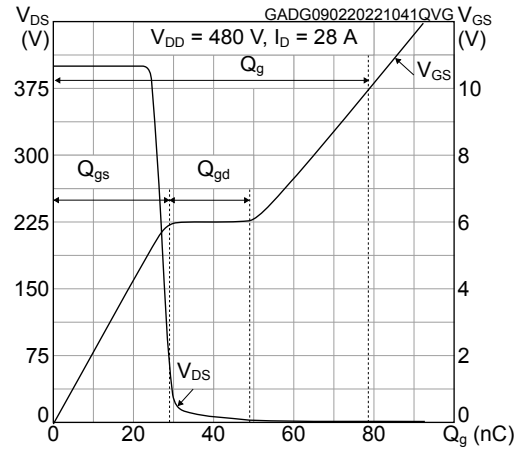


Figure 6. Typical drain-source on-resistance

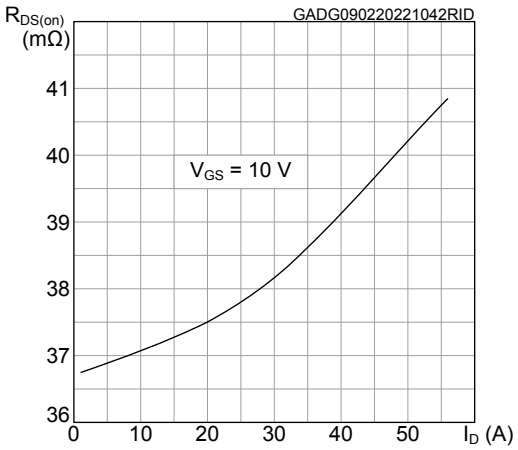


Figure 7. Typical capacitance characteristics

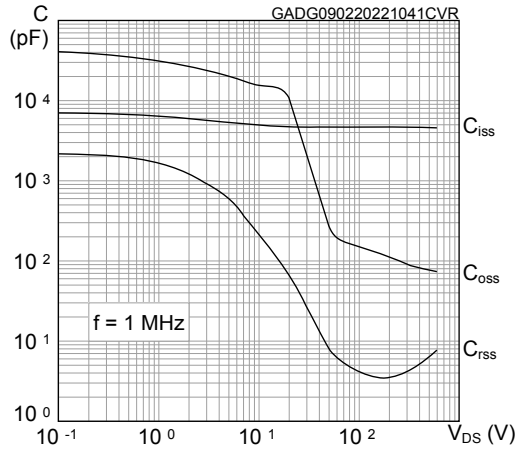


Figure 8. Typical output capacitance stored energy

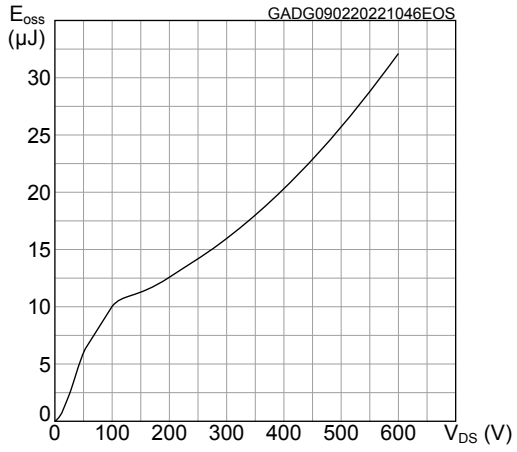


Figure 9. Normalized gate threshold vs temperature

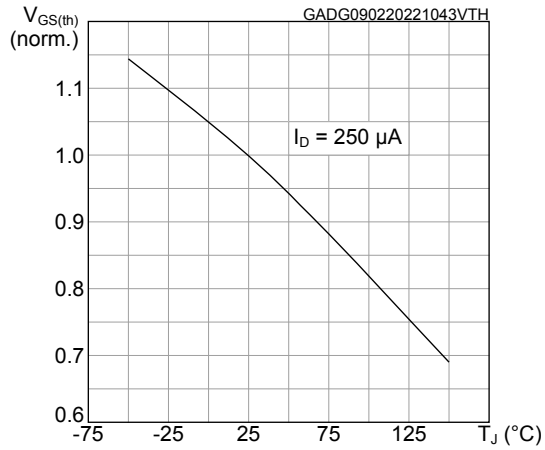


Figure 10. Normalized on-resistance vs temperature

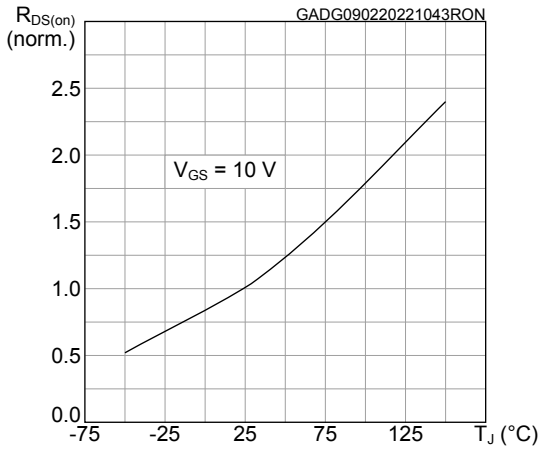


Figure 11. Normalized breakdown voltage vs temperature

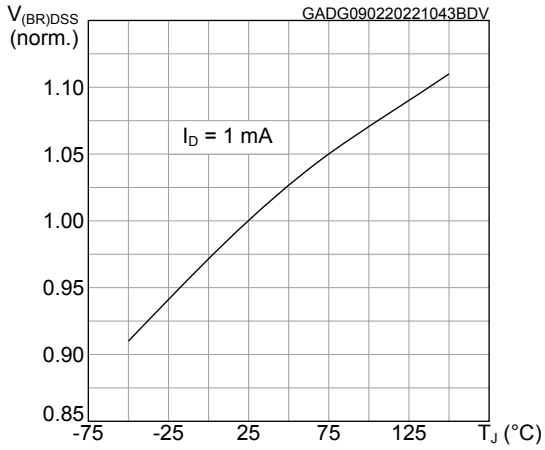
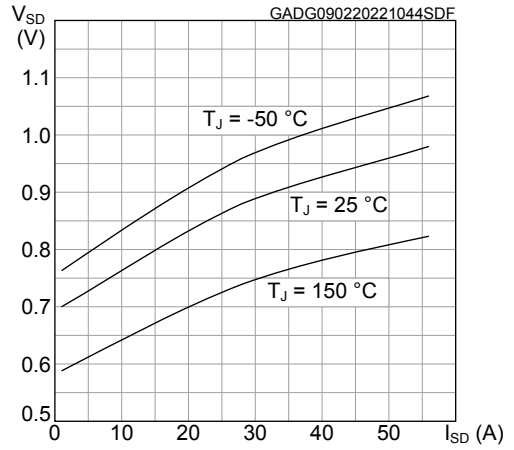


Figure 12. Typical reverse diode forward characteristics



3 Test circuits

Figure 13. Test circuit for resistive load switching times

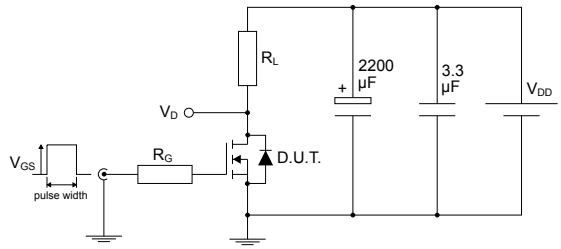


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Figure 14. Test circuit for gate charge behavior

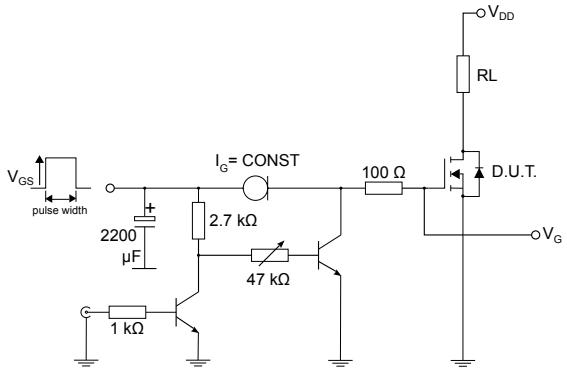

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Figure 15. Test circuit for inductive load switching and diode recovery times

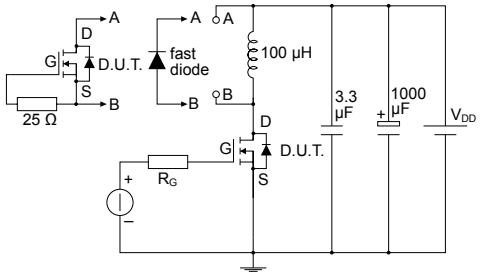

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Figure 16. Unclamped inductive load test circuit

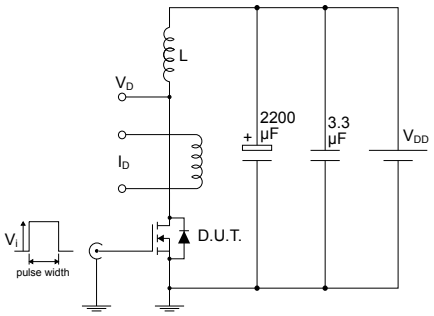

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Figure 17. Unclamped inductive waveform

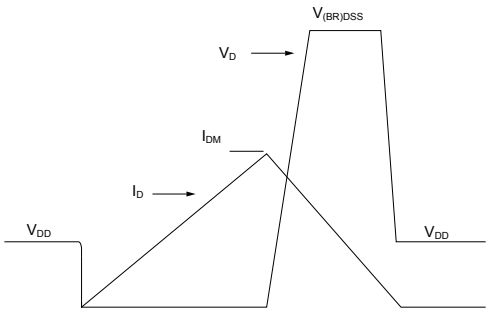

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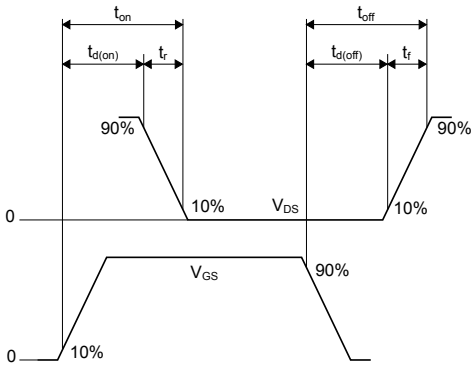
Figure 18. Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 long leads package information

Figure 19. TO-247 long leads package outline

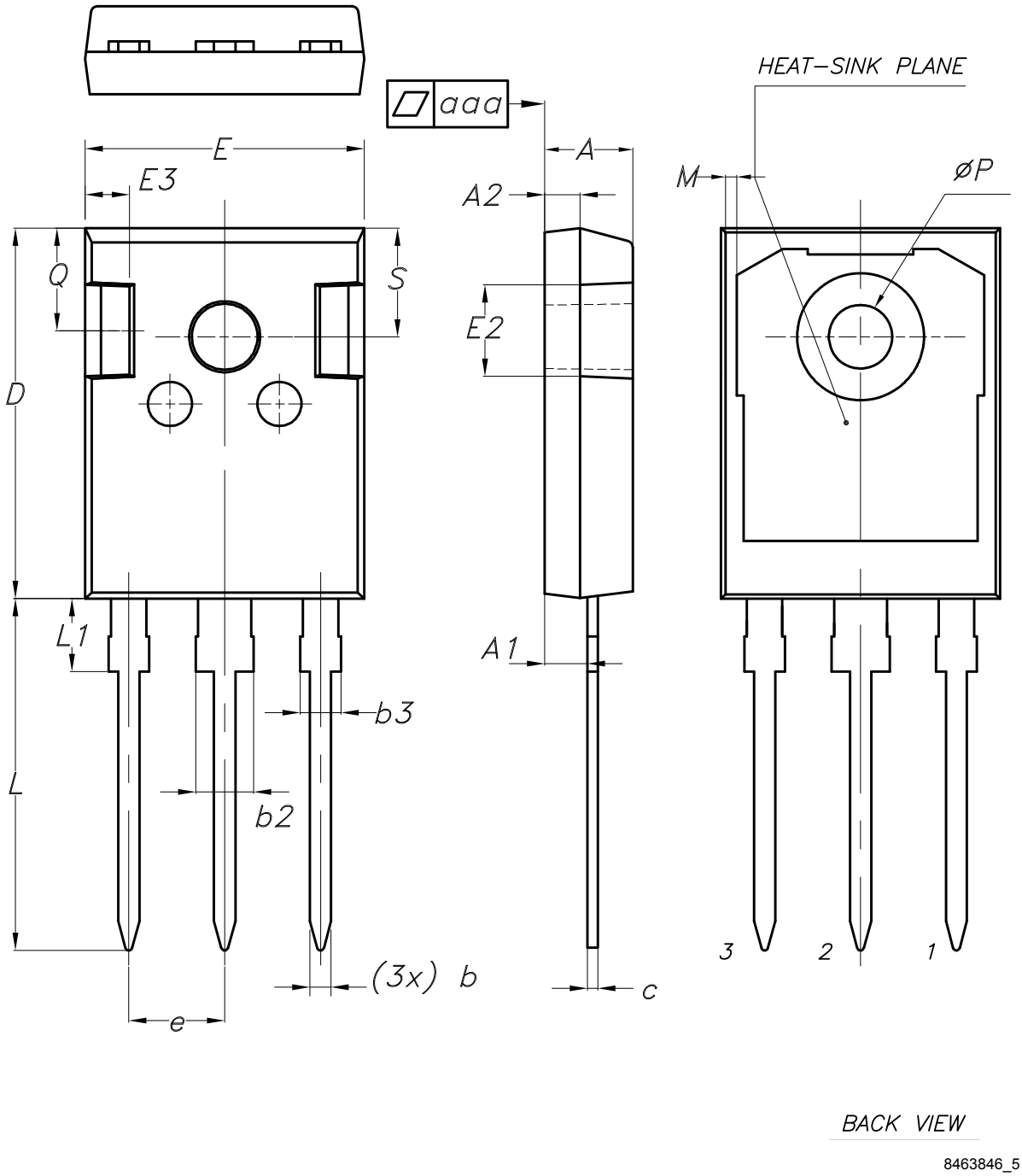

Table 8. **TO-247 long leads package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
c	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
M	0.35		0.95
P	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25
aaa		0.04	0.10

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
23-Feb-2023	1	First release.
28-Apr-2023	2	Updated *Table 6. Switching times.*
29-Aug-2023	3	Updated title and *Features* on cover page. Updated *Table 1. Absolute maximum ratings.* Updated *Table 6. Switching times.* Updated *Table 7. Source-drain diode.* Updated *Section 3 Test circuits.*
21-Mar-2024	4	Updated Table 3. Avalanche characteristics.

Contents